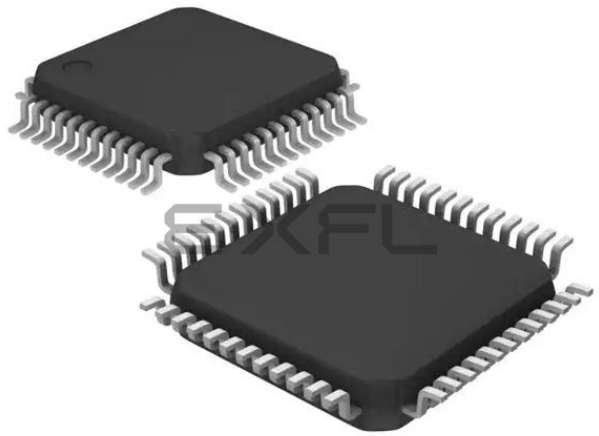

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Peripherals	LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	5.5V ~ 18V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
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Supplier Device Package	48-LQFP (7x7)
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Table 5-6. BDCCSRL Field Descriptions (continued)

Field	Description
0 ILLCMD	**Illegal Command Flag** — Indicates an illegal BDC command. This bit is set in the following cases: When an unimplemented BDC command opcode is received. When a DUMP_MEM{_WS}, FILL_MEM{_WS} or READ_SAME{_WS} is attempted in an illegal sequence. When an active BDM command is received whilst BDM is not active When a non Always-available command is received whilst the BDC is disabled or a flash mass erase is ongoing. When a non Always-available command is received whilst the device is secure Read commands return a value of 0xEE for each data byte Writing a “1” to this bit, clears the bit. 0 No illegal command detected. 1 Illegal BDC command detected.

5.4 Functional Description

5.4.1 Security

If the device resets with the system secured, the device clears the BDCCSR UNSEC bit. In the secure state BDC access is restricted to the BDCCSR register. A mass erase can be requested using the ERASE_FLASH command. If the mass erase is completed successfully, the device programs the security bits to the unsecure state and sets the BDC UNSEC bit. If the mass erase is unsuccessful, the device remains secure and the UNSEC bit is not set.

For more information regarding security, please refer to device specific security information.

5.4.2 Enabling BDC And Entering Active BDM

BDM can be activated only after being enabled. BDC is enabled by setting the ENBDC bit in the BDCCSR register, via the single-wire interface, using the command WRITE_BDCCSR.

After being enabled, BDM is activated by one of the following[1]:

- The BDC BACKGROUND command
- A CPU BGND instruction
- The DBG Breakpoint mechanism

Alternatively BDM can be activated directly from reset when resetting into Special Single Chip Mode.

The BDC is ready for receiving the first command 10 core clock cycles after the deassertion of the internal reset signal. This is delayed relative to the external pin reset as specified in the device reset documentation. On S12Z devices an NVM initialization phase follows reset. During this phase the BDC commands classified as always available are carried out immediately, whereas other BDC commands are subject to delayed response due to the NVM initialization phase.

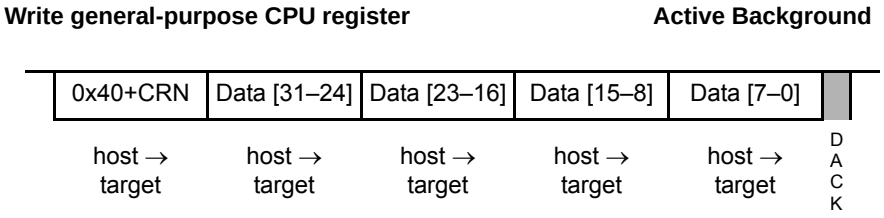
NOTE

After resetting into SSC mode, the initial PC address must be supplied by the host using the WRITE_Rn command before issuing the GO command.

1. BDM active immediately out of special single-chip reset.

The hardware forces low-order address bits to zero longword accesses to ensure these accesses are on 0-modulo-size alignments. Byte alignment details are described in Section 5.4.5.2, “BDC Access Of Device Memory Mapped Resources”.

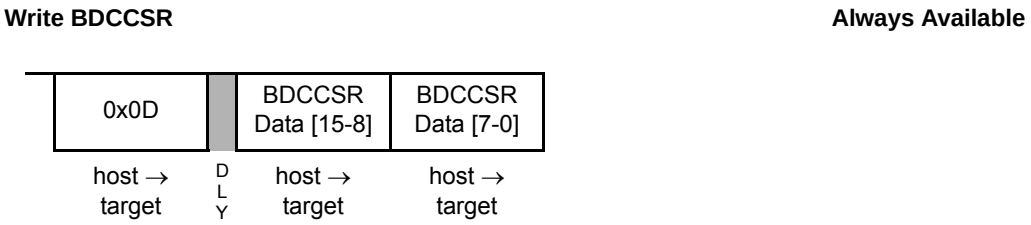
5.4.4.17 WRITE_Rn



If the device is in active BDM, this command writes the 32-bit operand to the selected CPU general-purpose register. See Section 5.4.5.1, “BDC Access Of CPU Registers for the CRN details. Accesses to CPU registers are always 32-bits wide, regardless of implemented register width. If enabled an ACK pulse is generated after the internal write access has been completed or aborted.

If the device is not in active BDM, this command is rejected as an illegal operation, the ILLCMD bit is set and no operation is performed.

5.4.4.18 WRITE_BDCCSR



16-bit write to the BDCCSR register. No ACK pulse is generated. Writing to this register can be used to configure control bits or clear flag bits. Refer to the register bit descriptions.

5.4.4.19 ERASE_FLASH

Mass erase the internal flash. This command can always be issued. On receiving this command twice in succession, the BDC sets the ERASE bit in BDCCSR and requests a flash mass erase. Any other BDC command following a single ERASE_FLASH initializes the sequence, such that thereafter the ERASE_FLASH must be applied twice in succession to request a mass erase. If 512 BDCSI clock cycles

Chapter 9
S12 Clock, Reset and Power Management Unit (S12CPMU_UHV)

Table 9-1. Revision History

Rev. No. (Item No)	Date (Submitted By)	Sections Affected	Substantial Change(s)
V09.00	8 Sept.2014		• initial version for ZVL128, copied from ZVL32 • CPMUPROT register: added CPMUVREGCTL2 to list of protected registers • added CPMUVREGCTL2 register containing 5V/3V option Bit and respective trim values
V09.01	21 Oct. 2014		• Improved Figure: Start up of clock system after Reset • Improved Figure: Full stop mode using Oscillator • Improved Figure: Enabling the external oscillator • Improved Table: Trimming effect of ACLKTR • Improved Table: Trimming effect of HTTR • Register Description for CPMUHTCTL: Added note on how to compute V_{HT} • Functional Description PBE Mode: Added Note that the clock system might stall if osc monitor reset disabled (OMRE=0) • Signal Descriptions: changed recommended resistor for BCTL pin to 1KΩ
V09.02	11 Nov. 2014		• Moved VREG5VEN bit to CPMUVREGCTL register
V09.03	14 Nov. 2014		• Corrected typos

9.1 Introduction

This specification describes the function of the Clock, Reset and Power Management Unit (S12CPMU_UHV).

- The Pierce oscillator (XOSCLCP) provides a robust, low-noise and low-power external clock source. It is designed for optimal start-up margin with typical crystal oscillators.
- The Voltage regulator (VREGAUTO) operates from the range 6V to 18V. It provides all the required chip internal voltages and voltage monitors.
- The Phase Locked Loop (PLL) provides a highly accurate frequency multiplier with internal filter.
- The Internal Reference Clock (IRC1M) provides a 1MHz internal clock.

10.3 Key Features

- Programmer’s Model with List Based Architecture for conversion command and result value organization
- Selectable resolution of 8-bit, 10-bit, or 12-bit
- Channel select control for n external analog input channels
- Provides up to eight device internal channels (please see the device reference manual for connectivity information and Figure 10-2)
- Programmable sample time
- A sample buffer amplifier for channel sampling (improved performance in view to influence of channel input path resistance versus conversion accuracy)
- Left/right justified result data
- Individual selectable VRH_0/1 and VRL_0/1 inputs (ADC12B_LBA V1 and V2) or VRH_0/1/2 inputs (ADC12B_LBA V3) on a conversion command basis (please see Figure 10-2, Table 10-2)
- Special conversions for selected VRH_0/1 (V1 and V2) or VRH_0/1/2 (V3), VRL_0/1 (V1 and V2) or VRL_0 (V3), (VRL_0/1 + VRH_0/1) / 2 (V1 and V2) or (VRL_0 + VRH_0/1/2) / 2 (V3) (please see Table 10-2)
- 15 conversion interrupts with flexible interrupt organization per conversion result
- One dedicated interrupt for “End Of List” type commands
- Command Sequence List (CSL) with a maximum number of 64 command entries
- Provides conversion sequence abort
- Restart from top of active Command Sequence List (CSL)
- The Command Sequence List and Result Value List are implemented in double buffered manner (two lists in parallel for each function)
- Conversion Command (CSL) loading possible from System RAM or NVM
- Single conversion flow control register with software selectable access path
- Two conversion flow control modes optimized to different application use cases
- Four option bits in the conversion command for top level SoC specific feature/function implementation option (Please refer to the device reference manual for details of the top level feature/function if implemented)

10.3.2 Block Diagram

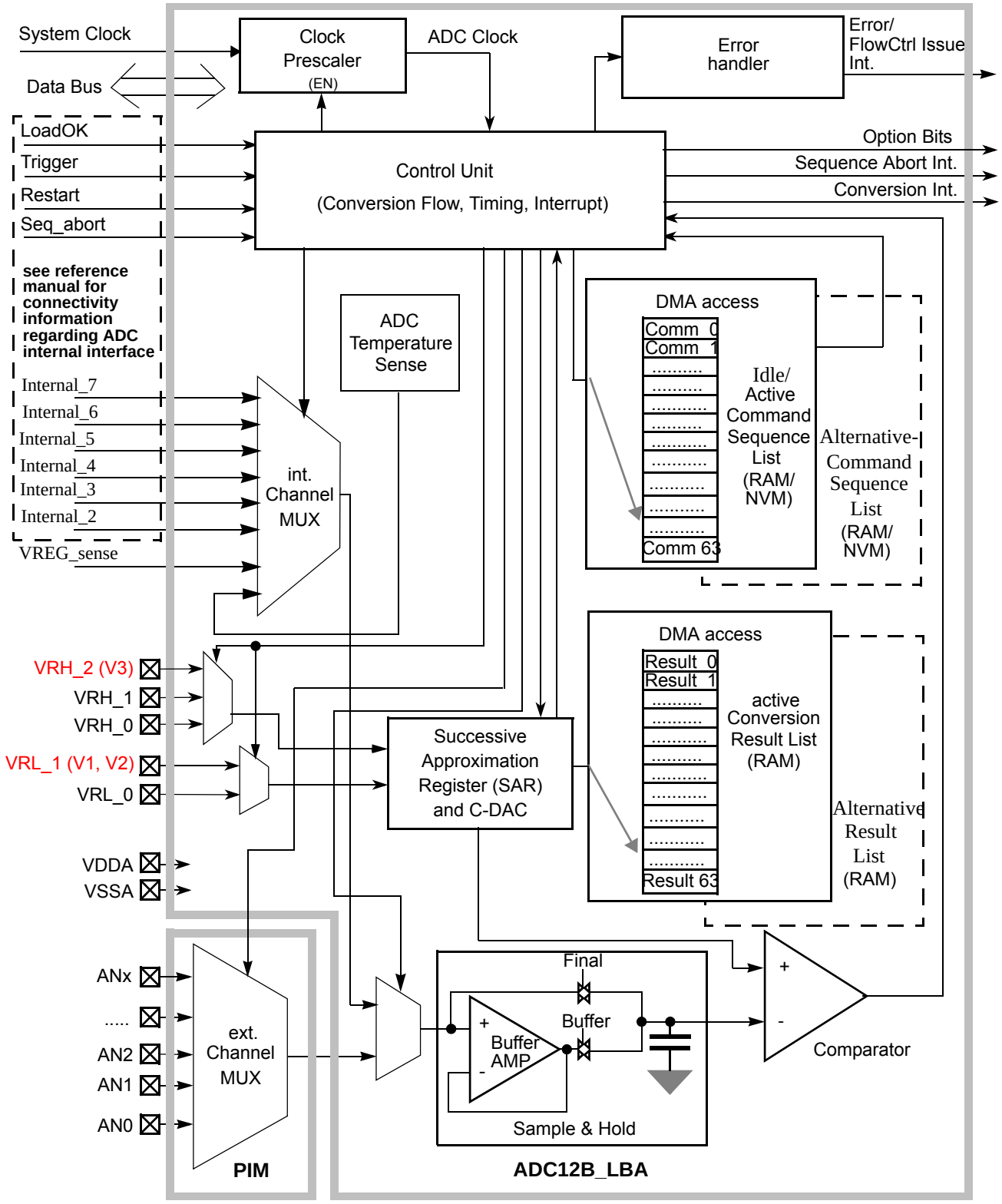


Figure 10-2. ADC12B_LBA Block Diagram

10.5.2.8 ADC Interrupt Enable Register (ADCIE)

Module Base + 0x0007

	7	6	5	4	3	2	1	0
R	SEQAD_IE	CONIF_OIE	Reserved	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 10-11. ADC Interrupt Enable Register (ADCIE)

Read: Anytime

Write: Anytime

Table 10-13. ADCIE Field Descriptions

Field	Description
7 SEQAD_IE	**Conversion Sequence Abort Done Interrupt Enable Bit** — This bit enables the conversion sequence abort event done interrupt. 0 Conversion sequence abort event done interrupt disabled. 1 Conversion sequence abort event done interrupt enabled.
6 CONIF_OIE	**ADCCONIF Register Flags Overrun Interrupt Enable** — This bit enables the flag which indicates if an overrun situation occurred for one of the CON_IF[15:1] flags or for the EOL_IF flag. 0 No ADCCONIF Register Flag overrun occurred. 1 ADCCONIF Register Flag overrun occurred.

If the WUPE bit in CANCTL0 is not asserted, the MSCAN will mask any activity it detects on CAN. RXCAN is therefore held internally in a recessive state. This locks the MSCAN in sleep mode. WUPE must be set before entering sleep mode to take effect.

The MSCAN is able to leave sleep mode (wake up) only when:

- CAN bus activity occurs and WUPE = 1

  or
- the CPU clears the SLPRQ bit

NOTE

The CPU cannot clear the SLPRQ bit before sleep mode (SLPRQ = 1 and SLPAK = 1) is active.

After wake-up, the MSCAN waits for 11 consecutive recessive bits to synchronize to the CAN bus. As a consequence, if the MSCAN is woken-up by a CAN frame, this frame is not received.

The receive message buffers (RxFG and RxBG) contain messages if they were received before sleep mode was entered. All pending actions will be executed upon wake-up; copying of RxBG into RxFG, message aborts and message transmissions. If the MSCAN remains in bus-off state after sleep mode was exited, it continues counting the 128 occurrences of 11 consecutive recessive bits.

13.4.5.6 MSCAN Power Down Mode

The MSCAN is in power down mode (Table 13-37) when

- CPU is in stop mode

  or
- CPU is in wait mode and the CSWAI bit is set

When entering the power down mode, the MSCAN immediately stops all ongoing transmissions and receptions, potentially causing CAN protocol violations. To protect the CAN bus system from fatal consequences of violations to the above rule, the MSCAN immediately drives TXCAN into a recessive state.

NOTE

The user is responsible for ensuring that the MSCAN is not active when power down mode is entered. The recommended procedure is to bring the MSCAN into Sleep mode before the STOP or WAI instruction (if CSWAI is set) is executed. Otherwise, the abort of an ongoing message can cause an error condition and impact other CAN bus devices.

In power down mode, all clocks are stopped and no registers can be accessed. If the MSCAN was not in sleep mode before power down mode became active, the module performs an internal recovery cycle after powering up. This causes some fixed delay before the module enters normal mode again.

Chapter 14
Supply Voltage Sensor (BATSV3)

Table 14-1. Revision History Table

Rev. No. (Item No.)	Data	Sections Affected	Substantial Change(s)
V02.00	16 Mar 2011	14.3.2.1 14.4.2.1	- added BVLS[1] to support four voltage level - moved BVHS to register bit 6
V03.00	26 Apr 2011	allBATSV3	- removed Vsense
V03.10	04 Oct 2011	14.4.2.1 and 14.4.2.2	- removed BSESE

14.1 Introduction

The BATS module provides the functionality to measure the voltage of the chip supply pin VSUP.

14.1.1 Features

The VSUP pin can be routed via an internal divider to the internal Analog to Digital Converter. Independent of the routing to the Analog to Digital Converter, it is possible to route this voltage to a comparator to generate a low or a high voltage interrupt to alert the MCU.

14.1.2 Modes of Operation

The BATS module behaves as follows in the system power modes:

1. Run mode

   The activation of the VSUP Level Sense Enable (BSUSE=1) or ADC connection Enable (BSUAE=1) closes the path from VSUP pin through the resistor chain to ground and enables the associated features if selected.

2. Stop mode

   During stop mode operation the path from the VSUP pin through the resistor chain to ground is opened and the low and high voltage sense features are disabled.
   The content of the configuration register is unchanged.

By enabling the PRNT bit of the TSCR1 register, the performance of the timer can be enhanced. In this case, it is possible to set additional prescaler settings for the main timer counter in the present timer by using PTPSR[7:0] bits of PTPSR register generating divide by 1, 2, 3, 4,....20, 21, 22, 23,.....255, or 256.

15.4.2 Input Capture

Clearing the I/O (input/output) select bit, IOSx, configures channel x as an input capture channel. The input capture function captures the time at which an external event occurs. When an active edge occurs on the pin of an input capture channel, the timer transfers the value in the timer counter into the timer channel registers, TCx.

The minimum pulse width for the input capture input is greater than two Bus clocks.

An input capture on channel x sets the CxF flag. The CxI bit enables the CxF flag to generate interrupt requests. Timer module must stay enabled (TEN bit of TSCR1 register must be set to one) while clearing CxF (writing one to CxF).

15.4.3 Output Compare

Setting the I/O select bit, IOSx, configures channel x when available as an output compare channel. The output compare function can generate a periodic pulse with a programmable polarity, duration, and frequency. When the timer counter reaches the value in the channel registers of an output compare channel, the timer can set, clear, or toggle the channel pin if the corresponding OCPDx bit is set to zero. An output compare on channel x sets the CxF flag. The CxI bit enables the CxF flag to generate interrupt requests. Timer module must stay enabled (TEN bit of TSCR1 register must be set to one) while clearing CxF (writing one to CxF).

The output mode and level bits, OMx and OLx, select set, clear, toggle on output compare. Clearing both OMx and OLx results in no output compare action on the output compare channel pin.

Setting a force output compare bit, FOCx, causes an output compare on channel x. A forced output compare does not set the channel flag.

Writing to the timer port bit of an output compare pin does not affect the pin state. The value written is stored in an internal latch. When the pin becomes available for general-purpose output, the last value written to the bit appears at the pin.

15.4.3.1 OC Channel Initialization

The internal register whose output drives OCx can be programmed before the timer drives OCx. The desired state can be programmed to this internal register by writing a one to CFORCx bit with TIOSx, OCPDx and TEN bits set to one.

Set OCx: Write a 1 to FOCx while TEN=1, IOSx=1, OMx=1, OLx=1 and OCPDx=1

Clear OCx: Write a 1 to FOCx while TEN=1, IOSx=1, OMx=1, OLx=0 and OCPDx=1

17.4.2.6 Center Aligned Outputs

For center aligned output mode selection, set the CAEx bit (CAEx = 1) in the PWMCAE register and the corresponding PWM output will be center aligned.

The 8-bit counter operates as an up/down counter in this mode and is set to up whenever the counter is equal to $00. The counter compares to two registers, a duty register and a period register as shown in the block diagram in Figure 17-16. When the PWM counter matches the duty register, the output flip-flop changes state, causing the PWM waveform to also change state. A match between the PWM counter and the period register changes the counter direction from an up-count to a down-count. When the PWM counter decrements and matches the duty register again, the output flip-flop changes state causing the PWM output to also change state. When the PWM counter decrements and reaches zero, the counter direction changes from a down-count back to an up-count and a load from the double buffer period and duty registers to the associated registers is performed, as described in Section 17.4.2.3, “PWM Period and Duty”. The counter counts from 0 up to the value in the period register and then back down to 0. Thus the effective period is PWMPERx*2.

NOTE

Changing the PWM output mode from left aligned to center aligned output (or vice versa) while channels are operating can cause irregularities in the PWM output. It is recommended to program the output mode before enabling the PWM channel.

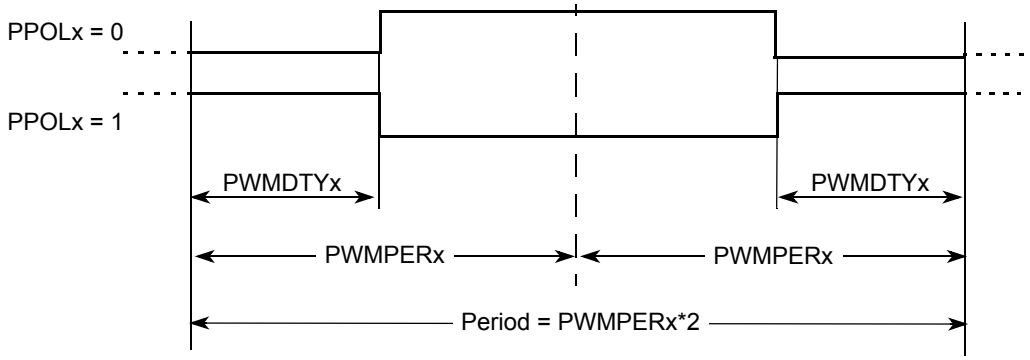


Figure 17-19. PWM Center Aligned Output Waveform

To calculate the output frequency in center aligned output mode for a particular channel, take the selected clock source frequency for the channel (A, B, SA, or SB) and divide it by twice the value in the period register for that channel.

- PWMx Frequency = Clock (A, B, SA, or SB) / (2*PWMPERx)
- PWMx Duty Cycle (high time as a% of period):
  - Polarity = 0 (PPOLx = 0)
    Duty Cycle = [(PWMPERx-PWMDTYx)/PWMPERx] * 100%
  - Polarity = 1 (PPOLx = 1)
    Duty Cycle = [PWMDTYx / PWMPERx] * 100%

As an example of a center aligned output, consider the following case:

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0006 SCIDRH	R	R8	T8	0	0	0	Reserved	Reserved	Reserved
	W								
0x0007 SCIDRL	R	R7	R6	R5	R4	R3	R2	R1	R0
	W	T7	T6	T5	T4	T3	T2	T1	T0

1.These registers are accessible if the AMAP bit in the SCISR2 register is set to zero.
2,These registers are accessible if the AMAP bit in the SCISR2 register is set to one.

= Unimplemented or Reserved

Figure 18-2. SCI Register Summary (Sheet 2 of 2)

18.3.2.1 SCI Baud Rate Registers (SCIBDH, SCIBDL)

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R W	SBR15	SBR14	SBR13	SBR12	SBR11	SBR10	SBR9	SBR8
Reset	0	0	0	0	0	0	0	0

Figure 18-3. SCI Baud Rate Register (SCIBDH)

Module Base + 0x0001

	7	6	5	4	3	2	1	0
R W	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
Reset	0	1	0	0	0	0	0	0

Figure 18-4. SCI Baud Rate Register (SCIBDL)

Read: Anytime, if AMAP = 0.

Write: Anytime, if AMAP = 0.

NOTE

Those two registers are only visible in the memory map if AMAP = 0 (reset condition).

The SCI baud rate register is used by to determine the baud rate of the SCI, and to control the infrared modulation/demodulation submodule.

Figure 18-17 shows two cases of break detect. In trace RXD_1 the break symbol starts with the start bit, while in RXD_2 the break starts in the middle of a transmission. If BRKDFE = 1, in RXD_1 case there will be no byte transferred to the receive buffer and the RDRF flag will not be modified. Also no framing error or parity error will be flagged from this transfer. In RXD_2 case, however the break signal starts later during the transmission. At the expected stop bit position the byte received so far will be transferred to the receive buffer, the receive data register full flag will be set, a framing error and if enabled and appropriate a parity error will be set. Once the break is detected the BRKDIF flag will be set.

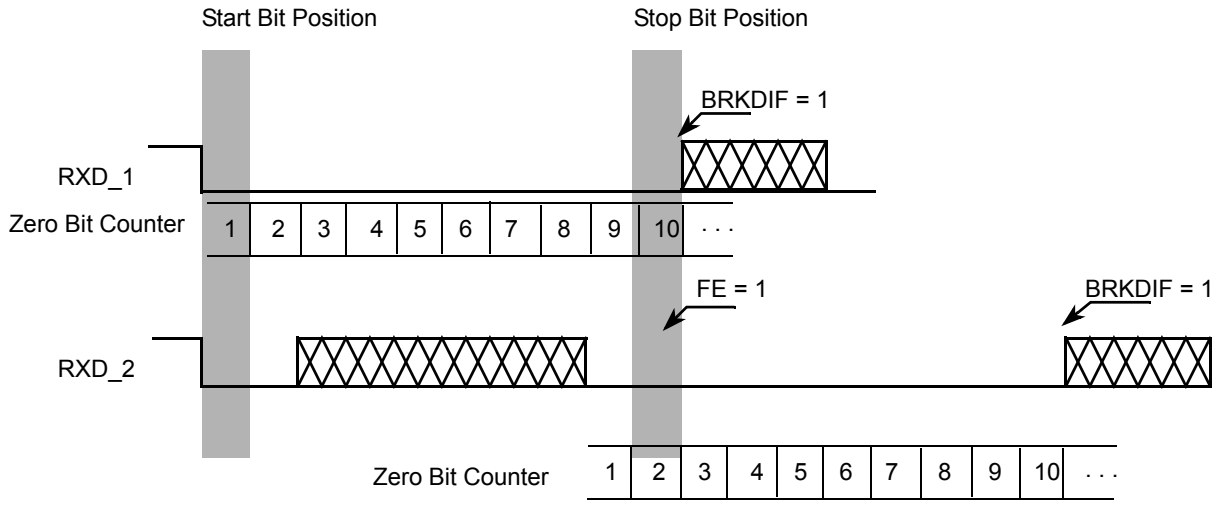


Figure 18-17. Break Detection if BRKDFE = 1 (M = 0)

18.4.5.4 Idle Characters

An idle character (or preamble) contains all logic 1s and has no start, stop, or parity bit. Idle character length depends on the M bit in SCI control register 1 (SCICR1). The preamble is a synchronizing idle character that begins the first transmission initiated after writing the TE bit from 0 to 1.

If the TE bit is cleared during a transmission, the TXD pin becomes idle after completion of the transmission in progress. Clearing and then setting the TE bit during a transmission queues an idle character to be sent after the frame currently being transmitted.

NOTE

When queueing an idle character, return the TE bit to logic 1 before the stop bit of the current frame shifts out through the TXD pin. Setting TE after the stop bit appears on TXD causes data previously written to the SCI data register to be lost. Toggle the TE bit for a queued idle character while the TDRE flag is set and immediately before writing the next byte to the SCI data register.

If the TE bit is clear and the transmission is complete, the SCI is not the master of the TXD pin

As the receiver samples an incoming frame, it re-synchronizes the RT clock on any valid falling edge within the frame. Re synchronization within frames will correct a misalignment between transmitter bit times and receiver bit times.

18.4.6.5.1 Slow Data Tolerance

Figure 18-28 shows how much a slow received frame can be misaligned without causing a noise error or a framing error. The slow stop bit begins at RT8 instead of RT1 but arrives in time for the stop bit data samples at RT8, RT9, and RT10.

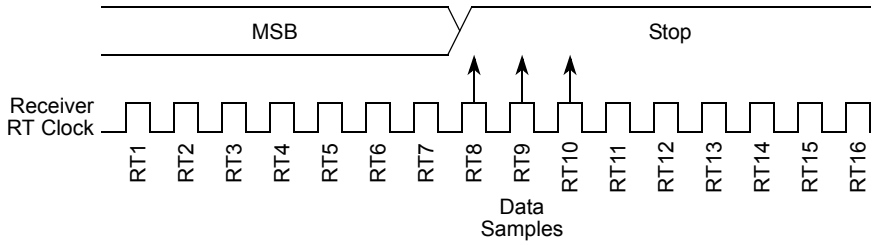


Figure 18-28. Slow Data

Let’s take RTr as receiver RT clock and RTt as transmitter RT clock.

For an 8-bit data character, it takes the receiver 9 bit times x 16 RTr cycles +7 RTr cycles = 151 RTr cycles to start data sampling of the stop bit.

With the misaligned character shown in Figure 18-28, the receiver counts 151 RTr cycles at the point when the count of the transmitting device is 9 bit times x 16 RTt cycles = 144 RTt cycles.

The maximum percent difference between the receiver count and the transmitter count of a slow 8-bit data character with no errors is:

((151 – 144) / 151) x 100 = 4.63%

For a 9-bit data character, it takes the receiver 10 bit times x 16 RTr cycles + 7 RTr cycles = 167 RTr cycles to start data sampling of the stop bit.

With the misaligned character shown in Figure 18-28, the receiver counts 167 RTr cycles at the point when the count of the transmitting device is 10 bit times x 16 RTt cycles = 160 RTt cycles.

The maximum percent difference between the receiver count and the transmitter count of a slow 9-bit character with no errors is:

((167 – 160) / 167) X 100 = 4.19%

18.4.6.5.2 Fast Data Tolerance

Figure 18-29 shows how much a fast received frame can be misaligned. The fast stop bit ends at RT10 instead of RT16 but is still sampled at RT8, RT9, and RT10.

Table 18-20. SCI Interrupt Sources

RXEDGIF	SCIASR1[7]	RXEDGIE	Active high level. Indicates that an active edge (falling for RXPOL = 0, rising for RXPOL = 1) was detected.
BERRIF	SCIASR1[1]	BERRIE	Active high level. Indicates that a mismatch between transmitted and received data in a single wire application has happened.
BKDIF	SCIASR1[0]	BRKDIE	Active high level. Indicates that a break character has been received.

18.5.3.1 Description of Interrupt Operation

The SCI only originates interrupt requests. The following is a description of how the SCI makes a request and how the MCU should acknowledge that request. The interrupt vector offset and interrupt number are chip dependent. The SCI only has a single interrupt line (SCI Interrupt Signal, active high operation) and all the following interrupts, when generated, are ORed together and issued through that port.

18.5.3.1.1 TDRE Description

The TDRE interrupt is set high by the SCI when the transmit shift register receives a byte from the SCI data register. A TDRE interrupt indicates that the transmit data register (SCIDRH/L) is empty and that a new byte can be written to the SCIDRH/L for transmission.Clear TDRE by reading SCI status register 1 with TDRE set and then writing to SCI data register low (SCIDRL).

18.5.3.1.2 TC Description

The TC interrupt is set by the SCI when a transmission has been completed. Transmission is completed when all bits including the stop bit (if transmitted) have been shifted out and no data is queued to be transmitted. No stop bit is transmitted when sending a break character and the TC flag is set (providing there is no more data queued for transmission) when the break character has been shifted out. A TC interrupt indicates that there is no transmission in progress. TC is set high when the TDRE flag is set and no data, preamble, or break character is being transmitted. When TC is set, the TXD pin becomes idle (logic 1). Clear TC by reading SCI status register 1 (SCISR1) with TC set and then writing to SCI data register low (SCIDRL).TC is cleared automatically when data, preamble, or break is queued and ready to be sent.

18.5.3.1.3 RDRF Description

The RDRF interrupt is set when the data in the receive shift register transfers to the SCI data register. A RDRF interrupt indicates that the received data has been transferred to the SCI data register and that the byte can now be read by the MCU. The RDRF interrupt is cleared by reading the SCI status register one (SCISR1) and then reading SCI data register low (SCIDRL).

18.5.3.1.4 OR Description

The OR interrupt is set when software fails to read the SCI data register before the receive shift register receives the next frame. The newly acquired data in the shift register will be lost in this case, but the data already in the SCI data registers is not affected. The OR interrupt is cleared by reading the SCI status register one (SCISR1) and then reading SCI data register low (SCIDRL).

22.3.2.9 P-Flash Protection Register (FPROT)

The FPROT register defines which P-Flash sectors are protected against program and erase operations.

Offset Module Base + 0x0008

	7	6	5	4	3	2	1	0
R	FPOPEN	RNV6	FPHDIS	FPHS[1:0]		FPLDIS	FPLS[1:0]	
W								
Reset	F[1]	F[1]	F[1]	F[1]	F[1]	F[1]	F[1]	F[1]

= Unimplemented or Reserved

Figure 22-13. Flash Protection Register (FPROT)

[1] Loaded from Flash configuration field, during reset sequence.

The (unreserved) bits of the FPROT register are writable Normal Single Chip Mode with the restriction that the size of the protected region can only be increased see Section 22.3.2.9.1, “P-Flash Protection Restrictions,” and Table 22-22). All (unreserved) bits of the FPROT register are writable without restriction in Special Single Chip Mode.

During the reset sequence, the FPROT register is loaded with the contents of the P-Flash protection byte in the Flash configuration field at global address 0xFF_FE0C located in P-Flash memory (see Table 22-3) as indicated by reset condition ‘F’ in Figure 22-13. To change the P-Flash protection that will be loaded during the reset sequence, the upper sector of the P-Flash memory must be unprotected, then the P-Flash protection byte must be reprogrammed. If a double bit fault is detected while reading the P-Flash phrase containing the P-Flash protection byte during the reset sequence, the FPOPEN bit will be cleared and remaining bits in the FPROT register will be set to leave the P-Flash memory fully protected.

Trying to alter data in any protected area in the P-Flash memory will result in a protection violation error and the FPVIOL bit will be set in the FSTAT register. The block erase of a P-Flash block is not possible if any of the P-Flash sectors contained in the same P-Flash block are protected.

Table 22-18. FPROT Field Descriptions

Field	Description
7 FPOPEN	**Flash Protection Operation Enable** — The FPOPEN bit determines the protection function for program or erase operations as shown in Table 22-19 for the P-Flash block. 0 When FPOPEN is clear, the FPHDIS and FPLDIS bits define unprotected address ranges as specified by the corresponding FPHS and FPLS bits 1 When FPOPEN is set, the FPHDIS and FPLDIS bits enable protection for the address range specified by the corresponding FPHS and FPLS bits
6 RNV[6]	**Reserved Nonvolatile Bit** — The RNV bit should remain in the erased state for future enhancements.
5 FPHDIS	**Flash Protection Higher Address Range Disable** — The FPHDIS bit determines whether there is a protected/unprotected area in a specific region of the P-Flash memory ending with global address 0xFF_FFFF. 0 Protection/Unprotection enabled 1 Protection/Unprotection disabled
4–3 FPHS[1:0]	**Flash Protection Higher Address Size** — The FPHS bits determine the size of the protected/unprotected area in P-Flash memory as shown inTable 22-20. The FPHS bits can only be written to while the FPHDIS bit is set.

A.1.6 Power Dissipation and Thermal Characteristics

Power dissipation and thermal characteristics are closely related. The user must assure that the maximum operating junction temperature is not exceeded. The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \Theta_{JA})$$

T_J = Junction Temperature, [°C]

T_A = Ambient Temperature, [°C]

P_D = Total Chip Power Dissipation, [W]

Θ_{JA} = Package Thermal Resistance, [°C/W]

The total power dissipation P_D can be calculated from the equation below. Table A-6 below lists the power dissipation components. Table A-7 gives an overview of the supply currents.

$$P_D = P_{VSUP} + P_{BCTL} + P_{INT} - P_{GPIO} + P_{LIN} - P_{PP7}$$

Table A-7. Power Dissipation Components

Power Component	Description
$P_{SUP} = V_{SUP}\ I_{SUP}$	Internal Power through VSUP pin
$P_{BCTL} = V_{BCTL}\ I_{BCTL}$	Internal Power through BCTL pin
$P_{INT} = V_{DDX}\ I_{VDDX} + V_{DDA}\ I_{VDDA}$	Internal Power through VDDX/A pins.
$P_{GPIO} = V_{I/O}\ I_{I/O}$	Power dissipation of external load driven by GPIO Port. Assuming the load is connected between GPIO and ground. This power component is included in P_{INT} and is subtracted from overall MCU power dissipation P_D.
$P_{LIN} = V_{LIN}\ I_{LIN}$	Power dissipation of LINPHY
$P_{PP7} = V_{DDX}\ I_{PP7}$	Power dissipation of PP7 pin. Assuming the load is connected between PP7 and ground. This power component is included in P_{INT} and is subtracted from overall MCU power dissipation P_D.

Table A-11. 3.3V I/O Characteristics (Junction Temperature From –40°C To +175°C)

Conditions are 3.2V ≤ V_{DDX} ≤ 3.39V,
unless otherwise noted. I/O Characteristics for all GPIO pins (defined in A.1.1.1/A-671).

Num	Rating	Symbol	Min	Typ	Max	Unit
1a	Input high voltage	V_{IH}	0.65*V_{DDX}	—	—	V
1b	Input high voltage BKGD pin, 3.15 V < V_{DDX} <5.5V	V_{IH}	0.65*V_{DDX}	—	—	V
2	Input high voltage	V_{IH}	—	—	V_{DDX}+0.3	V
3a	Input low voltage	V_{IL}	—	—	0.30*V_{DDX}	V
3b	Input low voltage BKGD pin, 3.15 V < V_{DDX} <5.5V	V_{IL}	—	—	0.30*V_{DDX}	V
4	Input low voltage	V_{IL}	V_{SSX}–0.3	—	—	V
5	Input hysteresis	V_{HYS}	—	250	—	mV
6	Input leakage current on all GPIO except PP1, PP3, PP5 and PP7 (Pins in high impedance input mode) [1] V_{in} = V_{DDX} or V_{SSX}	I_{in}	-1	—	1	µA
7	Input leakage current on PP1, PP3, PP5 and PP7 (Pins in high impedance input mode)[1] V_{in} = V_{DDX} or V_{SSX}	I_{in}	-2.5	—	2.5	µA
8	Output high voltage (All GPIO except PP1, PP3[2], PP5[2] and PP7) I_{OH} = -1.75 mA	V_{OH}	V_{DDX} – 0.8	—	—	V
9	Output low voltage (All GPIO except PP1, PP3[2], PP5[2] and PP7) I_{OL} = +1.75 mA	V_{OL}	—	—	0.8	V
I/O Characteristics PP1, also valid for PP3 and PP5 if VSSX2 is available						
10	Output high voltage Partial Drive I_{OH} = –0.8mA Full Drive IOH = –9 mA[3]	V_{OH}	V_{DDX} – 0.8	—	—	V
11	Output low voltage, Partial drive I_{OL} = +0.8 mA Full drive I_{OL} = +9 mA[3]	V_{OL}	—	—	0.8 0.4	V
12	Maximum allowed continuous current	I_{PP}	-10	—	+25	mA
13	Over-current Detect Threshold	I_{OCD}	25	—	85	mA
I/O Characteristics PP7						
14	Output high voltage Partial Drive I_{OH} = –0.8 mA Full Drive I_{OH} = –9 mA[3]	V_{OH}	V_{DDX} – 0.8 V_{DDX} – 0.4	—	—	V
15	Output low voltage Partial Drive I_{OL} = +1.75 mA Full Drive I_{OL} = +9 mA[3]	V_{OL}	—	—	0.8	V
16	Maximum allowed continuous current	I_{PP}	-20	—	10	mA
17	Over-current Detect Threshold	I_{OCD}	-85	—	-25	mA

G.1 Static Electrical Characteristics

Table G-1. Static Electrical Characteristics - dac_8b5v_analog_ll18 @5V VDDA

Characteristics noted under conditions 4.85V ≤ V_{DDA} ≤ 5.15V, -40°C ≤ T_J ≤ 175°C, V_{RH} = V_{DDA}, V_{RL} = V_{SSA} unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Num	Ratings	Symbol	Min	Typ	Max	Unit
1	Supply Current of dac_8b5v_analog_ll18 buffer disabled buffer enabled FVR=0 DRIVE=1 buffer enabled FVR=1 DRIVE=0	I_{buf}	- - -	- 365 215	5 800 800	µA
2	Reference current reference disabled reference enabled	I_{ref}	-	- 50	1 150	µA
3	Resolution		8			bit
4	Relative Accuracy measured at AMP -40°C < T_J ≤ 150°C 150°C < T_J < 175°C	INL	-0.5 -0.75		+0.5 +0.75	LSB
5	Differential Nonlinearity measure at AMP -40°C < T_J ≤ 150°C 150°C < T_J < 175°C	DNL	-0.5 -0.75		+0.5 +0.75	LSB
6	DAC Range A (FVR bit = 1)	V_{out}	0...255/256(V_{RH}-V_{RL})+V_{RL}			V
7	DAC Range B (FVR bit = 0	V_{out}	32...287/320(V_{RH}-V_{RL})+V_{RL}			V
8	Output Voltage unbuffered range A or B (load >= 50MΩ)	V_{out}	full DAC Range A or B			V
9	Output Voltage (DRIVE bit = 0) *) buffered range A (load >= 100KΩ to VSSA) or buffered range A (load >= 100KΩ to VDDA) buffered range B (load >= 100KΩ to VSSA) buffered range B (load >= 100KΩ to VDDA)	V_{out}	0 0.15 full DAC Range B	- -	V_{DDA}-0.15 V_{DDA}	V
10	Output Voltage (DRIVE bit = 1) **) buffered range B with 6.4KΩ load into resistor divider of 800Ω /6.56KΩ between VDDA and VSSA. (equivalent load is >= 65KΩ to VSSA) or (equivalent load is >= 7.5KΩ to VDDA)	V_{out}	full DAC Range B			V
11	Buffer Output Capacitive load	C_{load}	0	-	100	pF
12	Buffer Output Offset	V_{offset}	-30	-	+30	mV
13	Settling time	t_{delay}	-	3	5	µs
14	Reverence voltage high	V_{refh}	V_{DDA}-0.1V	V_{DDA}	V_{DDA}+0.1V	V

*) DRIVE bit = 1 is not recomended in this case.

I.3 Dynamic Electrical Characteristics

Table I-3. Dynamic Electrical Characteristics of the analog comparator - ACMP

Characteristics noted under conditions $3.20V \le V_{DDA} \le 5.15V$, $-40°C \le T_J \le 175°C$[1] unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25°C$[2] under nominal conditions unless otherwise noted.						
Num	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	Output uncertain time after module enable	$t_{ACMP\_dly\_en}$	-	1	2	µs
2	ACMP Propagation Delay of Inputs ACMP0 and ACMP1 for $-2*V_{hyst(typ)}$ to $+2*V_{hyst(typ)}$ input step (w/o synchronize delay) • ACDLY=0 Low speed mode • ACDLY=1 High speed mode ACMPP is crossing ACMPN in positive direction	t_{ACMP_delay}	130 20	300 70	750 400	ns ns
3	ACMP Propagation Delay of Inputs ACMP0 and ACMP1 for $-2*V_{hyst(typ)}$ to $+2*V_{hyst(typ)}$ input step (w/o synchronize delay) $150°C \le T_J \le 175°C$ • ACDLY=0 Low speed mode • ACDLY=1 High speed mode ACMPP is crossing ACMPN in positive direction	t_{ACMP_delay}	- -	- -	800 450	ns ns

1 T_J: Junction Temperature

2 T_A: Ambient Temperature

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0830-0x083F	CANTXFG	R W	See Section 13.3.3, “Programmer’s Model of Message Storage”							

O.22 0x0980-0x0987 LINPHY0

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0980	LP0DR	R	0	0	0	0	0	0	LPDR1	LPDR0
		W								
0x0981	LP0CR	R	0	0	0	0	LPE	RXONLY	LPWUE	LPPUE
		W								
0x0982	Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		W								
0x0983	LPSLRM	R	LPDTDIS	0	0	0	0	0	LPSLR1	LPSLR0
		W								
0x0984	Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		W								
0x0985	LP0SR	R	LPDT	0	0	0	0	0	0	0
		W								
0x0986	LP0IE	R	LPDTIE	LPOCIE	0	0	0	0	0	0
		W								
0x0987	LP0IF	R	LPDTIF	LPOCIF	0	0	0	0	0	0
		W								

O.23 0x0B40-0x0B47 PGA

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0B40	PGAEN	R	0	0	0	0	0		PGAOFFSCEN	PGAEN
		W								
0x0B41	PGACNTL	R	0	0	PGAREFSEL[1:0]		0	0	PGAINSEL[1:0]	
		W								
0x0B42	PGAGAIN	R	0	0	0	0	PGAGAIN[3:0]			
		W								
0x0B43	PGAOFFSET	R	0		PGAOFFSET[5:0]					
		W								
0x0B44-0xB46	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0B47	Reserved	R	0	0	0	0	0	Reserved	Reserved	Reserved
		W								