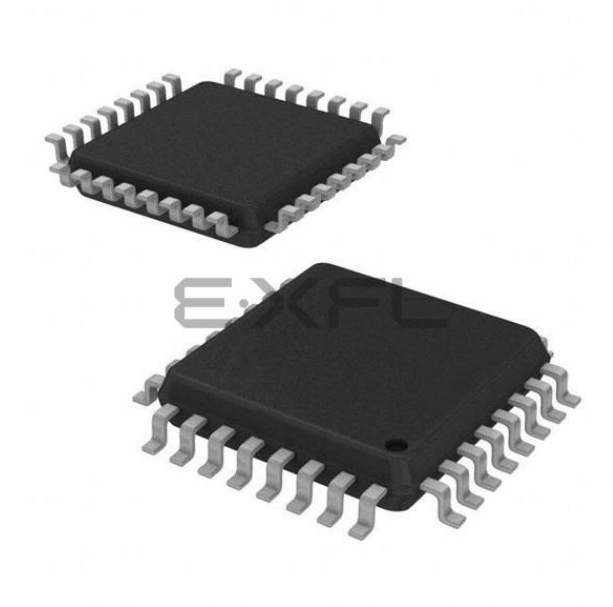

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Details	
Product Status	Active
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Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SCI, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	19
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	5.5V ~ 18V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12zvl32f0mlc

1.7.2.7 PJ[1:0] — Port P I/O Signals

PJ[1:0] are general-purpose input or output signals. They can have a pull-up or pull-down device selected and enabled on per signal basis. During and out of reset the pull devices are enabled.

1.7.2.8 PP[7:0] / KWP[7:0] — Port P I/O Signals

PP[7:0] are general-purpose input or output signals. The signals can be configured on per signal basis as interrupt inputs with wake-up capability (KWP[7:0]). They can have a pull-up or pull-down device selected and enabled on per signal basis. During and out of reset the pull devices are disabled.

1.7.2.9 PS[3:0] / KWS[3:0] — Port S I/O Signals

PS[3:0] are general-purpose input or output signals. The signals can be configured on per signal basis as interrupt inputs with wake-up capability (KWS[3:0]). They can have a pull-up or pull-down device selected and enabled on per signal basis. During and out of reset the pull-up devices are enabled.

1.7.2.10 PT[7:0] — Port T I/O Signals

PT[7:0] are general-purpose input or output signals. They can have a pull-up or pull-down device selected and enabled on per signal basis. During and out of reset the pull devices are disabled.

1.7.2.11 AN0[9:0] — ADC Input Signals

These are the analog inputs of the Analog-to-Digital Converters. ADC has 10 analog input channels connected to PAD port pins.

1.7.2.12 ACMP Signals

1.7.2.12.1 ACMP_0 / ACMP_1 — Analog Comparator Inputs

ACMP_0 and ACMP_1 are the inputs of the analog comparator ACMP.

1.7.2.12.2 ACMPO — Analog Comparator Output

ACMPO is the outputs of the analog comparators.

1.7.2.13 DAC Signals

1.7.2.13.1 AMP Output Pin

This analog pin is used for the buffered analog output voltage from the operational amplifier outputs, when the according mode is selected in DACCTL register bits DACM[2:0].

1.7.2.13.2 AMPP Input Pin

This analog input pin is used as input signal for the operational amplifier positive input pins when the according mode is selected in DACCTL register bits DACM[2:0].

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0070	MODE	R	MODC	0	0	0	0	0	0	0
		W								
0x0071-0x007F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0080	MMCECH	R	ITR[3:0]				TGT[3:0]			
		W								
0x0081	MMCECL	R	ACC[3:0]				ERR[3:0]			
		W								
0x0082	MMCCCRH	R	CPUU	0	0	0	0	0	0	0
		W								
0x0083	MMCCCRL	R	0	CPUX	0	CPUI	0	0	0	0
		W								
0x0084	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0085	MMCPCH	R	CPUPC[23:16]							
		W								
0x0086	MMCPCM	R	CPUPC[15:8]							
		W								
0x0087	MMCPCL	R	CPUPC[7:0]							
		W								
0x0088-0x00FF	Reserved	R	0	0	0	0	0	0	0	0
		W								

= Unimplemented or Reserved

Figure 4-2. S12ZDBG Register Summary

4.3.2 Register Descriptions

This section consists of the S12ZDBG control and status register descriptions in address order.

- All illegal accesses performed by the ADC module trigger error interrupts. See ADC section for details.

NOTE

Illegal accesses caused by S12ZCPU opcode prefetches will also trigger machine exceptions, even if those opcodes might not be executed in the program flow. To avoid these machine exceptions, S12ZCPU instructions must not be executed from the last (high addresses) 8 bytes of RAM, EEPROM, and Flash.

4.4.3 Uncorrectable ECC Faults

RAM and flash use error correction codes (ECC) to detect and correct memory corruption. Each uncorrectable memory corruption, which is detected during a S12ZCPU or ADC access triggers a machine exception. Uncorrectable memory corruptions which are detected during a S12ZBDC access, are captured in the RAMWF or the RDINV bit of the BDCCSRL register.

9.3.2.11 S12CPMU_UHV RTI Control Register (CPMURTI)

This register selects the time-out period for the Real Time Interrupt.

The clock source for the RTI is either IRCCLK or OSCCLK depending on the setting of the RTIOSCSEL bit. In Stop Mode with PSTP=1 (Pseudo Stop Mode) and RTIOSCSEL=1 the RTI continues to run, else the RTI counter halts in Stop Mode.

Module Base + 0x000B

	7	6	5	4	3	2	1	0
R W	RTDEC	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
Reset	0	0	0	0	0	0	0	0

Figure 9-14. S12CPMU_UHV RTI Control Register (CPMURTI)

Read: Anytime

Write: Anytime

NOTE

A write to this register starts the RTI time-out period. A change of the RTIOSCSEL bit (writing a different value or loosing UPOSC status) re-starts the RTI time-out period.

Table 9-11. CPMURTI Field Descriptions

Field	Description
7 RTDEC	**Decimal or Binary Divider Select Bit** — RTDEC selects decimal or binary based prescaler values. 0 Binary based divider value. See Table 9-12 1 Decimal based divider value. See Table 9-13
6–4 RTR[6:4]	**Real Time Interrupt Prescale Rate Select Bits** — These bits select the prescale rate for the RTI.See Table 9-12 and Table 9-13.
3–0 RTR[3:0]	**Real Time Interrupt Modulus Counter Select Bits** — These bits select the modulus counter target value to provide additional granularity.Table 9-12 and Table 9-13 show all possible divide values selectable by the CPMURTI register.

10.5.2.8 ADC Interrupt Enable Register (ADCIE)

Module Base + 0x0007

	7	6	5	4	3	2	1	0
R	SEQAD_IE	CONIF_OIE	Reserved	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 10-11. ADC Interrupt Enable Register (ADCIE)

Read: Anytime

Write: Anytime

Table 10-13. ADCIE Field Descriptions

Field	Description
7 SEQAD_IE	**Conversion Sequence Abort Done Interrupt Enable Bit** — This bit enables the conversion sequence abort event done interrupt. 0 Conversion sequence abort event done interrupt disabled. 1 Conversion sequence abort event done interrupt enabled.
6 CONIF_OIE	**ADCCONIF Register Flags Overrun Interrupt Enable** — This bit enables the flag which indicates if an overrun situation occurred for one of the CON_IF[15:1] flags or for the EOL_IF flag. 0 No ADCCONIF Register Flag overrun occurred. 1 ADCCONIF Register Flag overrun occurred.

– *Function:*
Start the first conversion of a conversion sequence which is defined in the active Command Sequence List

– *Requested by:*
- Positive edge of internal interface signal Trigger
- Write Access via data bus to set control bit TRIG

– *When finished:*
This bit is cleared by the ADC when the first conversion of the sequence is beginning to sample

– *Mandatory Requirements:*
- In all ADC conversion flow control modes bit TRIG is only set (Trigger Event executed) if the Trigger Event occurs while no conversion or conversion sequence is ongoing (ADC idle)
- In ADC conversion flow control mode “Restart Mode” with a Restart Event in progress it is not allowed that a Trigger Event occurs before the background command load phase has finished (Restart Event has been executed) else the error flag TRIG_EIF is set
- In ADC conversion flow control mode “Trigger Mode” a Restart Event causes bit TRIG being set automatically. Bit TRIG is set when no conversion or conversion sequence is ongoing (ADC idle) and the RVL done condition is reached by one of the following:
* A “End Of List” command type has been executed
* A Sequence Abort Event is in progress or has been executed
The ADC executes the Restart Event followed by the Trigger Event.
- In ADC conversion flow control mode “Trigger Mode” a Restart Event and a simultaneous Trigger Event via internal interface or data bus causes the TRIG_EIF bit being set and ADC cease operation.

• **Restart Event** (with current active CSL)
Internal Interface Signal: Restart
Corresponding Bit Name: RSTA

– *Function:*
- Go to top of active CSL (clear index register for CSL)
- Load one background command register and wait for Trigger (CSL offset register is not switched independent of bit CSL_BMOD)
- Set error flag RSTA_EIF when a Restart Request occurs before one of the following conditions was reached:
* The "End Of List" command type has been executed
* Depending on bit STR_SEQA if the "End Of List" command type is about to be executed
* The current CSL has been aborted or is about to be aborted due to a Sequence Abort Request.

– *Requested by:*
- Positive edge of internal interface signal Restart
- Write Access via data bus to set control bit RSTA

10.9.3 List Usage — CSL double buffer mode and RVL double buffer mode

In this use case both list types are configured for double buffer mode (CSL_BMOD=1’b1 and RVL_BMOD=1’b1) and whenever a Command Sequence List (CSL) is finished or aborted the command Sequence List is swapped by the simultaneous assertion of bits LDOK and RSTA.

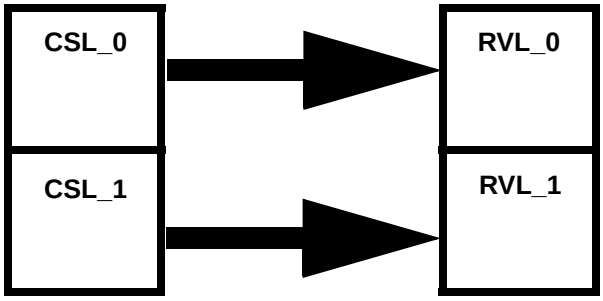


Figure 10-37. CSL Double Buffer Mode — RVL Double Buffer Mode Diagram

This use case can be used if the channel order or CSL length varies very frequently in an application.

10.9.4 List Usage — CSL double buffer mode and RVL single buffer mode

In this use case the CSL is configured for double buffer mode (CSL_BMOD=1’b1) and the RVL is configured for single buffer mode (RVL_BMOD=1’b0).

The two command lists can be different sizes and the allocated result list memory area in the RAM must be able to hold as many entries as the larger of the two command lists. Each time when the end of a Command Sequence List is reached, if bits LDOK and RSTA are set, the commands list is swapped.

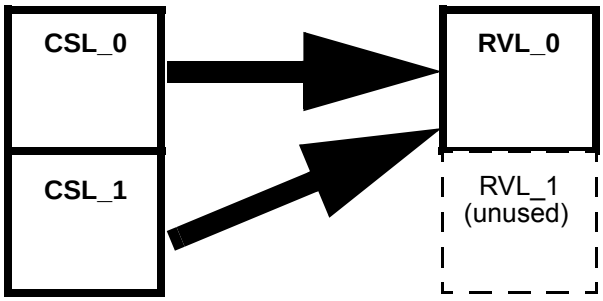


Figure 10-38. CSL Double Buffer Mode — RVL Single Buffer Mode Diagram

11.4.2.1 Control Register (DACCTL)

Module Base + 0x0000 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	FVR	DRIVE	0	0	0	DACM[2:0]		
W								
Reset	1	0	0	0	0	0	0	0

= Unimplemented

Figure 11-3. Control Register (DACCTL)

[1] Read: Anytime
Write: Anytime

Table 11-3. DACCTL Field Description

Field	Description
7 FVR	**Full Voltage Range** — This bit defines the voltage range of the DAC. 0 DAC resistor network operates with the reduced voltage range 1 DAC resistor network operates with the full voltage range **Note:** For more details see Section 11.5.8, “Analog output voltage calculation”.
6 DRIVE	**Drive Select** — This bit selects the output drive capability of the operational amplifier, see electrical Spec. for more details. 0 Low output drive for high resistive loads 1 High output drive for low resistive loads
2:0 DACM[2:0]	**Mode Select** — These bits define the mode of the DAC. A write access with an unsupported mode will be ignored. 000 Off 001 Operational Amplifier 010 Internal DAC only 100 Unbuffered DAC 101 Unbuffered DAC with Operational Amplifier 111 Buffered DAC other Reserved

software simpler because only one address area is applicable for the transmit process, and the required address space is minimized.

The CPU then stores the identifier, the control bits, and the data content into one of the transmit buffers. Finally, the buffer is flagged as ready for transmission by clearing the associated TXE flag.

The MSCAN then schedules the message for transmission and signals the successful transmission of the buffer by setting the associated TXE flag. A transmit interrupt (see Section 13.4.7.2, “Transmit Interrupt”) is generated[1] when TXEx is set and can be used to drive the application software to re-load the buffer.

If more than one buffer is scheduled for transmission when the CAN bus becomes available for arbitration, the MSCAN uses the local priority setting of the three buffers to determine the prioritization. For this purpose, every transmit buffer has an 8-bit local priority field (PRIO). The application software programs this field when the message is set up. The local priority reflects the priority of this particular message relative to the set of messages being transmitted from this node. The lowest binary value of the PRIO field is defined to be the highest priority. The internal scheduling process takes place whenever the MSCAN arbitrates for the CAN bus. This is also the case after the occurrence of a transmission error.

When a high priority message is scheduled by the application software, it may become necessary to abort a lower priority message in one of the three transmit buffers. Because messages that are already in transmission cannot be aborted, the user must request the abort by setting the corresponding abort request bit (ABTRQ) (see Section 13.3.2.9, “MSCAN Transmitter Message Abort Request Register (CANTARQ)”.) The MSCAN then grants the request, if possible, by:

1. Setting the corresponding abort acknowledge flag (ABTAK) in the CANTAAK register.
2. Setting the associated TXE flag to release the buffer.
3. Generating a transmit interrupt. The transmit interrupt handler software can determine from the setting of the ABTAK flag whether the message was aborted (ABTAK = 1) or sent (ABTAK = 0).

13.4.2.3 Receive Structures

The received messages are stored in a five stage input FIFO. The five message buffers are alternately mapped into a single memory area (see Figure 13-38). The background receive buffer (RxBG) is exclusively associated with the MSCAN, but the foreground receive buffer (RxFG) is addressable by the CPU (see Figure 13-38). This scheme simplifies the handler software because only one address area is applicable for the receive process.

All receive buffers have a size of 15 bytes to store the CAN control bits, the identifier (standard or extended), the data contents, and a time stamp, if enabled (see Section 13.3.3, “Programmer’s Model of Message Storage”).

The receiver full flag (RXF) (see Section 13.3.2.5, “MSCAN Receiver Flag Register (CANRFLG)”) signals the status of the foreground receive buffer. When the buffer contains a correctly received message with a matching identifier, this flag is set.

On reception, each message is checked to see whether it passes the filter (see Section 13.4.3, “Identifier Acceptance Filter”) and simultaneously is written into the active RxBG. After successful reception of a valid message, the MSCAN shifts the content of RxBG into the receiver FIFO, sets the RXF flag, and

1. The transmit interrupt occurs only if not masked. A polling scheme can be applied on TXEx also.

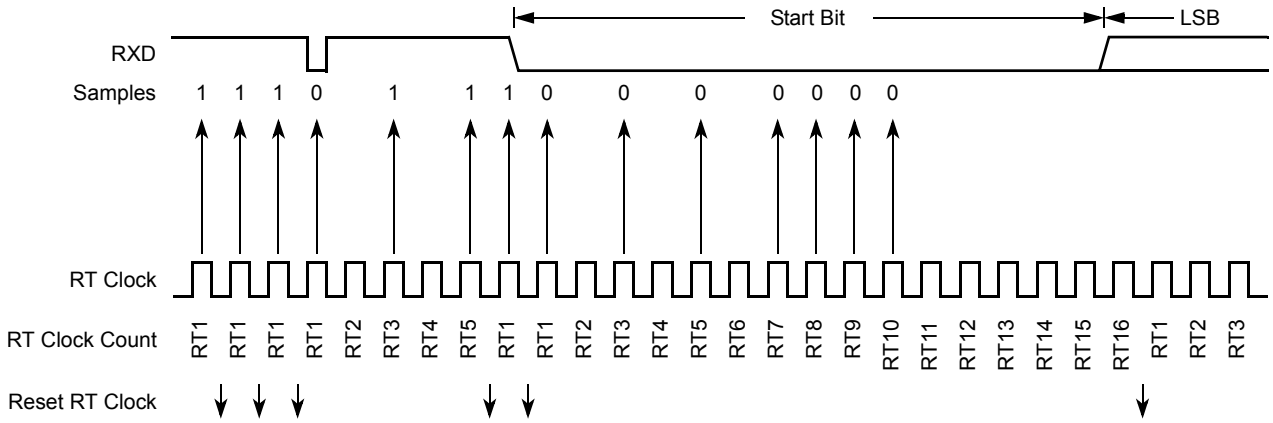


Figure 18-22. Start Bit Search Example 1

In Figure 18-23, verification sample at RT3 is high. The RT3 sample sets the noise flag. Although the perceived bit time is misaligned, the data samples RT8, RT9, and RT10 are within the bit time and data recovery is successful.

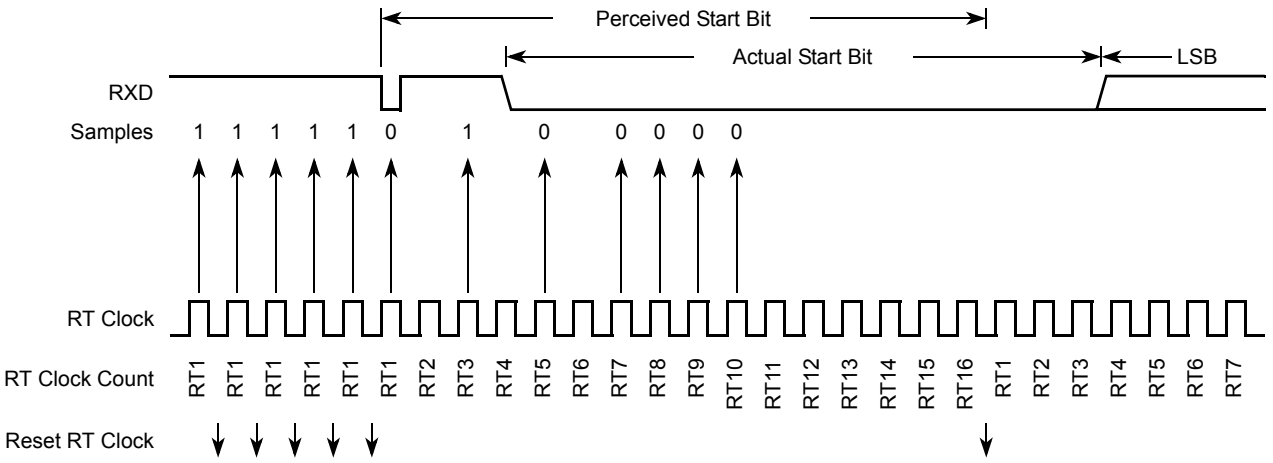


Figure 18-23. Start Bit Search Example 2

In Figure 18-24, a large burst of noise is perceived as the beginning of a start bit, although the test sample at RT5 is high. The RT5 sample sets the noise flag. Although this is a worst-case misalignment of perceived bit time, the data samples RT8, RT9, and RT10 are within the bit time and data recovery is successful.

Table 19-4. SPICR2 Field Descriptions

Field	Description
6 XFRW	**Transfer Width —** This bit is used for selecting the data transfer width. If 8-bit transfer width is selected, SPIDRL becomes the dedicated data register and SPIDRH is unused. If 16-bit transfer width is selected, SPIDRH and SPIDRL form a 16-bit data register. Please refer to Section 19.3.2.4, “SPI Status Register (SPISR) for information about transmit/receive data handling and the interrupt flag clearing mechanism. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. 0 8-bit Transfer Width (n = 8)[1] 1 16-bit Transfer Width (n = 16)[1]
4 MODFEN	**Mode Fault Enable Bit** — This bit allows the MODF failure to be detected. If the SPI is in master mode and MODFEN is cleared, then the $\overline{SS}$ port pin is not used by the SPI. In slave mode, the $\overline{SS}$ is available only as an input regardless of the value of MODFEN. For an overview on the impact of the MODFEN bit on the $\overline{SS}$ port pin configuration, refer to Table 19-3. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. 0 $\overline{SS}$ port pin is not used by the SPI. 1 $\overline{SS}$ port pin with MODF feature.
3 BIDIROE	**Output Enable in the Bidirectional Mode of Operation** — This bit controls the MOSI and MISO output buffer of the SPI, when in bidirectional mode of operation (SPC0 is set). In master mode, this bit controls the output buffer of the MOSI port, in slave mode it controls the output buffer of the MISO port. In master mode, with SPC0 set, a change of this bit will abort a transmission in progress and force the SPI into idle state. 0 Output buffer disabled. 1 Output buffer enabled.
1 SPISWAI	**SPI Stop in Wait Mode Bit** — This bit is used for power conservation while in wait mode. 0 SPI clock operates normally in wait mode. 1 Stop SPI clock generation when in wait mode.
0 SPC0	**Serial Pin Control Bit 0** — This bit enables bidirectional pin configurations as shown in Table 19-5. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state.

[1] n is used later in this document as a placeholder for the selected transfer width.

Table 19-5. Bidirectional Pin Configurations

Pin Mode	SPC0	BIDIROE	MISO	MOSI
Master Mode of Operation				
Normal	0	X	Master In	Master Out
Bidirectional	1	0	MISO not used by SPI	Master In
		1		Master I/O
Slave Mode of Operation				
Normal	0	X	Slave Out	Slave In
Bidirectional	1	0	Slave In	MOSI not used by SPI
		1	Slave I/O	

The main element of the SPI system is the SPI data register. The n-bit[1] data register in the master and the n-bit[1] data register in the slave are linked by the MOSI and MISO pins to form a distributed 2n-bit[1] register. When a data transfer operation is performed, this 2n-bit[1] register is serially shifted n[1] bit positions by the S-clock from the master, so data is exchanged between the master and the slave. Data written to the master SPI data register becomes the output data for the slave, and data read from the master SPI data register after a transfer operation is the input data from the slave.

A read of SPISR with SPTEF = 1 followed by a write to SPIDR puts data into the transmit data register. When a transfer is complete and SPIF is cleared, received data is moved into the receive data register. This data register acts as the SPI receive data register for reads and as the SPI transmit data register for writes. A common SPI data register address is shared for reading data from the read data buffer and for writing data to the transmit data register.

The clock phase control bit (CPHA) and a clock polarity control bit (CPOL) in the SPI control register 1 (SPICR1) select one of four possible clock formats to be used by the SPI system. The CPOL bit simply selects a non-inverted or inverted clock. The CPHA bit is used to accommodate two fundamentally different protocols by sampling data on odd numbered SCK edges or on even numbered SCK edges (see Section 19.4.3, “Transmission Formats”).

The SPI can be configured to operate as a master or as a slave. When the MSTR bit in SPI control register1 is set, master mode is selected, when the MSTR bit is clear, slave mode is selected.

NOTE

A change of CPOL or MSTR bit while there is a received byte pending in the receive shift register will destroy the received byte and must be avoided.

19.4.1 Master Mode

The SPI operates in master mode when the MSTR bit is set. Only a master SPI module can initiate transmissions. A transmission begins by writing to the master SPI data register. If the shift register is empty, data immediately transfers to the shift register. Data begins shifting out on the MOSI pin under the control of the serial clock.

- Serial clock

  The SPR2, SPR1, and SPR0 baud rate selection bits, in conjunction with the SPPR2, SPPR1, and SPPR0 baud rate preselection bits in the SPI baud rate register, control the baud rate generator and determine the speed of the transmission. The SCK pin is the SPI clock output. Through the SCK pin, the baud rate generator of the master controls the shift register of the slave peripheral.
- MOSI, MISO pin

  In master mode, the function of the serial data output pin (MOSI) and the serial data input pin (MISO) is determined by the SPC0 and BIDIROE control bits.
- $\overline{SS}$ pin

  If MODFEN and SSOE are set, the $\overline{SS}$ pin is configured as slave select output. The $\overline{SS}$ output becomes low during each transmission and is high when the SPI is in idle state.

1. n depends on the selected transfer width, please refer to Section 19.3.2.2, “SPI Control Register 2 (SPICR2)

20.3.1.6 IIC Control Register 2(IBCR2)

Module Base + 0x0005

	7	6	5	4	3	2	1	0
R	GCEN	ADTYPE	0	0	0	ADR10	ADR9	ADR8
W								
Reset	0	0	0	0	0	0	0	0

Figure 20-9. IIC Bus Control Register 2(IBCR2)

This register contains the variables used in general call and in ten-bit address.

Read and write anytime

Table 20-10. IBCR2 Field Descriptions

Field	Description
7 GCEN	**General Call Enable**. 0 General call is disabled. The module dont receive any general call data and address. 1 enable general call. It indicates that the module can receive address and any data.
6 ADTYPE	**Address Type— This bit selects the address length. The variable must be configured correctly before IIC enters slave mode.** **0 7-bit address** **1 10-bit address**
5,4,3 RESERVED	**Reserved** — Bit 5,4 and 3 of the IBCR2 are reserved for future compatibility. These bits will always read 0.
2:0 ADR[10:8]	**Slave Address [10:8]** —These 3 bits represent the MSB of the 10-bit address when address type is asserted (ADTYPE = 1).

20.4 Functional Description

This section provides a complete functional description of the IICV3.

20.4.1 I-Bus Protocol

The IIC bus system uses a serial data line (SDA) and a serial clock line (SCL) for data transfer. All devices connected to it must have open drain or open collector outputs. Logic AND function is exercised on both lines with external pull-up resistors. The value of these resistors is system dependent.

Normally, a standard communication is composed of four parts: START signal, slave address transmission, data transfer and STOP signal. They are described briefly in the following sections and illustrated in Figure 20-10.

21.3.2.1 Port LP Data Register (LPDR)

Module Base + Address 0x0000 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	LPDR1	LPDR0
W								
Reset	0	0	0	0	0	0	1	1

= Unimplemented

Figure 21-3. Port LP Data Register (LPDR)

[1] Read: Anytime
Write: Anytime

Table 21-2. LPDR Field Description

Field	Description
1 LPDR1	Port LP Data Bit 1 — The S12LINPHYV2 LPTxD input (see Figure 21-1) can be directly controlled by this register bit. The routing of the LPTxD input is done in the Port Inetrgation Module (PIM). Please refer to the PIM chapter of the device Reference Manual for more info.
0 LPDR0	Port LP Data Bit 0 — Read-only bit. The S12LINPHYV2 LPRxD output state can be read at any time.

21.3.2.2 LIN Control Register (LPCR)

Module Base + Address 0x0001 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	LPE	RXONLY	LPWUE	LPPUE
W								
Reset	0	0	0	0	0	0	0	0

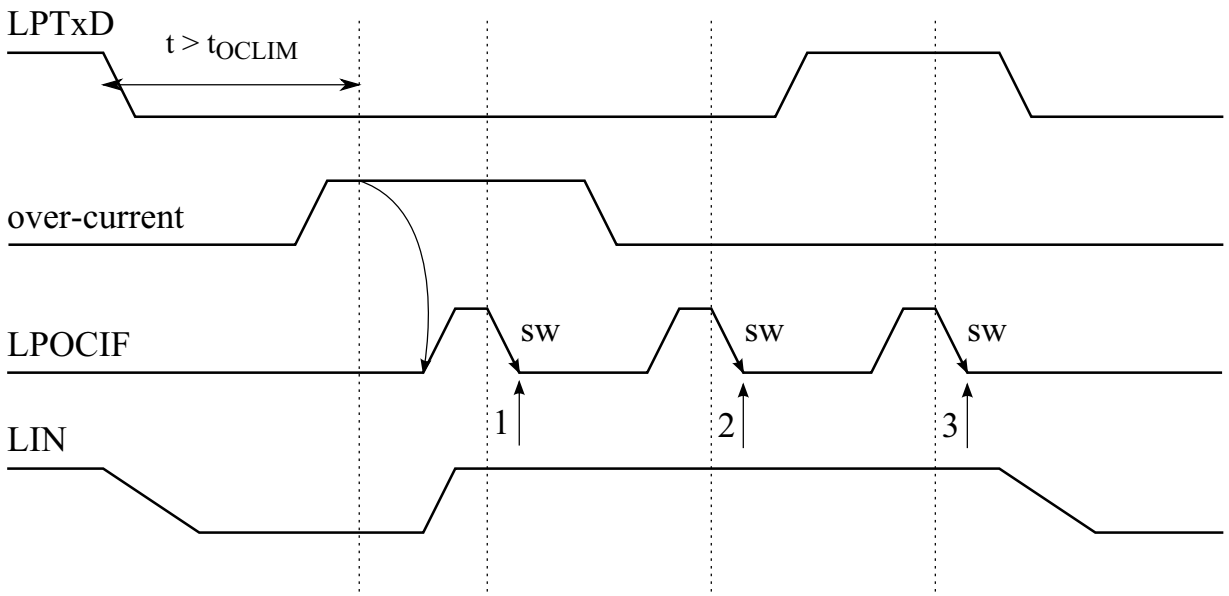
= Unimplemented

Figure 21-4. LIN Control Register (LPCR)

[1] Read: Anytime
Write: Anytime,

Table 21-3. LPCR Field Description

Field	Description
3 LPE	LIN Enable Bit — If set, this bit enables the LIN Physical Layer. 0 The LIN Physical Layer is in shutdown mode. None of the LIN Physical Layer functions are available, except that the bus line is held in its recessive state by a high ohmic (330kΩ) resistor. All registers are normally accessible. 1 The LIN Physical Layer is not in shutdown mode.
2 RXONLY	Receive Only Mode bit — This bit controls RXONLY mode. 0 The LIN Physical Layer is not in receive only mode. 1 The LIN Physical Layer is in receive only mode.



1: Flag cleared, transmitter re-enable not successful because over-current is still present
2: Flag cleared, transmitter re-enable not successful because LPTxD is dominant
3: Flag cleared, transmitter re-enable successful

Figure 21-12. Overcurrent interrupt handling

21.4.4.2 TxD-dominant timeout Interrupt

To protect the LIN bus from a network lock-up, the LIN Physical Layer implements a TxD-dominant timeout mechanism. When the LPTxD signal has been dominant for more than t_{DTLIM} the transmitter is disabled and the LPDT status flag and the LPDTIF interrupt flag are set.

In order to re-enable the transmitter again, the following prerequisites must be met:

1) TxD-dominant condition is over (LPDT=0)

2) LPTxD is recessive or the LIN Physical Layer is in shutdown or receive only mode for a minimum of a transmit bit time

To re-enable the transmitter then, the LPDTIF flag must be cleared (by writing a 1).

NOTE

Please make sure that LPDTIF=1 before trying to clear it. It is not allowed to try to clear LPDTIF if LPDTIF=0 already.

Table A-4. ESD and Latch-up Test Conditions

Model	Spec	Description	Symbol	Value	Unit
Human Body	JESD22-A114	Series Resistance	R	1500	Ω
		Storage Capacitance	C	100	pF
		Number of Pulse per pin positive negative	-	- 1 1	
Charged-Device	JESD22-C101	Series Resistance	R	0	Ω
		Storage Capacitance	C	4	pF
Latch-up for 5V GPIO's		Minimum Input Voltage Limit		-2.5	V
		Maximum Input Voltage Limit		+7.5	V
Latch-up for LIN		Minimum Input Voltage Limit		-7	V
		Maximum Input Voltage Limit		+27	V

Table A-5. ESD Protection and Latch-up Characteristics

Num	Rating	Symbol	Min	Max	Unit
1	Human Body Model (HBM): -LIN vs LGND -PL0 -all other pins	 V_{HBM} V_{HBM} V_{HBM}	 +/-6 +/-4 +/-2	-	KV
2	Charged-Device Model (CDM): Corner Pins	V_{CDM}	+/-750	-	V
3	Charged-Device Model (CDM): all other pins	V_{CDM}	+/-500	-	V
4	Direct Contact Discharge IEC61000-4-2 with and with out 220pF capacitor (R=330, C=150pF): LIN vs LGND	V_{ESDIEC}	+/-6	-	KV
5	Latch-up Current of 5V GPIO's at T=125°C positive negative	I_{LAT}	 +100 -100	-	mA
6	Latch-up Current at 27°C positive negative	I_{LAT}	 +200 -200	-	mA

A.1.5 Operating Conditions

This section describes the operating conditions of the device. Unless otherwise noted those conditions apply to all the following data.

C.1.2 ADC Accuracy

Table C-3 and Table C-2 specifies the ADC conversion performance excluding any errors due to current injection, input capacitance and source resistance.

C.1.2.1 ADC Accuracy Definitions

For the following definitions see also Figure C-2.
Differential non-linearity (DNL) is defined as the difference between two adjacent switching steps.

$$DNL(i) = \frac{V_i - V_{i-1}}{1LSB} - 1$$

The integral non-linearity (INL) is defined as the sum of all DNLs:

$$INL(n) = \sum_{i=1}^{n} DNL(i) = \frac{V_n - V_0}{1LSB} - n$$

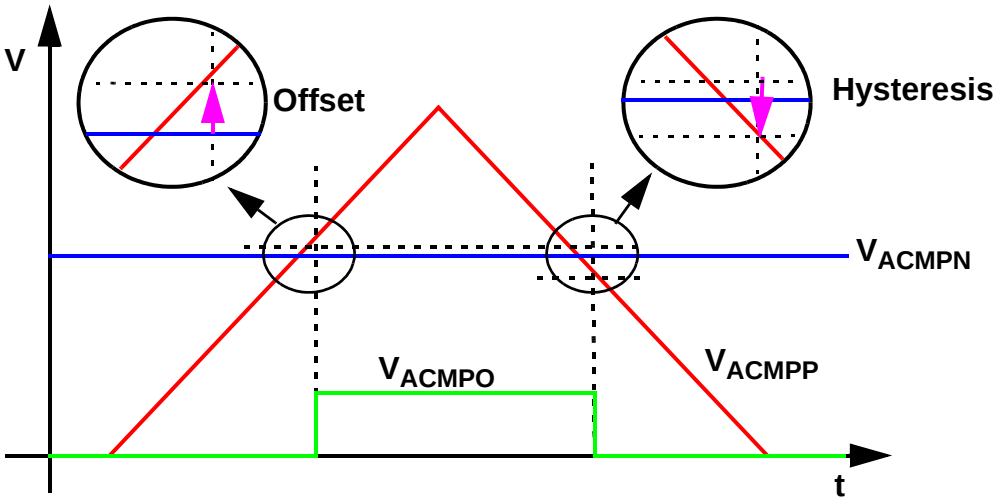
Table I-2. Static Electrical Characteristics of the analog comparator - ACMP

Characteristics noted under conditions 3.20V ≤ V_{DDA} ≤ 5.15V, -40°C ≤ T_J ≤ 175°C[1] unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C[2] under nominal conditions unless otherwise noted.						
Num	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
6	Input Hysteresis in run mode • [ACHYS] = 00 • [ACHYS] = 01 • [ACHYS] = 10 • [ACHYS] = 11	V_{ACMP_hyst}	 -3 -10 -30 -50	 -12 -24 -60 -125	 -22 -40 -100 -200	 mV mV mV mV
7	Common Mode Input range • V_{ACMP_0} • V_{ACMP_1} • V_{acmpi_0} • V_{acmpi_1}	V_{ACMP_in}	0	V_{DDA}/2	V_{DDA}	V

1 T_J: Junction Temperature

2 T_A: Ambient Temperature

Input Offset and Hysteresis



O.6 0x0380-0x039F FTMRZ (continued)

Address	Name		7	6	5	4	3	2	1	0
0x0394	FCCOB4HI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
		W								
0x0395	FCCOB4LO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
		W								
0x0396	FCCOB5HI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
		W								
0x0397	FCCOB5LO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
		W								

O.7 0x03C0-0x03CF SRAM_ECC_32D7P

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x03C0	ECCSTAT	R	0	0	0	0	0	0	0	RDY
		W								
0x03C1	ECCIE	R	0	0	0	0	0	0	0	SBEEIE
		W								
0x03C2	ECCIF	R	0	0	0	0	0	0	0	SBEEIF
		W								
0x03C3 - 0x03C6	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x03C7	ECCDPTRH	R	DPTR[23:16]							
		W								
0x03C8	ECCDPTRM	R	DPTR[15:8]							
		W								
0x03C9	ECCDPTRL	R	DPTR[7:1]							0
		W								
0x03CA - 0x03CB	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x03CC	ECCDDH	R	DDATA[15:8]							
		W								
0x03CD	ECCDDL	R	DDATA[7:0]							
		W								
0x03CE	ECCDE	R	0	0	DECC[5:0]					
		W								
0x03CF	ECCDCMD	R	ECCDRR	0	0	0	0	0	ECCDW	ECCDR
		W								