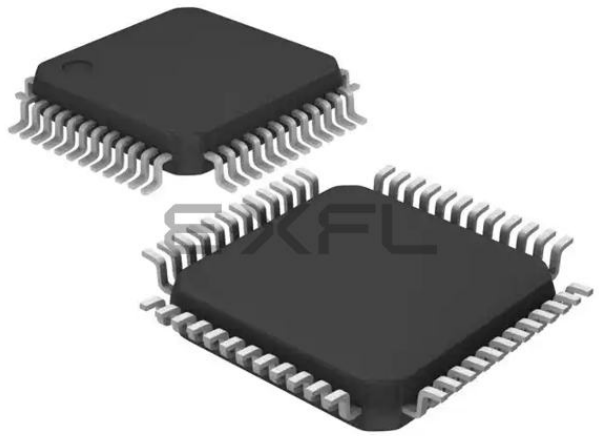

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SCI, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	5.5V ~ 18V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12zvl32f0mlfr

7.2 External Signal Description . . . 181
7.2.1 External Event Input . . . 181
7.3 Memory Map and Registers . . . 182
7.3.1 Module Memory Map . . . 182
7.3.2 Register Descriptions . . . 184
7.4 Functional Description . . . 196
7.4.1 DBG Operation . . . 196
7.4.2 Comparator Modes . . . 197
7.4.3 Events . . . 200
7.4.4 State Sequence Control . . . 202
7.4.5 Breakpoints . . . 202
7.5 Application Information . . . 204
7.5.1 Avoiding Unintended Breakpoint Re-triggering . . . 204
7.5.2 Breakpoints from other S12Z sources . . . 204

Chapter 8
ECC Generation Module (SRAM_ECCV2)

8.1 Introduction . . . 205
8.1.1 Features . . . 205
8.2 Memory Map and Register Definition . . . 206
8.2.1 Register Summary . . . 206
8.2.2 Register Descriptions . . . 208
8.3 Functional Description . . . 212
8.3.1 Aligned Memory Write Access . . . 213
8.3.2 Non-aligned Memory Write Access . . . 213
8.3.3 Memory Read Access . . . 214
8.3.4 Memory Initialization . . . 214
8.3.5 Interrupt Handling . . . 214
8.3.6 ECC Algorithm . . . 215
8.3.7 ECC Debug Behavior . . . 215

Chapter 9
S12 Clock, Reset and Power Management Unit (S12CPMU_UHV)

9.1 Introduction . . . 217
9.1.1 Features . . . 218
9.1.2 Modes of Operation . . . 220
9.1.3 S12CPMU_UHV Block Diagram . . . 224
9.2 Signal Description . . . 226
9.2.1 RESET . . . 226
9.2.2 EXTAL and XTAL . . . 226
9.2.3 VSUP — Regulator Power Input Pin . . . 226
9.2.4 VDDA, VSSA — Regulator Reference Supply Pins . . . 226
9.2.5 VDDX, VSSX — Pad Supply Pins . . . 226
9.2.6 BCTL — Base Control Pin for external PNP . . . 227

5.1.1 Glossary

Table 5-2. Glossary Of Terms

Term	Definition
DBG	On chip Debug Module
BDM	Active Background Debug Mode
CPU	S12Z CPU
SSC	Special Single Chip Mode (device operating mode
NSC	Normal Single Chip Mode (device operating mode)
BDCSI	Background Debug Controller Serial Interface. This refers to the single pin BKGD serial interface.
EWAIT	Optional S12 feature which allows external devices to delay external accesses until deassertion of EWAIT

5.1.2 Features

The BDC includes these distinctive features:

- Single-wire communication with host development system
- SYNC command to determine communication rate
- Genuine non-intrusive handshake protocol
- Enhanced handshake protocol for error detection and stop mode recognition
- Active out of reset in special single chip mode
- Most commands not requiring active BDM, for minimal CPU intervention
- Full global memory map access without paging
- Simple flash mass erase capability

5.1.3 Modes of Operation

S12 devices feature power modes (run, wait, and stop) and operating modes (normal single chip, special single chip). Furthermore, the operation of the BDC is dependent on the device security status.

5.1.3.1 BDC Modes

The BDC features module specific modes, namely disabled, enabled and active. These modes are dependent on the device security and operating mode. In active BDM the CPU ceases execution, to allow BDC system access to all internal resources including CPU internal registers.

5.1.3.2 Security and Operating mode Dependency

In device run mode the BDC dependency is as follows

- Normal modes, unsecure device

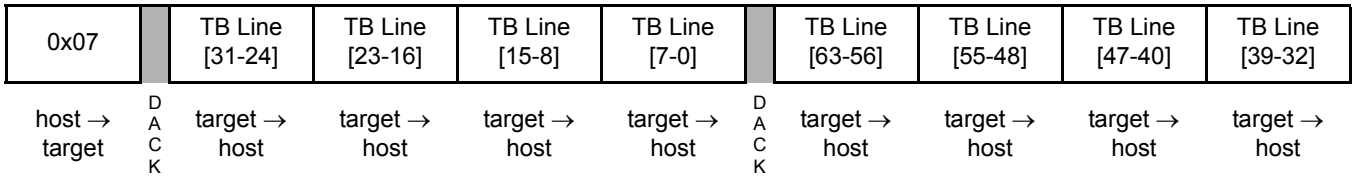
  General BDC operation available. The BDC is disabled out of reset.

returned before the read data. This status byte reflects the state after the memory read was performed. If enabled, an ACK pulse is driven before the data bytes are transmitted.

The examples show the READ_MEM.B{_WS}, READ_MEM.W{_WS} and READ_MEM.L{_WS} commands.

5.4.4.12 READ_DBGTB

Read DBG trace buffer **Non-intrusive**



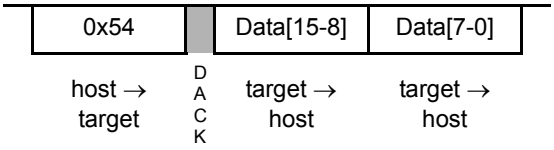
This command is only available on devices, where the DBG module includes a trace buffer. Attempted use of this command on devices without a traace buffer return 0x00.

Read 64 bits from the DBG trace buffer. Refer to the DBG module description for more detailed information. If enabled an ACK pulse is generated before each 32-bit longword is ready to be read by the host. After issuing the first ACK a timeout is still possible whilst accessing the second 32-bit longword, since this requires separate internal accesses. The first 32-bit longword corresponds to trace buffer line bits[31:0]; the second to trace buffer line bits[63:32]. If ACK handshaking is disabled, the host must wait 16 clock cycles (DLY) after completing the first 32-bit read before starting the second 32-bit read.

5.4.4.13 READ_SAME.sz, READ_SAME.sz_WS

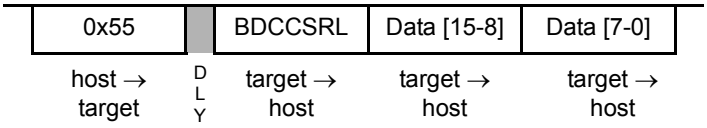
READ_SAME

Read same location specified by previous READ_MEM{_WS} **Non-intrusive**



READ_SAME_WS

Read same location specified by previous READ_MEM{_WS} **Non-intrusive**



9.3 Memory Map and Registers

This section provides a detailed description of all registers accessible in the S12CPMU_UHV.

9.3.1 Module Memory Map

The S12CPMU_UHV registers are shown in Figure 9-3.

Address Offset	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000	RESERVED	R	0	0	0	0	0	0	0	0
		W								
0x0001	RESERVED CPMU VREGTRIM0	R	0	0	0	0	U	U	U	U
		W								
0x0002	RESERVED CPMU VREGTRIM1	R	0	0	U	U	U	U	U	U
		W								
0x0003	CPMURFLG	R	0	PORF	LVRF	0	COPRF	0	OMRF	PMRF
		W								
0x0004	CPMU SYNR	R	VCOFRQ[1:0]		SYNDIV[5:0]					
		W								
0x0005	CPMU REFDIV	R	REFFRQ[1:0]		0	0	REFDIV[3:0]			
		W								
0x0006	CPMU POSTDIV	R	0	0	0	POSTDIV[4:0]				
		W								
0x0007	CPMUIFLG	R	RTIF	0	0	LOCKIF	LOCK	0	OSCIF	UPOSC
		W								
0x0008	CPMUINT	R	RTIE	0	0	LOCKIE	0	0	OSCIE	0
		W								
0x0009	CPMUCLKS	R	PLLSEL	PSTP	CSAD	COP OSCSEL1	PRE	PCE	RTI OSCSEL	COP OSCSEL0
		W								
0x000A	CPMUPLL	R	0	0	FM1	FM0	0	0	0	0
		W								
0x000B	CPMURTI	R	RTDEC	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
		W								
0x000C	CPMUCOP	R	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
		W			WRTMASK					
0x000D	RESERVED CPMUTEST0	R	0	0	0	0	0	0	0	0
		W								
			= Unimplemented or Reserved							

Figure 9-3. CPMU Register Summary

9.3.2.22 High Temperature Trimming Register (CPMUHTTR)

The CPMUHTTR register configures the trimming of the S12CPMU_UHV temperature sense.

Module Base + 0x0017

	7	6	5	4	3	2	1	0
R	HTOE	0	0	0	HTTR3	HTTR2	HTTR1	HTTR0
W								
Reset	0	0	0	0	F	F	F	F

After de-assert of System Reset a trim value is automatically loaded from the Flash memory. See Device specification for details.

= Unimplemented or Reserved

Figure 9-28. High Temperature Trimming Register (CPMUHTTR)

Read: Anytime

Write: Anytime

Table 9-25. CPMUHTTR Field Descriptions

Field	Description
7 HTOE	**High Temperature Offset Enable Bit** — If set the temperature sense offset is enabled. 0 The temperature sense offset is disabled. HTTR[3:0] bits don't care. 1 The temperature sense offset is enabled. HTTR[3:0] select the temperature offset.
3–0 HTTR[3:0]	**High Temperature Trimming Bits** — See Table 9-26 for trimming effects.

Table 9-26. Trimming Effect of HTTR

HTTR[3:0]	Temperature sensor voltage V_{HT}	Interrupt threshold temperatures T_{HTIA} and T_{HTID}
0000	lowest	highest
0001	increasing	decreasing
....		
1110		
1111	highest	lowest

11.5 Functional Description

11.5.1 Functional Overview

The DAC resistor network and the operational amplifier can be used together or stand alone. Following modes are supported:

Table 11-5. DAC Modes of Operation

DACM[2:0]		Description			
		Submodules		Output	
		DAC resistor network	Operational Amplifier	DACU	AMP
Off	000	disabled	disabled	disconnected	disconnected
Operational amplifier	001	disabled	enabled	disabled	depend on AMPP and AMPM input
Internal DAC only	010	enabled	disabled	disconnected	disconnected
Unbuffered DAC	100	enabled	disabled	unbuffered resistor output voltage	disconnected
Unbuffered DAC with Operational amplifier	101	enabled	enabled	unbuffered resistor output voltage	depend on AMPP and AMPM input
Buffered DAC	111	enabled	enabled	disconnected	buffered resistor output voltage

The DAC resistor network itself can work on two different voltage ranges:

Table 11-6. DAC Resistor Network Voltage ranges

DAC Mode	Description
Full Voltage Range (FVR)	DAC resistor network provides a output voltage over the complete input voltage range, default after reset
Reduced Voltage Range	DAC resistor network provides a output voltage over a reduced input voltage range

Table 11-7 shows the control signal decoding for each mode. For more detailed mode description see the sections below.

Table 11-7. DAC Control Signals

DACM		DAC resistor network	Operational Amplifier	Switch S1	Switch S2	Switch S3
Off	000	disabled	disabled	open	open	open
Operational amplifier	001	disabled	enabled	closed	open	open
Internal DAC only	010	enabled	disabled	open	open	open
Unbuffered DAC	100	enabled	disabled	open	open	closed

12.3.2.2 PGA Control Register (PGACNTL)

Module Base + 0x0001 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	PGAREFSEL[1:0]		0	0	PGAINSEL[1:0]	
W								
Reset	0	0	0	0	0	0	0	0

Figure 12-4. PGA Control Register (PGACNTL)

1 Read: Anytime
Write: Anytime

Table 12-4. PGACNTL Field Description

Field	Description
5:4 PGAREFSEL[1:0]	**PGA reference voltage selection** — If PGAEN=1 these register bits select the source for the reference voltage (PGAREF, minus input of both amplifier stages). 00 Internally generated V_{DDA} / 2 is selected as reference voltage (PGAREF) 01 Reserved 10 External PGA_REF0 input is selected as reference voltage (PGAREF). 11 External PGA_REF1 input is selected as reference voltage (PGAREF).
1:0 PGAINSEL[1:0]	**PGA input voltages selection** — This register bit defines the source for the plus input voltage of the amplifier. 00 no input voltage selected (PGAIN). 01 input voltage selection controlled by external modules, please see SoC level connection for more details. If the external control signals enables both inputs, then PGA_IN0 is selected. 10 PGA_IN0 is selected as input voltage (PGAIN). 11 PGA_IN1 is selected as input voltage (PGAIN).

12.3.2.3 PGA Gain Register (PGAGAIN)

Module Base + 0x0002 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0				PGAGAIN[3:0]			
W								
Reset	0	0	0	0	0	0	0	0

Figure 12-5. PGA Gain Register (PGAGAIN)

1 Read: Anytime
Write: Anytime

Table 12-5. PGAGAIN Field Description

Field	Description
3:0 PGAGAIN[3:0]	**PGA1 gain**— These register bits select the gain A_{PGA} (amplification factor) for the PGA stage, see Table 12-6., “Amplifier Gain

13.3.2.15 MSCAN Transmit Error Counter (CANTXERR)

This register reflects the status of the MSCAN transmit error counter.

Module Base + 0x000F — Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 13-18. MSCAN Transmit Error Counter (CANTXERR)

1 Read: Only when in sleep mode (SLPRQ = 1 and SLPAK = 1) or initialization mode (INITRQ = 1 and INITAK = 1)
Write: Unimplemented

NOTE

Reading this register when in any other mode other than sleep or initialization mode, may return an incorrect value. For MCUs with dual CPUs, this may result in a CPU fault condition.

13.3.2.16 MSCAN Identifier Acceptance Registers (CANIDAR0-7)

On reception, each message is written into the background receive buffer. The CPU is only signalled to read the message if it passes the criteria in the identifier acceptance and identifier mask registers (accepted); otherwise, the message is overwritten by the next message (dropped).

The acceptance registers of the MSCAN are applied on the IDR0–IDR3 registers (see Section 13.3.3.1, “Identifier Registers (IDR0–IDR3)”) of incoming messages in a bit by bit manner (see Section 13.4.3, “Identifier Acceptance Filter”).

For extended identifiers, all four acceptance and mask registers are applied. For standard identifiers, only the first two (CANIDAR0/1, CANIDMR0/1) are applied.

Module Base + 0x0010 to Module Base + 0x0013 — Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
Reset	0	0	0	0	0	0	0	0

Figure 13-19. MSCAN Identifier Acceptance Registers (First Bank) — CANIDAR0–CANIDAR3

1 Read: Anytime
Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Figure 13-23. Receive/Transmit Message Buffer — Extended Identifier Mapping

Register Name		Bit 7	6	5	4	3	2	1	Bit0
0x00X0 IDR0	R	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
	W								
0x00X1 IDR1	R	ID20	ID19	ID18	SRR (=1)	IDE (=1)	ID17	ID16	ID15
	W								
0x00X2 IDR2	R	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
	W								
0x00X3 IDR3	R	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
	W								
0x00X4 DSR0	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X5 DSR1	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X6 DSR2	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X7 DSR3	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X8 DSR4	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X9 DSR5	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00XA DSR6	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00XB DSR7	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00XC DLR	R					DLC3	DLC2	DLC1	DLC0
	W								

Module Base + 0x00X2

	7	6	5	4	3	2	1	0
R W	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
Reset:	x	x	x	x	x	x	x	x

Figure 13-27. Identifier Register 2 (IDR2) — Extended Identifier Mapping

Table 13-28. IDR2 Register Field Descriptions — Extended

Field	Description
7-0 ID[14:7]	**Extended Format Identifier —** The identifiers consist of 29 bits (ID[28:0]) for the extended format. ID28 is the most significant bit and is transmitted first on the CAN bus during the arbitration procedure. The priority of an identifier is defined to be highest for the smallest binary number.

Module Base + 0x00X3

	7	6	5	4	3	2	1	0
R W	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
Reset:	x	x	x	x	x	x	x	x

Figure 13-28. Identifier Register 3 (IDR3) — Extended Identifier Mapping

Table 13-29. IDR3 Register Field Descriptions — Extended

Field	Description
7-1 ID[6:0]	**Extended Format Identifier —** The identifiers consist of 29 bits (ID[28:0]) for the extended format. ID28 is the most significant bit and is transmitted first on the CAN bus during the arbitration procedure. The priority of an identifier is defined to be highest for the smallest binary number.
0 RTR	**Remote Transmission Request** — This flag reflects the status of the remote transmission request bit in the CAN frame. In the case of a receive buffer, it indicates the status of the received frame and supports the transmission of an answering frame in software. In the case of a transmit buffer, this flag defines the setting of the RTR bit to be sent. 0 Data frame 1 Remote frame

The comparator outputs BVLC and BVHC are forced to zero if the comparator is disabled (configuration bit BSUSE is cleared). If the software disables the comparator during a high or low Voltage condition (BVHC or BVLC active), then an additional interrupt is generated. To avoid this behavior the software must disable the interrupt generation before disabling the comparator.

The BATS interrupt vector is named in Table 14-6. Vector addresses and interrupt priorities are defined at MCU level.

The module internal interrupt sources are combined into one module interrupt signal.

Table 14-6. BATSV3 Interrupt Sources

Module Interrupt Source	Module Internal Interrupt Source	Local Enable
BATSV3 Interrupt (BATI)	BATS Voltage Low Condition Interrupt (BVLI)	BVLIE = 1
	BATS Voltage High Condition Interrupt (BVHI)	BVHIE = 1

14.4.2.1 BATS Voltage Low Condition Interrupt (BVLI)

To use the Voltage Low Interrupt the Level Sensing must be enabled (BSUSE =1).

If measured when

a) V_{LBI1} selected with BVLS[1:0] = 0x0
$V_{measure} < V_{LBI1\_A}$ (falling edge) or $V_{measure} < V_{LBI1\_D}$ (rising edge)

or when

b) V_{LBI2} selected with BVLS[1:0] = 0x1 at pin VSUP
$V_{measure} < V_{LBI2\_A}$ (falling edge) or $V_{measure} < V_{LBI2\_D}$ (rising edge)

or when

c) V_{LBI3} selected with BVLS[1:0] = 0x2
$V_{measure} < V_{LBI3\_A}$ (falling edge) or $V_{measure} < V_{LBI3\_D}$ (rising edge)

or when

d) V_{LBI4} selected with BVLS[1:0] = 0x3
$V_{measure} < V_{LBI4\_A}$ (falling edge) or $V_{measure} < V_{LBI4\_D}$ (rising edge)

then BVLC is set. BVLC status bit indicates that a low voltage at pin VSUP is present. The Low Voltage Interrupt flag (BVLIF) is set to 1 when the Voltage Low Condition (BVLC) changes state . The Interrupt flag BVLIF can only be cleared by writing a 1. If the interrupt is enabled by bit BVLIE the module requests an interrupt to MCU (BATI).

14.4.2.2 BATS Voltage High Condition Interrupt (BVHI)

To use the Voltage High Interrupt the Level Sensing must be enabled (BSUSE=1).

Write: Anytime, if AMAP = 1

Table 18-5. SCIASR1 Field Descriptions

Field	Description
7 RXEDGIF	**Receive Input Active Edge Interrupt Flag** — RXEDGIF is asserted, if an active edge (falling if RXPOL = 0, rising if RXPOL = 1) on the RXD input occurs. RXEDGIF bit is cleared by writing a “1” to it. 0 No active receive on the receive input has occurred 1 An active edge on the receive input has occurred
2 BERRV	**Bit Error Value** — BERRV reflects the state of the RXD input when the bit error detect circuitry is enabled and a mismatch to the expected value happened. The value is only meaningful, if BERRIF = 1. 0 A low input was sampled, when a high was expected 1 A high input reassembled, when a low was expected
1 BERRIF	**Bit Error Interrupt Flag** — BERRIF is asserted, when the bit error detect circuitry is enabled and if the value sampled at the RXD input does not match the transmitted value. If the BERRIE interrupt enable bit is set an interrupt will be generated. The BERRIF bit is cleared by writing a “1” to it. 0 No mismatch detected 1 A mismatch has occurred
0 BKDIF	**Break Detect Interrupt Flag** — BKDIF is asserted, if the break detect circuitry is enabled and a break signal is received. If the BKDIE interrupt enable bit is set an interrupt will be generated. The BKDIF bit is cleared by writing a “1” to it. 0 No break signal was received 1 A break signal was received

18.3.2.4 SCI Alternative Control Register 1 (SCIACR1)

Module Base + 0x0001

	7	6	5	4	3	2	1	0
R	RXEDGIE	0	0	0	0	0	BERRIE	BKDIE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 18-7. SCI Alternative Control Register 1 (SCIACR1)

Read: Anytime, if AMAP = 1

Write: Anytime, if AMAP = 1

Table 18-6. SCIACR1 Field Descriptions

Field	Description
7 RXEDGIE	**Receive Input Active Edge Interrupt Enable** — RXEDGIE enables the receive input active edge interrupt flag, RXEDGIF, to generate interrupt requests. 0 RXEDGIF interrupt requests disabled 1 RXEDGIF interrupt requests enabled

18.4.4 Baud Rate Generation

A 16-bit modulus counter in the two baud rate generator derives the baud rate for both the receiver and the transmitter. The value from 0 to 65535 written to the SBR15:SBR0 bits determines the baud rate. The value from 0 to 4095 written to the SBR15:SBR4 bits determines the baud rate clock with SBR3:SBR0 for fine adjust. The SBR bits are in the SCI baud rate registers (SCIBDH and SCIBDL) for both transmit and receive baud generator. The baud rate clock is synchronized with the bus clock and drives the receiver. The baud rate clock divided by 16 drives the transmitter. The receiver has an acquisition rate of 16 samples per bit time.

Baud rate generation is subject to one source of error:

- Integer division of the bus clock may not give the exact target frequency.

Table 18-16 lists some examples of achieving target baud rates with a bus clock frequency of 25 MHz.

When IREN = 0 then,

SCI baud rate = SCI bus clock / (SCIBR[15:0])

Table 18-16. Baud Rates (Example: Bus Clock = 25 MHz)

Bits SBR[15:0]	Receiver[1] Clock (Hz)	Transmitter[2] Clock (Hz)	Target Baud Rate	Error (%)
109	3669724.8	229,357.8	230,400	.452
217	1843318.0	115,207.4	115,200	.006
651	614439.3	38,402.5	38,400	.006
1302	307219.7	19,201.2	19,200	.006
2604	153,609.8	9600.6	9,600	.006
5208	76,804.9	4800.3	4,800	.006
10417	38,398.8	2399.9	2,400	.003
20833	19,200.3	1200.02	1,200	.00
41667	9599.9	600.0	600	.00
65535	6103.6	381.5		

1 16x faster then baud rate

2 divide 1/16 form transmit baud generator

block can support. Right after reset the Flash will be configured to run with the maximum amount of wait-states enabled; if the user application is setup to run at a slower frequency the control bits FCNFG[WSTAT] (see Section 22.3.2.5) can be configured by the user to disable the generation of wait-states, so it does not impose a performance penalty to the system if the read timing of the S12Z core is setup to be within the margins of the Flash block. For a definition of the frequency values where wait-states can be disabled please refer to the device electrical parameters.

The following sequence must be followed when the transition from a higher frequency to a lower frequency is going to happen:

- Flash resets with wait-states enabled;
- system frequency must be configured to the lower target;
- user writes to FNCNF[WSTAT] to disable wait-states;
- user reads the value of FPSTAT[WSTATACK], the new wait-state configuration will be effective when it reads as 1;
- user must re-write FCLKDIV to set a new value based on the lower frequency.

The following sequence must be followed on the contrary direction, going from a lower frequency to a higher frequency:

- user writes to FCNFG[WSTAT] to enable wait-states;
- user reads the value of FPSTAT[WSTATACK], the new wait-state configuration will be effective when it reads as 1;
- user must re-write FCLKDIV to set a new value based on the higher frequency;
- system frequency must be set to the upper target.

CAUTION

If the application is going to require the frequency setup to change, the value to be loaded on register FCLKDIV will have to be updated according to the new frequency value. In this scenario the application must take care to avoid locking the value of the FCLKDIV register: bit FDIVLCK must not be set if the value to be loaded on FDIV is going to be re-written, otherwise a reset is going to be required. Please refer to Section 22.3.2.1, “Flash Clock Divider Register (FCLKDIV) and Section 22.4.5.1, “Writing the FCLKDIV Register.

22.4.4 Internal NVM resource

IFR is an internal NVM resource readable by CPU. The IFR fields are shown in Table 22-4.

The NVM Resource Area global address map is shown in Table 22-5.

22.4.5 Flash Command Operations

Flash command operations are used to modify Flash memory contents.

The next sections describe:

22.4.8 Interrupts

The Flash module can generate an interrupt when a Flash command operation has completed or when a Flash command operation has detected an ECC fault.

Table 22-70. Flash Interrupt Sources

Interrupt Source	Interrupt Flag	Local Enable	Global (CCR) Mask
Flash Command Complete	CCIF (FSTAT register)	CCIE (FCNFG register)	I Bit
ECC Single Bit Fault on Flash Read	SFDIF (FERSTAT register)	SFDIE (FERCNFG register)	I Bit

NOTE

Vector addresses and their relative interrupt priority are determined at the MCU level.

22.4.8.1 Description of Flash Interrupt Operation

The Flash module uses the CCIF flag in combination with the CCIE interrupt enable bit to generate the Flash command interrupt request. The Flash module uses the SFDIF flag in combination with the SFDIE interrupt enable bits to generate the Flash error interrupt request. For a detailed description of the register bits involved, refer to Section 22.3.2.5, “Flash Configuration Register (FCNFG)”, Section 22.3.2.6, “Flash Error Configuration Register (FERCNFG)”, Section 22.3.2.7, “Flash Status Register (FSTAT)”, and Section 22.3.2.8, “Flash Error Status Register (FERSTAT)”.

The logic used for generating the Flash module interrupts is shown in Figure 22-31.

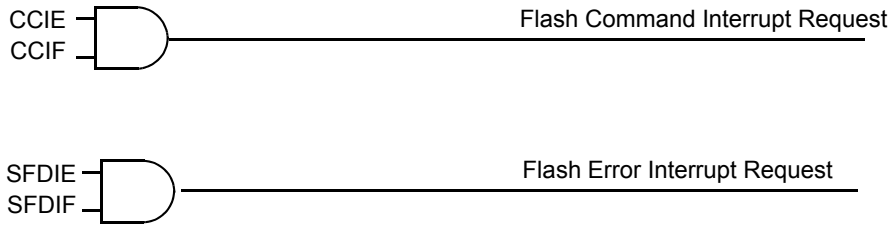


Figure 22-31. Flash Module Interrupts Implementation

22.4.9 Wait Mode

The Flash module is not affected if the MCU enters wait mode. The Flash module can recover the MCU from wait via the CCIF interrupt (see Section 22.4.8, “Interrupts”).

Table B-1. Voltage Regulator Electrical Characteristics

-40°C ≤T_J ≤ 175°C unless noted otherwise, V_{DDA} and V_{DDX} must be shorted on the application board.						
Num	**Characteristic**	**Symbol**	**Min**	**Typical**	**Max**	**Unit**
VDDX=3.3V, VREG5VEN = 1'b0, ZVL(A)128/96/64 only						
6a	Output Voltage V_{DDX}, with external PNP Full Performance Mode V_{SUP} >5.5V[1] Full Performance Mode V_{SUP} >5.5V[4] Full Performance Mode 3.5V <= V_{SUP} <=5.5V Reduced Performance Mode (stopmode) V_{SUP} > =3.5V	V_{DDX}	 3.2 3.23 3.13 2.2	 3.3 3.3 - 3.3	 3.39 3.36 3.39 3.6	V
6b	Output Voltage V_{DDX}, without PNP Full Performance Mode V_{SUP} >5.5V[1] Full Performance Mode V_{SUP} >5.5V[4] Full Performance Mode 3.5V <= V_{SUP} <=5.5V Reduced Performance Mode (stopmode) V_{SUP} > =3.5V	V_{DDX}	 3.18 3.21 3.13 2.2	 3.28 3.28 - 3.3	 3.37 3.35 3.37 3.6	V
7	Load Current V_{DDX}[2,3] without external PNP Full Performance Mode V_{SUP} > 5.5V Full Performance Mode 3.5V <= V_{SUP} <=5.5V Reduced Performance Mode (stopmode)	I_{DDX}	 0 0 0	 - - -	 70 25 5	mA
8	Short Circuit V_{DDX} fall back current V_{DDX} <= 0.5V	I_{DDX}	—	100	—	mA
9	Low Voltage Interrupt Assert Level[5] Low Voltage Interrupt Deassert Level	V_{LVIA} V_{LVID}	4.04 4.19	4.23 4.38	4.40 4.49	V
10a	V_{DDX} Low Voltage Reset deassert[6]	V_{LVRXD}	—	—	3.13	V
10b	V_{DDX} Low Voltage Reset assert	V_{LVRXA}	2.95	3.02	—	V
11	Trimmed ACLK output frequency[7]	f_{ACLK}	—	20	—	KHz
12	Trimmed ACLK internal clock Δf / $f_{nominal}$ [8]	df_{ACLK}	- 6%	—	+ 6%	—
13	The first period after enabling the counter by APIFE might be reduced by API start up delay	t_{sdel}	—	—	100	µs
14	Temperature Sensor Slope	dV_{HT}	5.05	5.25	5.45	mV/°C
15	Temperature Sensor Output Voltage (T_j=150°C)	V_{HT}	—	2.4	—	V
16	High Temperature Interrupt Assert[9] High Temperature Interrupt Deassert	T_{HTIA} T_{HTID}	120 110	132 122	144 134	°C °C
17	Bandgap output voltage	V_{BG}	1.14	1.20	1.28	V
18	V_{BG} voltage variation over input voltage V_{SUP} 3.5V ≤ V_{SUP} ≤ 18V, T_J = 125°C	Δ_{VBGV}	-5		5	mV

Appendix I
ACMP Electrical Specifications

This section describe the electrical characteristics of the analog comparator module.

I.1 Maximum Ratings

Table I-1. Maximum Ratings of the analog comparator - ACMP

Characteristics noted under conditions 3.20V ≤ V_{DDA} ≤ 5.15V, -40°C ≤ T_J ≤ 175°C[1] unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C[2] under nominal conditions unless otherwise noted.						
Num	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	Max Rating (relative to supply)	V_{ACMP_MAX}	-0.3	–	VDDA +0.3	V
	Max Rating (absolute) V_{ACMP_0} V_{ACMP_1} V_{acmpi_0} V_{acmpi_1}	V_{ACMP_MAXA}	-0.3	–	6	V

1 T_J: Junction Temperature

2 T_A: Ambient Temperature

I.2 Static Electrical Characteristics

Table I-2. Static Electrical Characteristics of the analog comparator - ACMP

Characteristics noted under conditions 3.20V ≤ V_{DDA} ≤ 5.15V, -40°C ≤ T_J ≤ 175°C[1] unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C[2] under nominal conditions unless otherwise noted.						
Num	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
2	Supply Current of ACMP T_J ≤ 150°C • Module disabled • Module enabled ΔV_{in} > 5*V_{hyst}	 I_{ACMP_off} I_{ACMP_run}	 - 80	 - -	 3 180	 µA µA
3	Supply Current of ACMP 150°C <T_J ≤ 175°C • Module disabled • Module enabled ΔV_{in} > 5*V_{hyst}	 I_{ACMP_off} I_{ACMP_run}	 - 80	 - -	 5 180	 µA µA
4	Pad Input Current in V_{ACMP_in} range • -40°C ≤ T_J ≤ 80°C • -40°C ≤ T_J ≤ 150°C • -40°C ≤ T_J ≤ 175°C For 0V < V_{pad_in} < V_{DDA}	$I_{ACMP\_pad\_in}$	 -1 -2 -3	 - - -	 1 2 3	 µA µA µA
5	Input Offset • -40°C ≤ T_J ≤ 175°C	V_{ACMP_offset}	-25	0	25	mV

[4] The structure of the HVI pins does not include diode structures shown in Figure A-1 that inject current when the input voltage goes outside the supply-ground range. Thus the HVI pin current injection is limited to below 200uA within the absolute maximum pin voltage range. However if the HVI impedance converter bypass is enabled, then even currents in this range can corrupt ADC results from simultaneous conversions on other channels. This can be prevented by disabling the bypass, either by clearing the PTAENLx or PTABYPLx bit. Similarly when the ADC is converting a HVI pin voltage then the impedance converter bypass must be disabled to ensure that current injection on PADx pins does not impact the HVI ADC conversion result.

NOTE

Not every combination is offered. Table 1-2 lists available derivatives. The mask identifier suffix and the Tape & Reel suffix are always both omitted from the partnumber which is actually marked on the device.

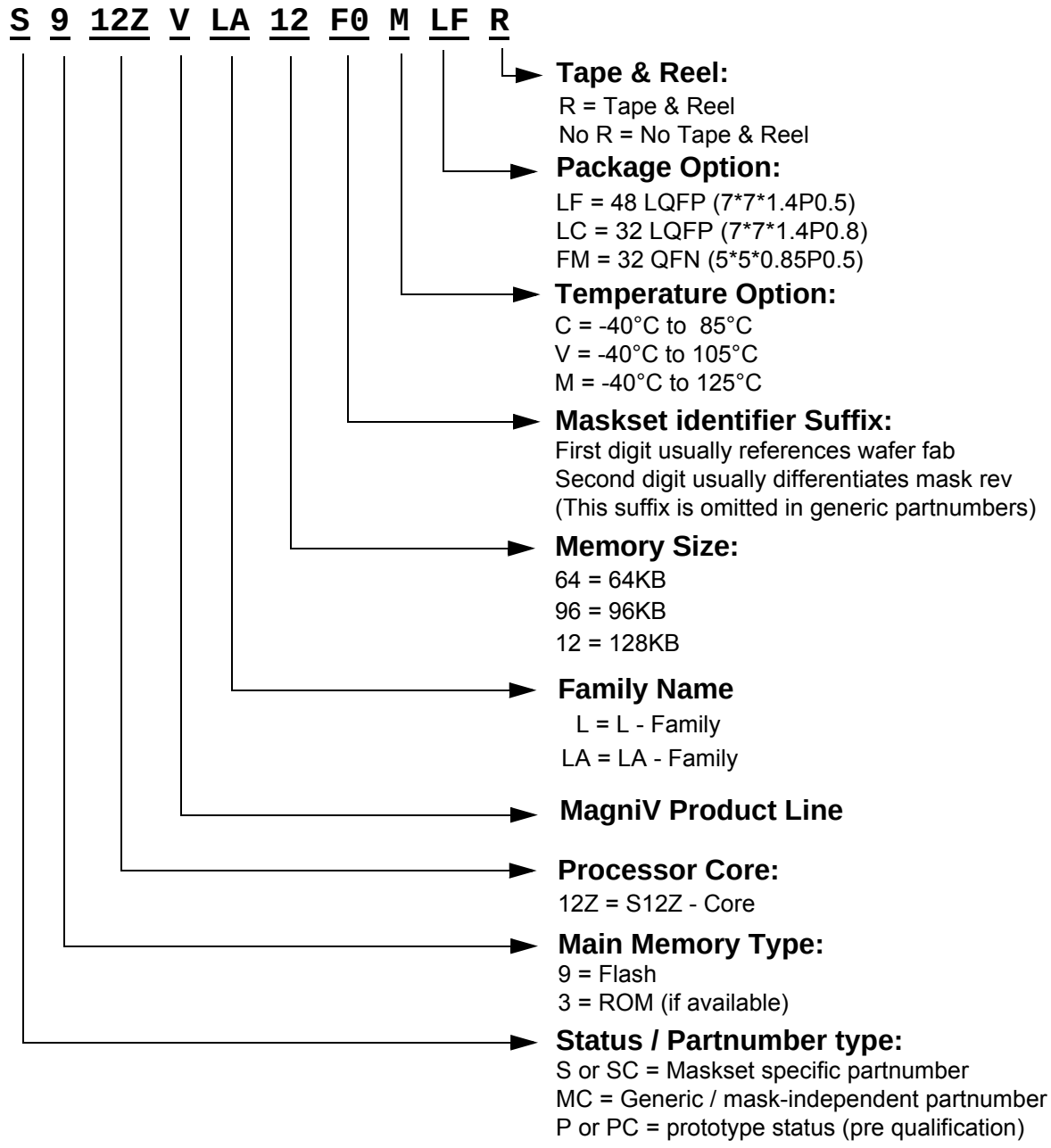


Figure N-2. Part Numbers for MC9S12ZVL(A)128/96/64

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