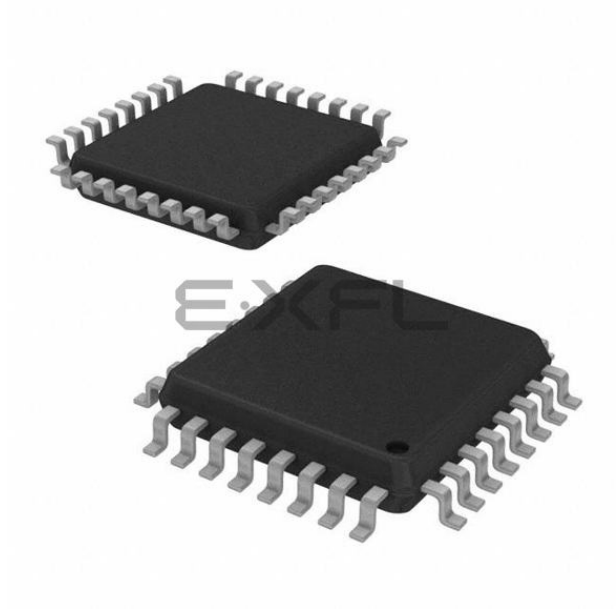

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SCI, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	19
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	5.5V ~ 18V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12zvl32f0vlc

1.6 Device Memory Map

Table 1-3 shows the device register memory map. All modules that can be instantiated more than once on S12 devices are listed with an index number, even if they are only instantiated once on this device family.

Table 1-3. Module Register Address Ranges

Address	Module	Size (Bytes)
0x0000–0x0003	Part ID Register Section 1.6.1, “Part ID Assignments	4
0x0004–0x000F	Reserved	12
0x0010–0x001F	INT	16
0x0020–0x006F	Reserved	80
0x0070–0x008F	MMC	32
0x0090–0x00FF	MMC Reserved	112
0x0100–0x017F	DBG	128
0x0180–0x01FF	Reserved	128
0x0200–0x037F	PIM	384
0x0380–0x039F	FTMRZ	32
0x03A0–0x03BF	Reserved	32
0x03C0–0x03CF	RAM ECC	16
0x03D0–0x03FF	Reserved	48
0x0400–0x042F	TIM1	48
0x0430–0x047F	Reserved	80
0x0480–0x04AF	PWM0	48
0x04B0–0x04FF	Reserved[1]	80
0x0500–0x052F	PWM1	48
0x0530–0x05BF	Reserved[1]	144
0x05C0–0x05EF	TIM0	48
0x05F0–0x05FF	Reserved	16
0x0600–0x063F	ADC	64
0x0640–0x067F	Reserved	64
0x0680–0x0687	DAC	8
0x0688–0x068F	Reserved	8
0x0690–0x0697	ACMP	8
0x0698–0x06BF	Reserved	40
0x06C0–0x06DF	CPMU	32
0x06E0–0x06EF	Reserved	16
0x06F0–0x06F7	BATS	8
0x06F8–0x06FF	Reserved	8

1.6.1 Part ID Assignments

The part ID is located in four 8-bit registers at addresses 0x0000-0x0003. The read-only value is a unique part ID for each revision of the chip. Table 1-4 shows the assigned part ID number and mask set number.

Table 1-4. Assigned Part ID Numbers

Device	Mask Set Number	Part ID
MC9S12ZVL32	N22G	0x04150000
MC9S12ZVL16	N22G	0x04150000
MC9S12ZVL8	N22G	0x04150000
MC9S12ZVLS32	N22G	0x04150000
MC9S12ZVLS16	N22G	0x04150000
MC9S12ZVL64	N37P	0x04170000
MC9S12ZVL96	N37P	0x04170000
MC9S12ZVL128	N37P	0x04170000
MC9S12ZVLA64	N37P	0x04170000
MC9S12ZVLA96	N37P	0x04170000
MC9S12ZVLA128	N37P	0x04170000

1.7 Signal Description and Device Pinouts

This section describes signals that connect off-chip. It includes pin out diagrams a table of signal properties, and detailed discussion of signals. Internal inter module signal mapping at device level is described in 1.9 Internal Signal Mapping.

1.7.1 Pin Assignment Overview

Table 1-5 provides a summary of which ports are available for 48-pin and 32-pin package option.

Table 1-5. Port availability by Package Option

	MC9S12ZVL / MC9S12ZVLA		MC9S12ZVLS
Port	**48-pin LQFP**	**32-pin LQFP / QFN-EP**	**32-pin QFN-EP**
Port AD	PAD[9:0]	PAD[5:0]	PAD[5:0]
Port E	PE[1:0]	PE[1:0]	PE[1:0]
Port L (HVI)	PL0	PL0	PL0
Port J	PJ[1:0]	-	-
Port P	PP[7:0]	PP[7,5,3,1]	PP[7,5,3,1]
Port S	PS[3:0]	PS[3:0]	PS[3:0]
Port T	PT[7:0]	PT[2:0]	PT[1:0]
sum of ports	35	20	19

1.13 Module device level dependencies

1.13.1 COP Configuration

The COP time-out rate bits CR[2:0] and the WCOP bit in the CPMUCOP register are loaded from the Flash configuration field byte at global address 0xFF_FE0E during the reset sequence. See Table 1-13 and Table 1-14 for coding.

Table 1-13. Initial COP Rate Configuration

NV[2:0] in FOPT Register	CR[2:0] in COPCTL Register
000	111
001	110
010	101
011	100
100	011
101	010
110	001
111	000

Table 1-14. Initial WCOP Configuration

NV[3] in FOPT Register	WCOP in COPCTL Register
1	0
0	1

1.13.2 BDC Command Restriction

The BDC command READ_DBGTB returns 0x00 on this device because the DBG module does not feature a trace buffer.

NOTE

This document assumes the availability of all features offered in the largest package option. Refer to the package and pin-out section in the device overview for functions not available in lower pin count packages.

2.1.2 Features

The PIM includes these distinctive registers:

- Data registers for ports E, AD, T, S, P and J when used as general-purpose I/O
- Data direction registers for ports E, AD, T, S, P and J
- Control registers to enable pull devices on ports E, AD, T, S, P, J and L
- Control registers to select pull-ups or pull-downs on ports E, AD, T, S, P and J
- Control register to enable open-drain (wired-or) mode on port S and J
- Control register to enable digital input buffers on port AD and L
- Interrupt enable register for pin interrupts and key-wakeup (KWU) on port AD, S, P and Interrupt flag register for pin interrupts and key-wakeup (KWU) on port AD, S, P and L
- Control register to configure $\overline{\text{IRQ}}$ pin operation
- Control register to enable ECLK output
- Routing registers to support signal relocation on external pins and control internal routings:
  - 6 PWM channels to alternative pins (one option each)
  - 8 TIM channels to alternative pins (one option each)
  - IIC0 to alternative pins (one option each)
  - SCI1 to alternative pins (one option each)
  - MSCAN to alternative pins (one option each)
  - ADC0 trigger input with edge select from internal TIM output compare channel link, ACMP0 output or external pins (four options)
  - Various SCI0-LINPHY0 routing options supporting standalone and LIN conformance testing
  - Internal RXD0 and RXD1 link to TIM input capture channel (IC0_3) for baud rate detection
  - Internal ACLK link to TIM input capture channel

A standard port pin has the following minimum features:

- Input/output selection
- 5V output drive
- 5V digital and analog input
- Input with selectable pull-up or pull-down device

Optional features supported on dedicated pins:

- Open drain for wired-or connections (ports S and J)
- Interrupt input with glitch filtering
- High current drive strength from VDDX with over-current protection

Table 2-27. Bit Indices of Implemented Register Bits per Port

		Port Data Register	Port Input Register	Data Direction Register	Pull Device Enable Register	Polarity Select Register	Port Interrupt Enable Register	Port Interrupt Flag Register	Digital Input Enable Register	Reduced Drive Register	Wired-Or Mode Register
Port		**PT**	**PTI**	**DDR**	**PER**	**PPS**	**PIE**	**PIF**	**DIE**	**RDR**	**WOM**
E		1-0	1-0	1-0	1-0	1-0	-	-	-	-	-
ADH		1-0	1-0	1-0	1-0	1-0	1-0	1-0	1-0	-	-
ADL		7-0	7-0	7-0	7-0	7-0	7-0	7-0	7-0	-	-
T		7-0	7-0	7-0	7-0	7-0	-	-	-	-	-
S		3-0	3-0	3-0	3-0	3-0	3-0	3-0	-	-	3-0
P		7-0	7-0	7-0	7-0	7-0	7-0	7-0	-	7,5,3,1	-
J		1-0	1-0	1-0	1-0	1-0	-	-	-	-	1-0
L		-	0	-	-	0	0	0	0	-	-

2.4.3 Pin I/O Control

Figure 2-30 illustrates the data paths to and from an I/O pin. Input and output data can always be read via the input register (PTIx, Section 2.3.3.2, “Port Input Register”) independent if the pin is used as general-purpose I/O or with a shared peripheral function. If the pin is configured as input (DDRx=0, Section 2.3.3.3, “Data Direction Register”), the pin state can also be read through the data register (PTx, Section 2.3.3.1, “Port Data Register”).

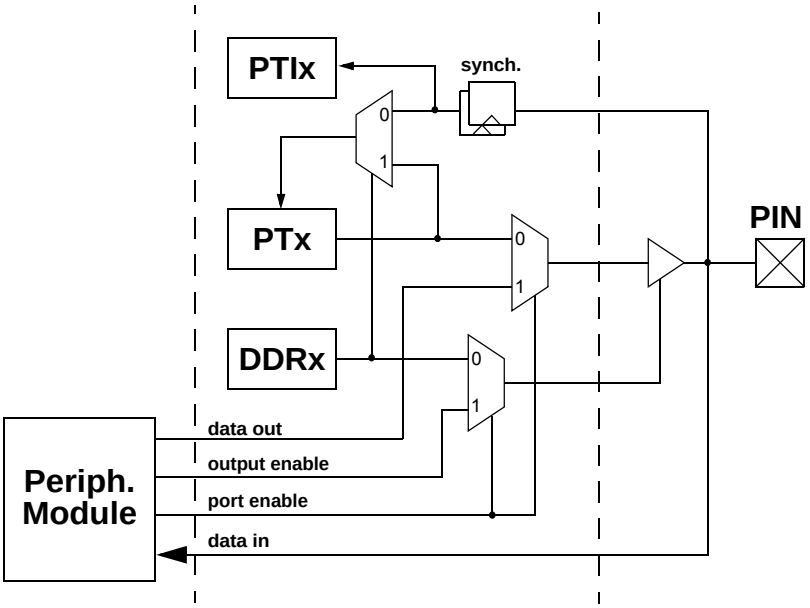

Figure 2-30. Illustration of I/O pin functionality

The general-purpose data direction configuration can be overruled by an enabled peripheral function shared on the same pin (Table 2-28). If more than one peripheral function is available and enabled at the

2.4.4 Interrupts

This section describes the interrupts generated by the PIM and their individual sources. Vector addresses and interrupt priorities are defined at MCU level.

Table 2-29. PIM Interrupt Sources

Module Interrupt Sources	Local Enable
$\overline{\text{XIRQ}}$	None
$\overline{\text{IRQ}}$	IRQCR[IRQEN]
Port AD pin interrupt	PIEADH[PIEADL1:PIEADH0] PIEADL[PIEADL7:PIEADL0]
Port S pin interrupt	PIES[PIES3:PIES0]
Port P pin interrupt	PIEP[PIEP7:PIEP0]
Port L pin interrupt	PIEL[PIEL0]
Port P over-current interrupt	OCIEP[OCIEP7,OCIEP5,OCIEP3,OCIEP1]

2.4.4.1 XIRQ, IRQ Interrupts

The $\overline{\text{XIRQ}}$ pin allows requesting non-maskable interrupts after reset initialization. During reset, the X bit in the condition code register is set and any interrupts are masked until software enables them.

The $\overline{\text{IRQ}}$ pin allows requesting asynchronous interrupts. The interrupt input is disabled out of reset. To enable the interrupt the IRQCR[IRQEN] bit must be set and the I bit cleared in the condition code register. The interrupt can be configured for level-sensitive or falling-edge-sensitive triggering. If IRQCR[IRQEN] is cleared while an interrupt is pending, the request will de-assert.

Both interrupts are capable to wake-up the device from stop mode. Means for glitch filtering are not provided on these pins.

2.4.4.2 Pin interrupts and Key-Wakeup (KWU)

Ports AD, S, P and L offer pin interrupt and key-wakeup capability. The related interrupt enable (PIE) as well as the sensitivity to rising or falling edges (PPS) can be individually configured on per-pin basis. All bits/pins in a port share the same interrupt vector. Interrupts can be used with the pins configured as inputs or outputs.

An interrupt is generated when a bit in the port interrupt flag (PIF) and its corresponding port interrupt enable (PIE) are both set. The pin interrupt feature is also capable to wake up the CPU when it is in stop or wait mode (key-wakeup).

A digital filter on each pin prevents short pulses from generating an interrupt. A valid edge on an input is detected if 4 consecutive samples of a passive level are followed by 4 consecutive samples of an active level. Else the sampling logic is restarted.

In run and wait mode the filters are continuously clocked by the bus clock. Pulses with a duration of $t_{PULSE} < n_{P\_MASK}/f_{bus}$ are assuredly filtered out while pulses with a duration of $t_{PULSE} > n_{P\_PASS}/f_{bus}$ guarantee a pin interrupt.

PP[5,3,1] connect the loads to the digital ground VSSX.

Similar protection mechanisms as for EVDD1 apply for PP[5,3,1] accordingly in an inverse way.

2.5.5 Open Input Detection on HVI

The connection of an external pull device on a high-voltage input can be validated by using the built-in pull functionality of the HVI. Depending on the application type an external pull-down circuit can be detected with the internal pull-up device whereas an external pull-up circuit can be detected with the internal pull-down device which is part of the input voltage divider.

Note that the following procedures make use of a function that overrides the automatic disable mechanism of the digital input buffer when using the HVI in analog mode. Make sure to switch off the override function when using the HVI in analog mode after the check has been completed.

External pull-down device (Figure 2-33):

1. Enable analog function on HVI in non-direct mode (PTAL[PTAENL]=1, PTAL[PTADIRL]=0)
2. Select internal pull-up device on HVI (PTAL[PTPSL]=1)
3. Enable function to force input buffer active on HVI in analog mode (PTAL[PTTEL]=1)
4. Verify PTIL=0 for a connected external pull-down device; read PTIL=1 for an open input

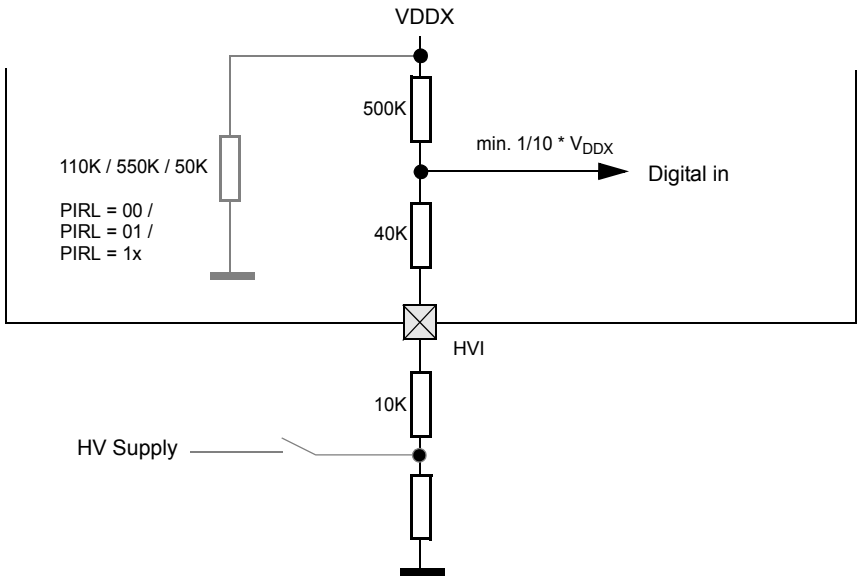

Figure 2-33. Digital Input Read with Pull-up Enabled

External pull-up device (Figure 2-34):

1. Enable analog function on HVI in non-direct mode (PTAL[PTAENL]=1, PTAL[PTADIRL]=0)
2. Select internal pulldown device on HVI (PTAL[PTPSL]=0)
3. Enable function to force input buffer active on HVI in analog mode (PTAL[PTTEL]=1)

3.7 Functional Description

The ACMP compares the analog voltage between inverting and non-inverting inputs. It generates a digital output signal and a related interrupt if enabled. The comparator output is high when the voltage at the non-inverting input is greater than the voltage at the inverting input, and is low when the non-inverting input voltage is lower than the inverting input voltage. The size of the ACMP hysteresis can be adapted to the specific application to prevent unintended rapid switching.

Both the non-inverting and inverting input of the ACMP can be selected from four inputs: Two inputs from external signals ACMP_0 and ACMP_1 and two internal inputs acmpi_0 and acmpi_1. Refer to device-level section for connectivity. The positive input is selected by ACMPC1[ACPSEL] and the negative input is selected by ACMPC1[ACNSEL]. These bits can only be changed while the ACMP is disabled.

The ACMP is enabled with ACMPC0[ACE]. When this bit is set, the inputs are connected to low-pass filters while the comparator output is disconnected from the subsequent logic for 127 bus clock cycles. During this time the output state is preserved to mask potential glitches. This initialization delay must be accounted for before the first comparison result can be expected. The same delay must be accounted for after returning from STOP mode.

The initial hold state after reset is logic level 0. If input voltages are set to result in logic level 1 ($V_{ACMPP} > V_{ACMPM}$) before the initialization delay has passed, a flag will be set immediately after the delay if rising edge is selected as flag setting event.

Similarly the ACMPS[ACIF] flag will also be set when disabling the ACMP, then re-enabling it with the inputs changing to produce an opposite result to the hold state before the end of the initialization delay.

The unsynchronized comparator output can be connected to the synchronized timer input capture channel defined at SoC-level (see Figure 3-1). This feature can be used to generate time stamps and timer interrupts on ACMP events.

The comparator output signal can be read at register bit location ACMPS[ACO].

The condition causing the interrupt flag to assert is selected with ACMPC0[ACMOD]. This includes any edge configuration, that is rising, or falling, or rising and falling edges of the comparator output. Also flag setting can be disabled.

An interrupt will be generated if the interrupt enable bit (ACMPC2[ACIE]) and the interrupt flag (ACMPS[ACIF]) are both set. ACMPS[ACIF] is cleared by writing a 1.

The comparator output signal ACMPO can be driven out on an external pin by setting ACMPC0[ACOPE] and optionally inverted by setting ACMPC0[ACOPS].

One out of four hysteresis levels can be selected by setting ACMPC0[ACHYS].

The input delay of the ACMP_0 and ACMP_1 input depends on the selected filter characteristic by ACMPC0[ACDLY].

3.8 Interrupts

Table 3-6 shows the interrupt generated by the ACMP.

Table 3-6. ACMP Interrupt Sources

Module Interrupt Sources	Local Enable
ACMP interrupt	ACMPC2[ACIE]

Chapter 5
Background Debug Controller (S12ZBDCV2)

Table 5-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V2.04	03.Dec.2012	Section 5.1.3.3, “Low-Power Modes	Included BACKGROUND/ Stop mode dependency
V2.05	22.Jan.2013	Section 5.3.2.2, “BDC Control Status Register Low (BDCCSRL)	Improved NORESP description and added STEP1/ Wait mode dependency
V2.06	22.Mar.2013	Section 5.3.2.2, “BDC Control Status Register Low (BDCCSRL)	Improved NORESP description of STEP1/ Wait mode dependency
V2.07	11.Apr.2013	Section 5.1.3.3.1, “Stop Mode	Improved STOP and BACKGROUND interdepency description
V2.08	31.May.2013	Section 5.4.4.4, “BACKGROUND Section 5.4.7.1, “Long-ACK Hardware Handshake Protocol	Removed misleading WAIT and BACKGROUND interdepency description Added subsection dedicated to Long-ACK
V2.09	29.Aug.2013	Section 5.4.4.12, “READ_DBGTB	Noted that READ_DBGTB is only available for devices featuring a trace buffer.
V2.10	21.Oct.2013	Section 5.1.3.3.2, “Wait Mode	Improved description of NORESP dependence on WAIT and BACKROUND
V2.11	02.Feb.2015	Section 5.1.3.3.1, “Stop Mode Section 5.3.2, “Register Descriptions	Corrected name of clock that can stay active in Stop mode

5.1 Introduction

The background debug controller (BDC) is a single-wire, background debug system implemented in on-chip hardware for minimal CPU intervention. The device BKGD pin interfaces directly to the BDC.

The S12ZBDC maintains the standard S12 serial interface protocol but introduces an enhanced handshake protocol and enhanced BDC command set to support the linear instruction set family of S12Z devices and offer easier, more flexible internal resource access over the BDC serial interface.

9.3.2 Register Descriptions

This section describes all the S12CPMU_UHV registers and their individual bits.

Address order is as listed in Figure 9-3

9.3.2.1 Reserved Register CPMUVREGTRIM0

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in Special Mode can alter the S12CPMU_UHV's functionality.

.

Module Base + 0x0001

	7	6	5	4	3	2	1	0
R	0	0	0	0	U			
W								
Reset	0	0	0	0	F	F	F	F
Power on Reset	0	0	0	0	0	0	0	0

Note: After de-assert of System Reset a value is automatically loaded from the Flash memory.

Figure 9-4. Reserved Register (CPMUVREGTRIM0)

Read: Anytime

Write: Only in Special Mode

9.3.2.2 Reserved Register CPMUVREGTRIM1

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in Special Mode can alter the S12CPMU_UHV's functionality.

.

Module Base + 0x0002

	7	6	5	4	3	2	1	0
R	0	0	U			U		
W								
Reset	0	0	F	F	F	F	F	F
Power on Reset	0	0	0	0	0	0	0	0

Note: After de-assert of System Reset a value is automatically loaded from the Flash memory.

Figure 9-5. Reserved Register (CPMUVREGTRIM1)

Read: Anytime

Write: Only in Special Mode

9.3.2.3 S12CPMU_UHV Reset Flags Register (CPMURFLG)

This register provides S12CPMU_UHV reset flags.

Module Base + 0x0003

	7	6	5	4	3	2	1	0
R	0	PORF	LVRF	0	COPRF	0	OMRF	PMRF
W								
Reset	0	Note 1	Note 2	0	Note 3	0	Note 4	Note 5

1. PORF is set to 1 when a power on reset occurs. Unaffected by System Reset.
2. LVRF is set to 1 when a low voltage reset occurs. Unaffected by System Reset. Set by power on reset.
3. COPRF is set to 1 when COP reset occurs. Unaffected by System Reset. Cleared by power on reset.
4. OMRF is set to 1 when an oscillator clock monitor reset occurs. Unaffected by System Reset. Cleared by power on reset.
5. PMRF is set to 1 when a PLL clock monitor reset occurs. Unaffected by System Reset. Cleared by power on reset.

= Unimplemented or Reserved

Figure 9-6. S12CPMU_UHV Flags Register (CPMURFLG)

Read: Anytime

Write: Refer to each bit for individual write conditions

9.3.2.25 S12CPMU_UHV Protection Register (CPMUPROT)

This register protects the following important configuration registers from accidental overwrite:

CPMUSYNR, CPMUREFDIV, CPMUCLKS, CPMUPLL, CPMUIRCTRIMH/L, CPMUOSC and CPMUOSC2

Module Base + 0x001B

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	PROT
W								
Reset	0	0	0	0	0	0	0	0

Figure 9-34. S12CPMU_UHV Protection Register (CPMUPROT)

Read: Anytime

Write: Anytime

Field	Description
PROT	**Clock Configuration Registers Protection Bit** — This bit protects the clock and voltage regulator configuration registers from accidental overwrite (see list of protected registers above): Writing 0x26 to the CPMUPROT register clears the PROT bit, other write accesses set the PROT bit. 0 Protection of clock and voltage regulator configuration registers is disabled. 1 Protection of clock and voltage regulator configuration registers is enabled. (see list of protected registers above).

12.3.2.2 PGA Control Register (PGACNTL)

Module Base + 0x0001 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	PGAREFSEL[1:0]		0	0	PGAINSEL[1:0]	
W								
Reset	0	0	0	0	0	0	0	0

Figure 12-4. PGA Control Register (PGACNTL)

1 Read: Anytime
Write: Anytime

Table 12-4. PGACNTL Field Description

Field	Description
5:4 PGAREFSEL[1:0]	**PGA reference voltage selection** — If PGAEN=1 these register bits select the source for the reference voltage (PGAREF, minus input of both amplifier stages). 00 Internally generated V_{DDA} / 2 is selected as reference voltage (PGAREF) 01 Reserved 10 External PGA_REF0 input is selected as reference voltage (PGAREF). 11 External PGA_REF1 input is selected as reference voltage (PGAREF).
1:0 PGAINSEL[1:0]	**PGA input voltages selection** — This register bit defines the source for the plus input voltage of the amplifier. 00 no input voltage selected (PGAIN). 01 input voltage selection controlled by external modules, please see SoC level connection for more details. If the external control signals enables both inputs, then PGA_IN0 is selected. 10 PGA_IN0 is selected as input voltage (PGAIN). 11 PGA_IN1 is selected as input voltage (PGAIN).

12.3.2.3 PGA Gain Register (PGAGAIN)

Module Base + 0x0002 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0				PGAGAIN[3:0]			
W								
Reset	0	0	0	0	0	0	0	0

Figure 12-5. PGA Gain Register (PGAGAIN)

1 Read: Anytime
Write: Anytime

Table 12-5. PGAGAIN Field Description

Field	Description
3:0 PGAGAIN[3:0]	**PGA1 gain**— These register bits select the gain A_{PGA} (amplification factor) for the PGA stage, see Table 12-6., “Amplifier Gain

Module Base + 0x00XF

Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
W								
Reset:	x	x	x	x	x	x	x	x

Figure 13-37. Time Stamp Register — Low Byte (TSRL)

1 Read: or transmit buffers: Anytime when TXEx flag is set (see Section 13.3.2.7, “MSCAN Transmitter Flag Register (CANTFLG)”) and the corresponding transmit buffer is selected in CANTBSEL (see Section 13.3.2.11, “MSCAN Transmit Buffer Selection Register (CANTBSEL)”). For receive buffers: Anytime when RXF is set.
Write: Unimplemented

17.2.1 PWM7 - PWM0 — PWM Channel 7 - 0

Those pins serve as waveform output of PWM channel 7 - 0.

17.3 Memory Map and Register Definition

17.3.1 Module Memory Map

This section describes the content of the registers in the scalable PWM module. The base address of the scalable PWM module is determined at the MCU level when the MCU is defined. The register decode map is fixed and begins at the first address of the module address offset. The figure below shows the registers associated with the scalable PWM and their relative offset from the base address. The register detail description follows the order they appear in the register map.

Reserved bits within a register will always read as 0 and the write will be unimplemented. Unimplemented functions are indicated by shading the bit.

NOTE

Register Address = Base Address + Address Offset, where the Base Address is defined at the MCU level and the Address Offset is defined at the module level.

17.3.2 Register Descriptions

This section describes in detail all the registers and register bits in the scalable PWM module.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 PWME[1]	R	PWME7	PWME6	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0
	W								
0x0001 PWMPOL[1]	R	PPOL7	PPOL6	PPOL5	PPOL4	PPOL3	PPOL2	PPOL1	PPOL0
	W								
0x0002 PWMCLK[1]	R	PCLK7	PCLKL6	PCLK5	PCLK4	PCLK3	PCLK2	PCLK1	PCLK0
	W								
0x0003 PWMPRCLK	R	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
	W								
0x0004 PWMCAE[1]	R	CAE7	CAE6	CAE5	CAE4	CAE3	CAE2	CAE1	CAE0
	W								
0x0005 PWMCTL[1]	R	CON67	CON45	CON23	CON01	PSWAI	PFRZ	0	0
	W								

= Unimplemented or Reserved

Figure 17-2. The scalable PWM Register Summary (Sheet 1 of 4)

$$\text{BaudRateDivisor} = (\text{SPPR} + 1) \bullet 2^{(\text{SPR} + 1)} \qquad \textit{Eqn. 19-3}$$

When all bits are clear (the default condition), the SPI module clock is divided by 2. When the selection bits (SPR2–SPR0) are 001 and the preselection bits (SPPR2–SPPR0) are 000, the module clock divisor becomes 4. When the selection bits are 010, the module clock divisor becomes 8, etc.

When the preselection bits are 001, the divisor determined by the selection bits is multiplied by 2. When the preselection bits are 010, the divisor is multiplied by 3, etc. See Table 19-7 for baud rate calculations for all bit conditions, based on a 25 MHz bus clock. The two sets of selects allows the clock to be divided by a non-power of two to achieve other baud rates such as divide by 6, divide by 10, etc.

The baud rate generator is activated only when the SPI is in master mode and a serial transfer is taking place. In the other cases, the divider is disabled to decrease I_{DD} current.

NOTE

For maximum allowed baud rates, please refer to the SPI Electrical Specification in the Electricals chapter of this data sheet.

19.4.5 Special Features

19.4.5.1 $\overline{SS}$ Output

The $\overline{SS}$ output feature automatically drives the $\overline{SS}$ pin low during transmission to select external devices and drives it high during idle to deselect external devices. When $\overline{SS}$ output is selected, the $\overline{SS}$ output pin is connected to the $\overline{SS}$ input pin of the external device.

The $\overline{SS}$ output is available only in master mode during normal SPI operation by asserting SSOE and MODFEN bit as shown in Table 19-3.

The mode fault feature is disabled while $\overline{SS}$ output is enabled.

NOTE

Care must be taken when using the $\overline{SS}$ output feature in a multimaster system because the mode fault feature is not available for detecting system errors between masters.

19.4.5.2 Bidirectional Mode (MOMI or SISO)

The bidirectional mode is selected when the SPC0 bit is set in SPI control register 2 (see Table 19-11). In this mode, the SPI uses only one serial data pin for the interface with external device(s). The MSTR bit decides which pin to use. The MOSI pin becomes the serial data I/O (MOMI) pin for the master mode, and the MISO pin becomes serial data I/O (SISO) pin for the slave mode. The MISO pin in master mode and MOSI pin in slave mode are not used by the SPI.

It is possible to read from P-Flash memory while some commands are executing on EEPROM memory. It is not possible to read from EEPROM memory while a command is executing on P-Flash memory from the same block. Simultaneous P-Flash and EEPROM operations are discussed in Section 22.4.6.

Both P-Flash and EEPROM memories are implemented with Error Correction Codes (ECC) that can resolve single bit faults and detect double bit faults. For P-Flash memory, the ECC implementation requires that programming be done on an aligned 8 byte basis (a Flash phrase). Since P-Flash memory is always read by half-phrase, only one single bit fault in an aligned 4 byte half-phrase containing the byte or word accessed will be corrected.

22.1.1 Glossary

Command Write Sequence — An MCU instruction sequence to execute built-in algorithms (including program and erase) on the Flash memory.

EEPROM Memory — The EEPROM memory constitutes the nonvolatile memory store for data.

EEPROM Sector — The EEPROM sector is the smallest portion of the EEPROM memory that can be erased. The EEPROM sector consists of 4 bytes.

NVM Command Mode — An NVM mode using the CPU to setup the FCCOB register to pass parameters required for Flash command execution.

Phrase — An aligned group of four 16-bit words within the P-Flash memory. Each phrase includes two sets of aligned double words with each set including 7 ECC bits for single bit fault correction and double bit fault detection within each double word.

P-Flash Memory — The P-Flash memory constitutes the main nonvolatile memory store for applications.

P-Flash Sector — The P-Flash sector is the smallest portion of the P-Flash memory that can be erased. Each P-Flash sector contains 512 bytes.

Program IFR — Nonvolatile information register located in the P-Flash block that contains the Version ID, and the Program Once field.

22.1.2 Features

22.1.2.1 P-Flash Features

- Derivatives featuring up to and including 128 KB of P-Flash include one P-Flash block
- Derivatives featuring more than 128 KB of P-Flash include two Flash blocks
- In each case the P-Flash sector size is 512 bytes
- Single bit fault correction and double bit fault detection within a 32-bit double word during read operations

Mnemonic	Nominal Voltage	Description
VSSX2	0V	Ground pin for I/O drivers
VDDA	5.0 V	5V Power supply for the analog-to-digital converter and for the reference circuit of the internal voltage regulator if VREG5VEN is set
VDDA	3.3 V	3.3V Power supply for the analog-to-digital converter and for the reference circuit of the internal voltage regulator if VREG5VEN is cleared
VSSA	0V	Ground pin for VDDA analog supply
LGND	0V	Ground pin for LIN physical interface
VSUP	12V/18V	External power supply for voltage regulator

NOTE

VDDA is connected to VDDX pins by diodes for ESD protection such that VDDX must not exceed VDDA by more than a diode voltage drop. VSSA and VSSX are connected by anti-parallel diodes for ESD protection.

A.1.1 Pins

There are 4 groups of functional pins.

A.1.1.1 General Purpose I/O Pins (GPIO)

The I/O pins have a level in the VDDX/VDDA range of 5V. This class of pins is comprised of all port I/O pins, BKGD and the $\overline{\text{RESET}}$ pins.

A.1.1.2 High Voltage Pins

These consist of the LIN and the BCTL pin. These pins are intended to interface to external components operating in the automotive battery range. They have nominal voltages above the standard 5V I/O voltage range.

A.1.1.3 Oscillator

If the external oscillator is enabled, the EXTAL and XTAL pins have an operating range of 1.8V.

If the designated EXTAL and XTAL pins are configured for external oscillator operation then these pins have a nominal voltage of 1.8V.

A.1.1.4 TEST

This pin is used for production testing only. The TEST pin must be tied to ground in all applications.

I.3 Dynamic Electrical Characteristics

Table I-3. Dynamic Electrical Characteristics of the analog comparator - ACMP

Characteristics noted under conditions $3.20V \le V_{DDA} \le 5.15V$, $-40°C \le T_J \le 175°C$[1] unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25°C$[2] under nominal conditions unless otherwise noted.						
Num	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	Output uncertain time after module enable	$t_{ACMP\_dly\_en}$	-	1	2	µs
2	ACMP Propagation Delay of Inputs ACMP0 and ACMP1 for $-2*V_{hyst(typ)}$ to $+2*V_{hyst(typ)}$ input step (w/o synchronize delay) • ACDLY=0 Low speed mode • ACDLY=1 High speed mode ACMPP is crossing ACMPN in positive direction	t_{ACMP_delay}	130 20	300 70	750 400	ns ns
3	ACMP Propagation Delay of Inputs ACMP0 and ACMP1 for $-2*V_{hyst(typ)}$ to $+2*V_{hyst(typ)}$ input step (w/o synchronize delay) $150°C \le T_J \le 175°C$ • ACDLY=0 Low speed mode • ACDLY=1 High speed mode ACMPP is crossing ACMPN in positive direction	t_{ACMP_delay}	- -	- -	800 450	ns ns

1 T_J: Junction Temperature

2 T_A: Ambient Temperature