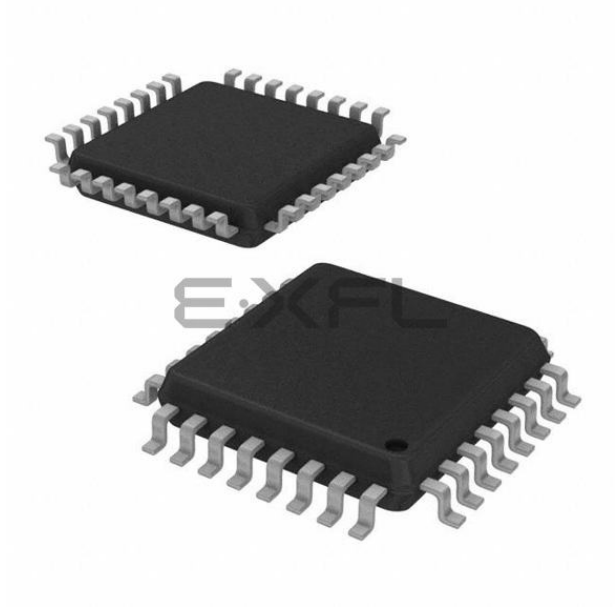

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Connectivity	I²C, IrDA, LINbus, SCI, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	19
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	5.5V ~ 18V
Data Converters	A/D 6x10b
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Operating Temperature	-40°C ~ 105°C (TA)
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Supplier Device Package	32-LQFP (7x7)
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Chapter 10
Analog-to-Digital Converter (ADC12B_LBA)

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1.12 Resets and Interrupts

1.12.1 Resets

Table 1-11. lists all reset sources and the vector locations. Resets are explained in detail in the Chapter 9, “S12 Clock, Reset and Power Management Unit (S12CPMU_UHV)”.

Table 1-11. Reset Sources and Vector Locations

Vector Address	Reset Source	CCR Mask	Local Enable
0xFFFFFC	Power-On Reset (POR)	None	None
	Low Voltage Reset (LVR)	None	None
	External pin $\overline{\text{RESET}}$	None	None
	Clock monitor reset	None	OSCE Bit in CPMUOSC and OMRE Bit in CPMUOSC2 register
	COP watchdog reset	None	CR[2:0] in CPMUCOP register

1.12.2 Interrupt Vectors

Table 1-12 lists all interrupt sources and vectors in the default order of priority. The interrupt module description provides an interrupt vector base register (IVBR) to relocate the vectors.

Table 1-12. Interrupt Vector Locations (Sheet 1 of 4)

Vector Address[1]	Interrupt Source	CCR Mask	Local Enable	Wake up from STOP	Wake up from WAIT
Vector base + 0x1F8	Unimplemented page1 op-code trap (SPARE)	None	None	-	-
Vector base + 0x1F4	Unimplemented page2 op-code trap (TRAP)	None	None	-	-
Vector base + 0x1F0	Software interrupt instruction (SWI)	None	None	-	-
Vector base + 0x1EC	System call interrupt instruction (SYS)	None	None	-	-
Vector base + 0x1E8	Machine exception	None	None	-	-
Vector base + 0x1E4	Reserved				
Vector base + 0x1E0	Reserved				
Vector base + 0x1DC	Spurious interrupt	—	None	-	-
Vector base + 0x1D8	$\overline{\text{XIRQ}}$ interrupt request	X bit	None	Yes	Yes
Vector base + 0x1D4	$\overline{\text{IRQ}}$ interrupt request	I bit	IRQCR(IRQEN)	Yes	Yes
Vector base + 0x1D0	RTI time-out interrupt	I bit	CPMUINT (RTIE)	**See CPMU section**	Yes

3.7 Functional Description

The ACMP compares the analog voltage between inverting and non-inverting inputs. It generates a digital output signal and a related interrupt if enabled. The comparator output is high when the voltage at the non-inverting input is greater than the voltage at the inverting input, and is low when the non-inverting input voltage is lower than the inverting input voltage. The size of the ACMP hysteresis can be adapted to the specific application to prevent unintended rapid switching.

Both the non-inverting and inverting input of the ACMP can be selected from four inputs: Two inputs from external signals ACMP_0 and ACMP_1 and two internal inputs acmpi_0 and acmpi_1. Refer to device-level section for connectivity. The positive input is selected by ACMPC1[ACPSEL] and the negative input is selected by ACMPC1[ACNSEL]. These bits can only be changed while the ACMP is disabled.

The ACMP is enabled with ACMPC0[ACE]. When this bit is set, the inputs are connected to low-pass filters while the comparator output is disconnected from the subsequent logic for 127 bus clock cycles. During this time the output state is preserved to mask potential glitches. This initialization delay must be accounted for before the first comparison result can be expected. The same delay must be accounted for after returning from STOP mode.

The initial hold state after reset is logic level 0. If input voltages are set to result in logic level 1 ($V_{ACMPP} > V_{ACMPM}$) before the initialization delay has passed, a flag will be set immediately after the delay if rising edge is selected as flag setting event.

Similarly the ACMPS[ACIF] flag will also be set when disabling the ACMP, then re-enabling it with the inputs changing to produce an opposite result to the hold state before the end of the initialization delay.

The unsynchronized comparator output can be connected to the synchronized timer input capture channel defined at SoC-level (see Figure 3-1). This feature can be used to generate time stamps and timer interrupts on ACMP events.

The comparator output signal can be read at register bit location ACMPS[ACO].

The condition causing the interrupt flag to assert is selected with ACMPC0[ACMOD]. This includes any edge configuration, that is rising, or falling, or rising and falling edges of the comparator output. Also flag setting can be disabled.

An interrupt will be generated if the interrupt enable bit (ACMPC2[ACIE]) and the interrupt flag (ACMPS[ACIF]) are both set. ACMPS[ACIF] is cleared by writing a 1.

The comparator output signal ACMPO can be driven out on an external pin by setting ACMPC0[ACOPE] and optionally inverted by setting ACMPC0[ACOPS].

One out of four hysteresis levels can be selected by setting ACMPC0[ACHYS].

The input delay of the ACMP_0 and ACMP_1 input depends on the selected filter characteristic by ACMPC0[ACDLY].

Chapter 6
Interrupt (S12ZINTV0)

Table 6-1. Revision History

Version Number	Revision Date	Effective Date	Description of Changes
V00.10	21 Feb 2012	all	Corrected reset value for INT_CFADDR register
V00.11	02 Jul 2012	all	Removed references and functions related to XGATE
V00.12	22 May 2013	all	added footnote about availability of “Wake-up from STOP or WAIT by XIRQ with X bit set” feature

6.1 Introduction

The S12ZINTV0 module decodes the priority of all system exception requests and provides the applicable vector for processing the exception to the CPU. The S12ZINTV0 module supports:

- I-bit and X-bit maskable interrupt requests
- One non-maskable unimplemented page1 op-code trap
- One non-maskable unimplemented page2 op-code trap
- One non-maskable software interrupt (SWI)
- One non-maskable system call interrupt (SYS)
- One non-maskable machine exception vector request
- One spurious interrupt vector request
- One system reset vector request

Each of the I-bit maskable interrupt requests can be assigned to one of seven priority levels supporting a flexible priority scheme. The priority scheme can be used to implement nested interrupt capability where interrupts from a lower level are automatically blocked if a higher level interrupt is being processed.

6.1.1 Glossary

The following terms and abbreviations are used in the document.

Table 6-2. Terminology

Term	Meaning
CCW	Condition Code Register (in the S12Z CPU)
DMA	Direct Memory Access
INT	Interrupt
IPL	Interrupt Processing Level
ISR	Interrupt Service Routine

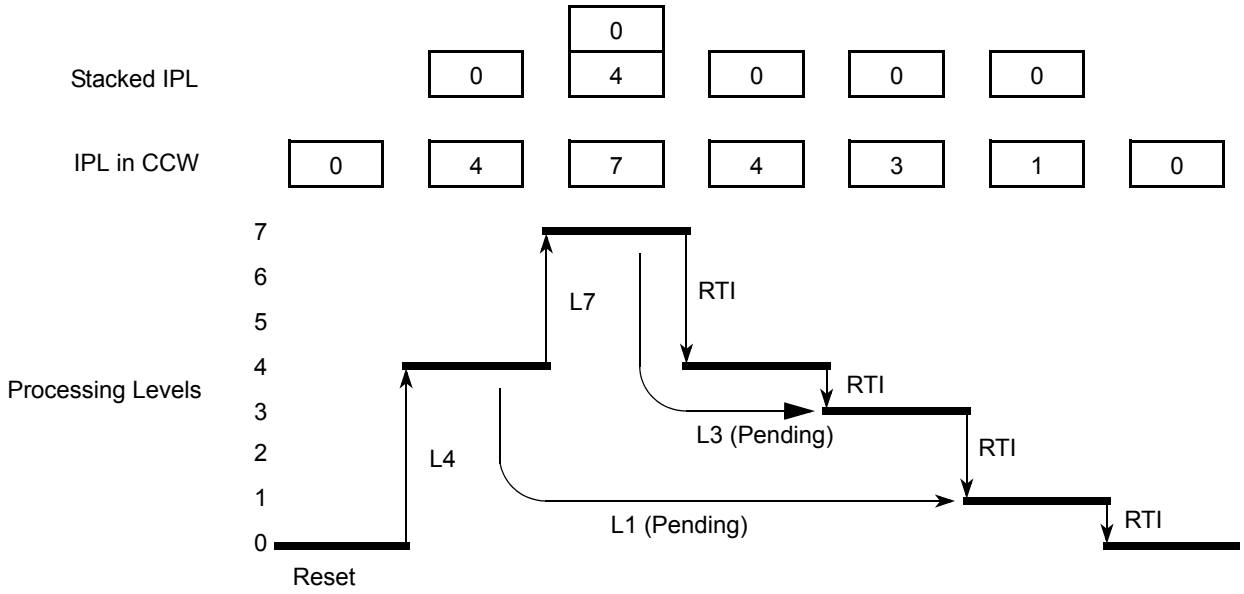


Figure 6-14. Interrupt Processing Example

6.5.3 Wake Up from Stop or Wait Mode

6.5.3.1 CPU Wake Up from Stop or Wait Mode

Every I-bit maskable interrupt request which is configured to be handled by the CPU is capable of waking the MCU from stop or wait mode. Additionally machine exceptions can wake-up the MCU from stop or wait mode.

To determine whether an I-bit maskable interrupts is qualified to wake up the CPU or not, the same settings as in normal run mode are applied during stop or wait mode:

- If the I-bit in the CCW is set, all I-bit maskable interrupts are masked from waking up the MCU.
- An I-bit maskable interrupt is ignored if it is configured to a priority level below or equal to the current IPL in CCW.

The X-bit maskable interrupt request can wake up the MCU from stop or wait mode at anytime, even if the X-bit in CCW is set[1]. If the X-bit maskable interrupt request is used to wake-up the MCU with the X-bit in the CCW set, the associated ISR is not called. The CPU then resumes program execution with the instruction following the WAI or STOP instruction. This feature works following the same rules like any interrupt request, i.e. care must be taken that the X-bit maskable interrupt request used for wake-up remains active at least until the system begins execution of the instruction following the WAI or STOP instruction; otherwise, wake-up may not occur.

1. The capability of the $\overline{\text{XIRQ}}$ pin to wake-up the MCU with the X bit set may not be available if, for example, the $\overline{\text{XIRQ}}$ pin is shared with other peripheral modules on the device. Please refer to the Port Integration Module (PIM) section of the MCU reference manual for details.

9.3.2.10 S12CPMU_UHV PLL Control Register (CPMUPLL)

This register controls the PLL functionality.

Module Base + 0x000A

	7	6	5	4	3	2	1	0
R	0	0	FM1	FM0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 9-13. S12CPMU_UHV PLL Control Register (CPMUPLL)

Read: Anytime

Write: Anytime if PROT=0 (CPMUPROT register) and PLLSEL=1 (CPMUCLKS register). Else write has no effect.

NOTE

Write to this register clears the LOCK and UPOSC status bits.

NOTE

Care should be taken to ensure that the bus frequency does not exceed the specified maximum when frequency modulation is enabled.

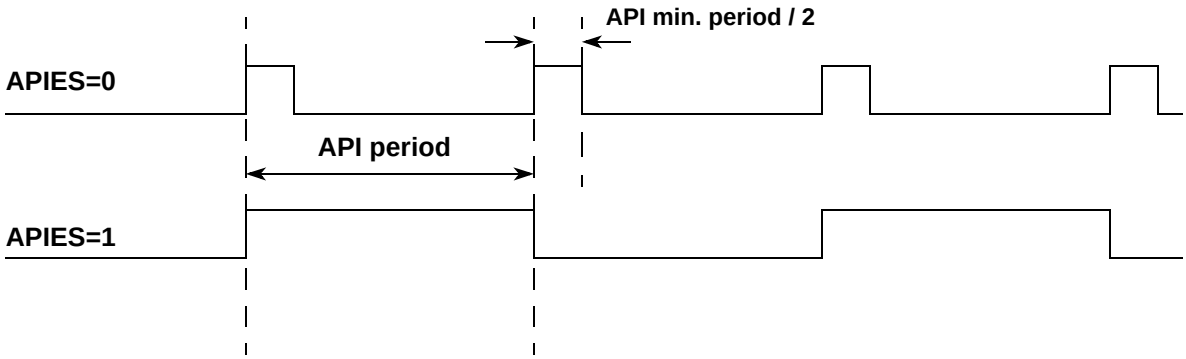
Table 9-9. CPMUPLL Field Descriptions

Field	Description
5, 4 FM1, FM0	PLL **Frequency Modulation Enable Bits** — FM1 and FM0 enable frequency modulation on the VCOCLK. This is to reduce noise emission. The modulation frequency is f_{ref} divided by 16. See Table 9-10 for coding.

Table 9-10. FM Amplitude selection

FM1	FM0	FM Amplitude / f_{VCO} Variation
0	0	FM off
0	1	±1%
1	0	±2%
1	1	±4%

Figure 9-23. Waveform selected on API_EXTCLK pin (APIEA=1, APIFE=1)



10.5 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the ADC12B_LBA.

10.5.1 Module Memory Map

Figure 10-3 gives an overview of all ADC12B_LBA registers.

NOTE

Register Address = Base Address + Address Offset, where the Base Address is defined at the MCU level and the Address Offset is defined at the module level.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000	ADCCTL_0	R	ADC_EN	ADC_SR	FRZ_MOD	SWAI	ACC_CFG[1:0]		STR_SEQA	MOD_CFG
		W								
0x0001	ADCCTL_1	R	CSL_BMOD	RVL_BMOD	SMOD_ACC	AUT_RSTA	0	0	0	0
		W								
0x0002	ADCSTS	R	CSL_SEL	RVL_SEL	DBECC_ERR	Reserved	READY	0	0	0
		W								
0x0003	ADCTIM	R	0	PRS[6:0]						
		W								
0x0004	ADCFMT	R	DJM	0	0	0	0	SRES[2:0]		
		W								
0x0005	ADCFLWCTL	R	SEQA	TRIG	RSTA	LDOK	0	0	0	0
		W								
0x0006	ADCEIE	R	IA_EIE	CMD_EIE	EOL_EIE	Reserved	TRIG_EIE	RSTAR_EIE	LDOK_EIE	0
		W								
0x0007	ADCIE	R	SEQAD_IE	CONIF_OIE	Reserved	0	0	0	0	0
		W								
0x0008	ADCEiF	R	IA_EIF	CMD_EIF	EOL_EIF	Reserved	TRIG_EIF	RSTAR_EIF	LDOK_EIF	0
		W								
0x0009	ADCIF	R	SEQAD_IF	CONIF_OIF	Reserved	0	0	0	0	0
		W								
0x000A	ADCCONIE_0	R	CON_IE[15:8]							
		W								
0x000B	ADCCONIE_1	R	CON_IE[7:1]							EOL_IE
		W								
0x000C	ADCCONIF_0	R	CON_IF[15:8]							
		W								
0x000D	ADCCONIF_1	R	CON_IF[7:1]							EOL_IF
		W								
0x000E	ADCIMDRI_0	R	CSL_IMD	RVL_IMD	0	0	0	0	0	0
		W								
0x000F	ADCIMDRI_1	R	0	0	RIDX_IMD[5:0]					
		W								

= Unimplemented or Reserved

Figure 10-3. ADC12B_LBA Register Summary (Sheet 1 of 3)

NOTE

The CANCTL0 register, except WUPE, INITRQ, and SLPRQ, is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK = 1). This register is writable again as soon as the initialization mode is exited (INITRQ = 0 and INITAK = 0).

Table 13-3. CANCTL0 Register Field Descriptions

Field	Description
7 RXFRM	**Received Frame Flag** — This bit is read and clear only. It is set when a receiver has received a valid message correctly, independently of the filter configuration. After it is set, it remains set until cleared by software or reset. Clearing is done by writing a 1. Writing a 0 is ignored. This bit is not valid in loopback mode. 0 No valid message was received since last clearing this flag 1 A valid message was received since last clearing of this flag
6 RXACT	**Receiver Active Status** — This read-only flag indicates the MSCAN is receiving a message[1]. The flag is controlled by the receiver front end. This bit is not valid in loopback mode. 0 MSCAN is transmitting or idle 1 MSCAN is receiving a message (including when arbitration is lost)
5 CSWAI[2]	**CAN Stops in Wait Mode** — Enabling this bit allows for lower power consumption in wait mode by disabling all the clocks at the CPU bus interface to the MSCAN module. 0 The module is not affected during wait mode 1 The module ceases to be clocked during wait mode
4 SYNCH	**Synchronized Status** — This read-only flag indicates whether the MSCAN is synchronized to the CAN bus and able to participate in the communication process. It is set and cleared by the MSCAN. 0 MSCAN is not synchronized to the CAN bus 1 MSCAN is synchronized to the CAN bus
3 TIME	**Timer Enable** — This bit activates an internal 16-bit wide free running timer which is clocked by the bit clock rate. If the timer is enabled, a 16-bit time stamp will be assigned to each transmitted/received message within the active TX/RX buffer. Right after the EOF of a valid message on the CAN bus, the time stamp is written to the highest bytes (0x000E, 0x000F) in the appropriate buffer (see Section 13.3.3, “Programmer’s Model of Message Storage”). In loopback mode no receive timestamp is generated. The internal timer is reset (all bits set to 0) when disabled. This bit is held low in initialization mode. 0 Disable internal MSCAN timer 1 Enable internal MSCAN timer
2 WUPE[3]	**Wake-Up Enable** — This configuration bit allows the MSCAN to restart from sleep mode or from power down mode (entered from sleep) when traffic on CAN is detected (see Section 13.4.5.5, “MSCAN Sleep Mode”). This bit must be configured before sleep mode entry for the selected function to take effect. 0 Wake-up disabled — The MSCAN ignores traffic on CAN 1 Wake-up enabled — The MSCAN is able to restart

If the WUPE bit in CANCTL0 is not asserted, the MSCAN will mask any activity it detects on CAN. RXCAN is therefore held internally in a recessive state. This locks the MSCAN in sleep mode. WUPE must be set before entering sleep mode to take effect.

The MSCAN is able to leave sleep mode (wake up) only when:

- CAN bus activity occurs and WUPE = 1

  or
- the CPU clears the SLPRQ bit

NOTE

The CPU cannot clear the SLPRQ bit before sleep mode (SLPRQ = 1 and SLPAK = 1) is active.

After wake-up, the MSCAN waits for 11 consecutive recessive bits to synchronize to the CAN bus. As a consequence, if the MSCAN is woken-up by a CAN frame, this frame is not received.

The receive message buffers (RxFG and RxBG) contain messages if they were received before sleep mode was entered. All pending actions will be executed upon wake-up; copying of RxBG into RxFG, message aborts and message transmissions. If the MSCAN remains in bus-off state after sleep mode was exited, it continues counting the 128 occurrences of 11 consecutive recessive bits.

13.4.5.6 MSCAN Power Down Mode

The MSCAN is in power down mode (Table 13-37) when

- CPU is in stop mode

  or
- CPU is in wait mode and the CSWAI bit is set

When entering the power down mode, the MSCAN immediately stops all ongoing transmissions and receptions, potentially causing CAN protocol violations. To protect the CAN bus system from fatal consequences of violations to the above rule, the MSCAN immediately drives TXCAN into a recessive state.

NOTE

The user is responsible for ensuring that the MSCAN is not active when power down mode is entered. The recommended procedure is to bring the MSCAN into Sleep mode before the STOP or WAI instruction (if CSWAI is set) is executed. Otherwise, the abort of an ongoing message can cause an error condition and impact other CAN bus devices.

In power down mode, all clocks are stopped and no registers can be accessed. If the MSCAN was not in sleep mode before power down mode became active, the module performs an internal recovery cycle after powering up. This causes some fixed delay before the module enters normal mode again.

Module Base + 0x00006

	7	6	5	4	3	2	1	0
R W	PCLKAB7	PCLKAB6	PCLKAB5	PCLKAB4	PCLKAB3	PCLKAB2	PCLKAB1	PCLKAB0
Reset	0	0	0	0	0	0	0	0

Figure 17-9. PWM Clock Select Register (PWMCLK)

Read: Anytime

Write: Anytime

NOTE

Register bits PCLKAB0 to PCLKAB7 can be written anytime. If a clock select is changed while a PWM signal is being generated, a truncated or stretched pulse can occur during the transition.

Table 17-11. PWMCLK Field Descriptions

Note: Bits related to available channels have functional significance. Writing to unavailable bits has no effect. Read from unavailable bits return a zero

Field	Description
7 PCLKAB7	Pulse Width Channel 7 Clock A/B Select 0 Clock B or SB is the clock source for PWM channel 7, as shown in Table 17-6. 1 Clock A or SA is the clock source for PWM channel 7, as shown in Table 17-6.
6 PCLKAB6	Pulse Width Channel 6 Clock A/B Select 0 Clock B or SB is the clock source for PWM channel 6, as shown in Table 17-6. 1 Clock A or SA is the clock source for PWM channel 6, as shown in Table 17-6.
5 PCLKAB5	Pulse Width Channel 5 Clock A/B Select 0 Clock A or SA is the clock source for PWM channel 5, as shown in Table 17-5. 1 Clock B or SB is the clock source for PWM channel 5, as shown in Table 17-5.
4 PCLKAB4	Pulse Width Channel 4 Clock A/B Select 0 Clock A or SA is the clock source for PWM channel 4, as shown in Table 17-5. 1 Clock B or SB is the clock source for PWM channel 4, as shown in Table 17-5.
3 PCLKAB3	Pulse Width Channel 3 Clock A/B Select 0 Clock B or SB is the clock source for PWM channel 3, as shown in Table 17-6. 1 Clock A or SA is the clock source for PWM channel 3, as shown in Table 17-6.
2 PCLKAB2	Pulse Width Channel 2 Clock A/B Select 0 Clock B or SB is the clock source for PWM channel 2, as shown in Table 17-6. 1 Clock A or SA is the clock source for PWM channel 2, as shown in Table 17-6.
1 PCLKAB1	Pulse Width Channel 1 Clock A/B Select 0 Clock A or SA is the clock source for PWM channel 1, as shown in Table 17-5. 1 Clock B or SB is the clock source for PWM channel 1, as shown in Table 17-5.
0 PCLKAB0	Pulse Width Channel 0 Clock A/B Select 0 Clock A or SA is the clock source for PWM channel 0, as shown in Table 17-5. 1 Clock B or SB is the clock source for PWM channel 0, as shown in Table 17-5.

The clock source of each PWM channel is determined by PCLKx bits in PWMCLK (see Section 17.3.2.3, “PWM Clock Select Register (PWMCLK)) and PCLKABx bits in PWMCLKAB as shown in Table 17-5

18.1.4 Block Diagram

Figure 18-1 is a high level block diagram of the SCI module, showing the interaction of various function blocks.

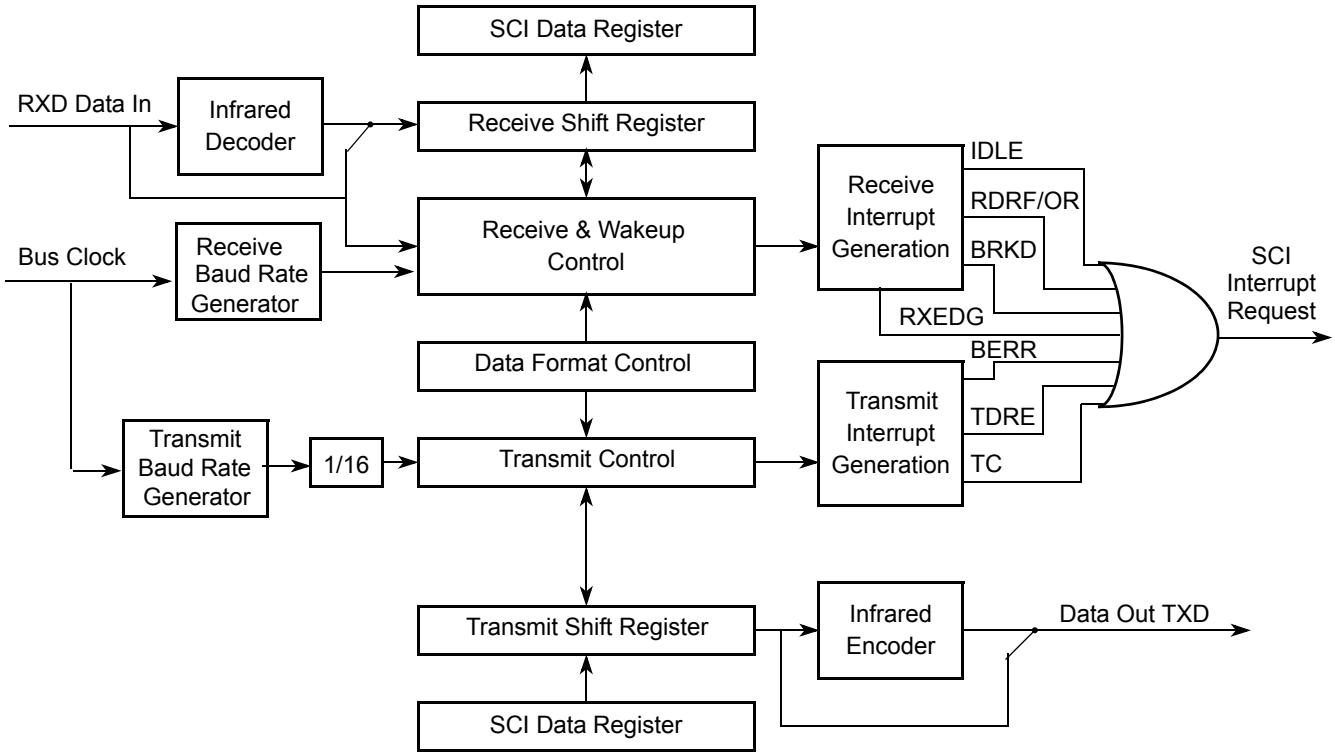


Figure 18-1. SCI Block Diagram

18.2 External Signal Description

The SCI module has a total of two external pins.

18.2.1 TXD — Transmit Pin

The TXD pin transmits SCI (standard or infrared) data. It will idle high in either mode and is high impedance anytime the transmitter is disabled.

18.2.2 RXD — Receive Pin

The RXD pin receives SCI (standard or infrared) data. An idle line is detected as a line high. This input is ignored when the receiver is disabled and should be terminated to a known voltage.

18.3 Memory Map and Register Definition

This section provides a detailed description of all the SCI registers.

19.3.2.5 SPI Data Register (SPIDR = SPIDRH:SPIDRL)

Module Base +0x0004

	7	6	5	4	3	2	1	0
R	R15	R14	R13	R12	R11	R10	R9	R8
W	T15	T14	T13	T12	T11	T10	T9	T8
Reset	0	0	0	0	0	0	0	0

Figure 19-7. SPI Data Register High (SPIDRH)

Module Base +0x0005

	7	6	5	4	3	2	1	0
R	R7	R6	R5	R4	R3	R2	R1	R0
W	T7	T6	T5	T4	T3	T2	T1	T0
Reset	0	0	0	0	0	0	0	0

Figure 19-8. SPI Data Register Low (SPIDRL)

Read: Anytime; read data only valid when SPIF is set

Write: Anytime

The SPI data register is both the input and output register for SPI data. A write to this register allows data to be queued and transmitted. For an SPI configured as a master, queued data is transmitted immediately after the previous transmission has completed. The SPI transmitter empty flag SPTEF in the SPISR register indicates when the SPI data register is ready to accept new data.

Received data in the SPIDR is valid when SPIF is set.

If SPIF is cleared and data has been received, the received data is transferred from the receive shift register to the SPIDR and SPIF is set.

If SPIF is set and not serviced, and a second data value has been received, the second received data is kept as valid data in the receive shift register until the start of another transmission. The data in the SPIDR does not change.

If SPIF is set and valid data is in the receive shift register, and SPIF is serviced before the start of a third transmission, the data in the receive shift register is transferred into the SPIDR and SPIF remains set (see Figure 19-9).

If SPIF is set and valid data is in the receive shift register, and SPIF is serviced after the start of a third transmission, the data in the receive shift register has become invalid and is not transferred into the SPIDR (see Figure 19-10).

20.4.1.8 Handshaking

The clock synchronization mechanism can be used as a handshake in data transfer. Slave devices may hold the SCL low after completion of one byte transfer (9 bits). In such case, it halts the bus clock and forces the master clock into wait states until the slave releases the SCL line.

20.4.1.9 Clock Stretching

The clock synchronization mechanism can be used by slaves to slow down the bit rate of a transfer. After the master has driven SCL low the slave can drive SCL low for the required period and then release it.If the slave SCL low period is greater than the master SCL low period then the resulting SCL bus signal low period is stretched.

20.4.1.10 Ten-bit Address

A ten-bit address is indicated if the first 5 bits of the first address byte are 0x11110. The following rules apply to the first address byte.

SLAVE ADDRESS	R/W BIT	DESCRIPTION
0000000	0	General call address
0000010	x	Reserved for different bus format
0000011	x	Reserved for future purposes
11111XX	x	Reserved for future purposes
11110XX	x	10-bit slave addressing

Figure 20-13. Definition of bits in the first byte.

The address type is identified by ADTYPE. When ADTYPE is 0, 7-bit address is applied. Reversely, the address is 10-bit address.Generally, there are two cases of 10-bit address.See the Figure 20-14 and Figure 20-15.

S	Slave Add1st 7bits 11110+ADR10+ADR9	R/W 0	A1	Slave Add 2nd byte ADR[8:1]	A2	Data	A3

Figure 20-14. A master-transmitter addresses a slave-receiver with a 10-bit address

S	Slave Add1st 7bits 11110+ADR10+ADR9	R/W 0	A1	Slave Add 2nd byte ADR[8:1]	A2	Sr	Slave Add 1st 7bits 11110+ADR10+ADR9	R/W 1	A3	Data	A4

Figure 20-15. A master-receiver addresses a slave-transmitter with a 10-bit address.

In the Figure 20-15, the first two bytes are the similar to Figure 20-14. After the repeated START(Sr),the first slave address is transmitted again, but the R/W is 1, meaning that the slave is acted as a transmitter.

Table 22-31. Allowed P-Flash and EEPROM Simultaneous Operations on a single hardblock

	EEPROM				
Program Flash	**Read**	**Margin Read[2]**	**Program**	**Sector Erase**	**Mass Erase[2]**
Read	OK[1]	OK	OK	OK	
Margin Read[2]					
Program					
Sector Erase					
Mass Erase[3]					OK

1 Strictly speaking, only one read of either the P-Flash or EEPROM can occur at any given instant, but the memory controller will transparently arbitrate P-Flash and EEPROM accesses giving uninterrupted read access whenever possible.

2 A 'Margin Read' is any read after executing the margin setting commands 'Set User Margin Level' or 'Set Field Margin Level' with anything but the 'normal' level specified. See the Note on margin settings in Section 22.4.7.12 and Section 22.4.7.13.

3 The 'Mass Erase' operations are commands 'Erase All Blocks' and 'Erase Flash Block'

22.4.7 Flash Command Description

This section provides details of all available Flash commands launched by a command write sequence. The ACCERR bit in the FSTAT register will be set during the command write sequence if any of the following illegal steps are performed, causing the command not to be processed by the Memory Controller:

- Starting any command write sequence that programs or erases Flash memory before initializing the FCLKDIV register
- Writing an invalid command as part of the command write sequence
- For additional possible errors, refer to the error handling table provided for each command

If a Flash block is read during execution of an algorithm (CCIF = 0) on that same block, the read operation may return invalid data resulting in an illegal access (as described on Section 22.4.6).

If the ACCERR or FPVIOL bits are set in the FSTAT register, the user must clear these bits before starting any command write sequence (see Section 22.3.2.7).

CAUTION

A Flash word or phrase must be in the erased state before being programmed. Cumulative programming of bits within a Flash word or phrase is not allowed.

22.4.7.1 Erase Verify All Blocks Command

The Erase Verify All Blocks command will verify that all P-Flash and EEPROM blocks have been erased.

Table A-8. Thermal Package Characteristics for ZVL(S)32/16/8[1]

Num	Rating	Symbol	Min	Typ	Max	Unit
48LQFP						
1	Thermal resistance 48LQFP, single sided PCB[1] Natural Convection	θ_{JA}	—	80	—	°C/W
2	Thermal resistance 48LQFP, double sided PCB with 2 internal planes[2]. Natural Convection.	θ_{JA}	—	56	—	°C/W
3	Thermal resistance 48LQFP, single sided PCB[1] (@200 ft/min)	θ_{JA}	—	67	—	°C/W
4	Thermal resistance 48LQFP, double sided PCB with 2 internal planes[2] (@200 ft/min).	θ_{JA}	—	50	—	°C/W
5	Junction to Board 48LQFP[3]	θ_{JB}	—	34	—	°C/W
6	Junction to Case Top 48LQFP[4]	θ_{JCtop}	—	24	—	°C/W
7	Junction to Package Top 48LQFP[5]	Ψ_{JT}	—	6	—	°C/W
32LQFP						
8	Thermal resistance 32LQFP, single sided PCB[1] Natural Convection	θ_{JA}	—	84	—	°C/W
9	Thermal resistance 32LQFP, double sided PCB with 2 internal planes[2]. Natural Convection	θ_{JA}	—	56	—	°C/W
10	Thermal resistance 32LQFP, single sided PCB[1] (@200 ft/min)	θ_{JA}	—	71	—	°C/W
11	Thermal resistance 32LQFP, double sided PCB with 2 internal planes[2] (@200 ft/min).	θ_{JA}	—	49	—	°C/W
12	Junction to Board 32LQFP[3]	θ_{JB}	—	32	—	°C/W
13	Junction to Case Top 32LQFP[4]	θ_{JCtop}	—	23	—	°C/W
14	Junction to Package Top 32LQFP[5]	Ψ_{JT}	—	6	—	°C/W
32QFN-EP						
15	Thermal resistance 32QFN-EP, single sided PCB[1] Natural Convection	θ_{JA}	—	96	—	°C/W
16	Thermal resistance 32QFN-EP, double sided PCB with 2 internal planes[2]. Natural Convection	θ_{JA}	—	33	—	°C/W
17	Thermal resistance 32QFN-EP, single sided PCB[1] (@200 ft/min)	θ_{JA}	—	80	—	°C/W
18	Thermal resistance 32QFN-EP, double sided PCB with 2 internal planes[2] (@200 ft/min).	θ_{JA}	—	28	—	°C/W
19	Junction to Board 32QFN-EP[3]	θ_{JB}	—	13	—	°C/W
20	Junction to Case Top 32QFN-EP[4]	θ_{JCtop}	—	25	—	°C/W
21	Junction to Case Bottom 32QFN-EP[5]	$\theta_{JCbottom}$	—	2.22	—	°C/W
22	Junction to Package Top 32QFN-EP[5]	Ψ_{JT}	—	3	—	°C/W

[1] Junction to ambient thermal resistance, θ_{JA} was simulated to be equivalent to JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.

Appendix G
DAC_8B5V Electrical Specifications

This section describe the electrical characteristics of the DAC_8B5V module.

NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

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TITLE: LQFP, 48 LEAD, 0.50 PITCH (7.0 X 7.0 X 1.4)	DOCUMENT NO: 98ASH00962A	REV: G
	CASE NUMBER: 932-03	14 APR 2005
	STANDARD: JEDEC MS-026-BBC	

O.17 0x0700-0x0707 SCI0 (continued)

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0706	SCI0DRH	R	R8	T8	0	0	0	0	0	0
		W								
0x0707	SCI0DRL	R	R7	R6	R5	R4	R3	R2	R1	R0
		W	T7	T6	T5	T4	T3	T2	T1	T0

1 These registers are accessible if the AMAP bit in the SCISR2 register is set to zero.

2 These registers are accessible if the AMAP bit in the SCISR2 register is set to one.

O.18 0x0710-0x0717 SCI1

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0710	SCI1BDH[1]	R	SBR15	SBR14	SBR13	SBR12	SBR11	SBR10	SBR9	SBR8
		W								
0x0711	SCI1BDL[1]	R	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
		W								
0x0712	SCI1CR1[1]	R	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
		W								
0x0710	SCI1ASR1[2]	R	RXEDGIF	0	0	0	0	BERRV	BERRIF	BKDIF
		W								
0x0711	SCI1ACR1[2]	R	RXEDGIE	0	0	0	0	0	BERRIE	BKDIE
		W								
0x0712	SCI1ACR2[2]	R	IREN	TNP1	TNP0	0	0	BERRM1	BERRM0	BKDFE
		W								
0x0713	SCI1CR2	R	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		W								
0x0714	SCI1SR1	R	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		W								
0x0715	SCI1SR2	R	AMAP	0	0	TXPOL	RXPOL	BRK13	TXDIR	RAF
		W								
0x0716	SCI1DRH	R	R8	T8	0	0	0	0	0	0
		W								
0x0717	SCI1DRL	R	R7	R6	R5	R4	R3	R2	R1	R0
		W	T7	T6	T5	T4	T3	T2	T1	T0

1 These registers are accessible if the AMAP bit in the SCISR2 register is set to zero.

2 These registers are accessible if the AMAP bit in the SCISR2 register is set to one.

O.19 0x0780-0x0787 SPI0

Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0780	SPI0CR1	R	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
		W								
0x0781	SPI0CR2	R	0	XFRW	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
		W								
0x0782	SPI0BR	R	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
		W								
0x0783	SPI0SR	R	SPIF	0	SPTEF	MODF	0	0	0	0
		W								
0x0784	SPI0DRH	R	R15	R14	R13	R12	R11	R10	R9	R8
		W	T15	T14	T13	T12	T11	T10	T9	T8
0x0785	SPI0DRL	R	R7	R6	R5	R4	R3	R2	R1	R0
		W	T7	T6	T5	T4	T3	T2	T1	T0
0x0786	Reserved	R								
		W								
0x0787	Reserved	R								
		W								