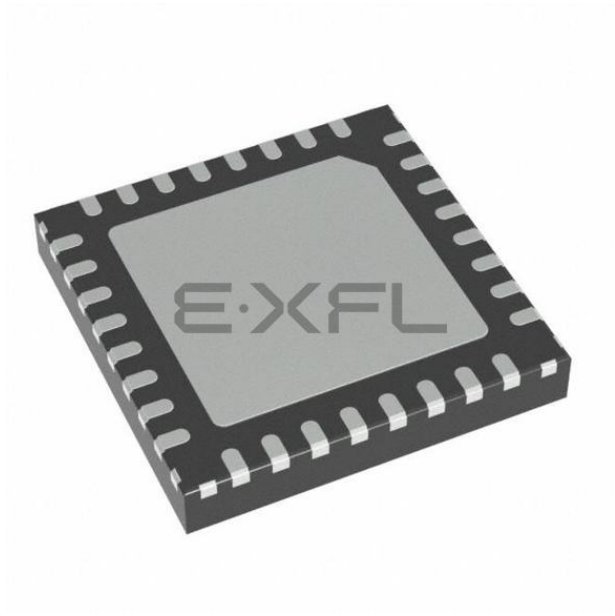

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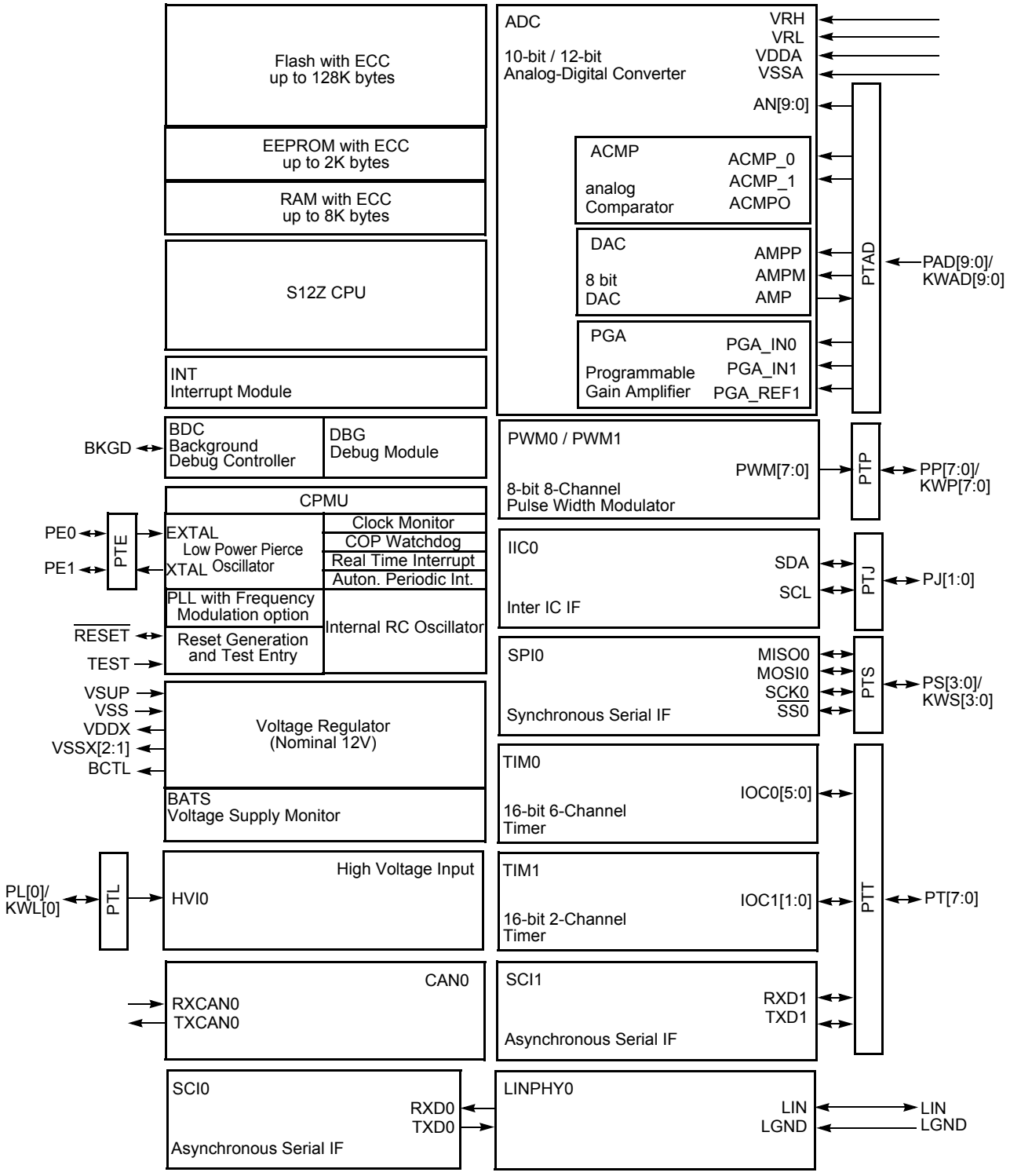
Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SCI, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	19
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	5.5V ~ 18V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount, Wettable Flank
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-QFN-EP (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12zvls1f0mfm

1.5 Block Diagram



Block Diagram shows the maximum configuration
Not all pins or all peripherals are available on all devices and packages.
Rerouting options are not shown.

Figure 1-1. MC9S12ZVL-Family Block Diagram

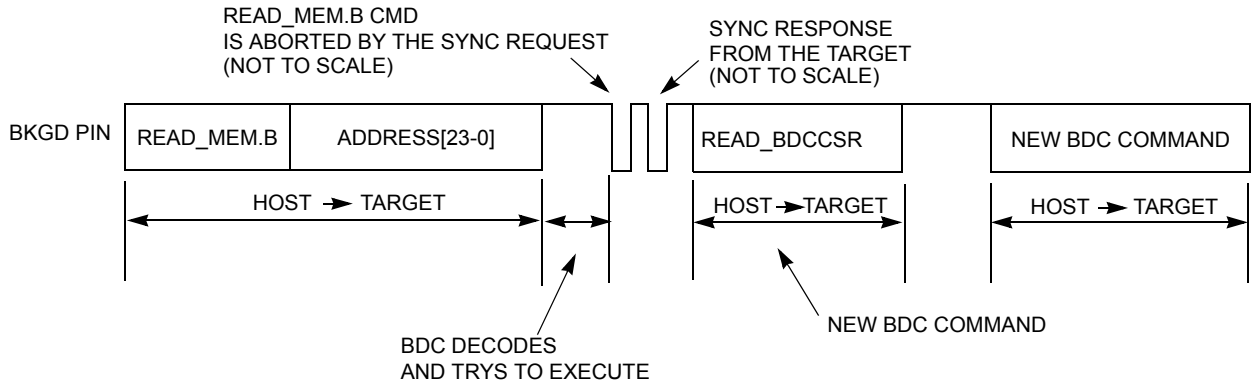


Figure 5-11. ACK Abort Procedure at the Command Level (Not To Scale)

Figure 5-12 shows a conflict between the ACK pulse and the SYNC request pulse. The target is executing a pending BDC command at the exact moment the host is being connected to the BKGD pin. In this case, an ACK pulse is issued simultaneously to the SYNC command. Thus there is an electrical conflict between the ACK speedup pulse and the SYNC pulse. As this is not a probable situation, the protocol does not prevent this conflict from happening.

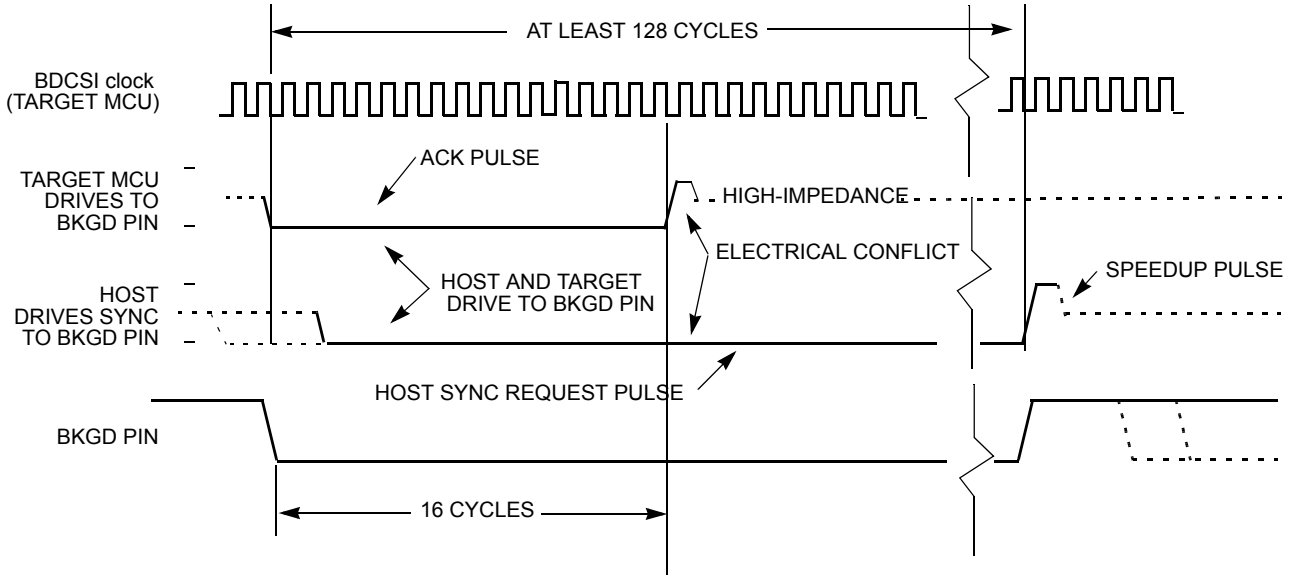


Figure 5-12. ACK Pulse and SYNC Request Conflict

5.4.9 Hardware Handshake Disabled (ACK Pulse Disabled)

The default state of the BDC after reset is hardware handshake protocol disabled. It can also be disabled by the ACK_DISABLE BDC command. This provides backwards compatibility with the existing host devices which are not able to execute the hardware handshake protocol. For host devices that support the hardware handshake protocol, true non-intrusive debugging and error flagging is offered.

If the ACK pulse protocol is disabled, the host needs to use the worst case delay time at the appropriate places in the protocol.

5.4.11 Serial Communication Timeout

The host initiates a host-to-target serial transmission by generating a falling edge on the BKGD pin. If BKGD is kept low for more than 128 target clock cycles, the target understands that a SYNC command was issued. In this case, the target waits for a rising edge on BKGD in order to answer the SYNC request pulse. When the BDC detects the rising edge a soft reset is generated, whereby the current BDC command is discarded. If the rising edge is not detected, the target keeps waiting forever without any timeout limit.

If a falling edge is not detected by the target within 512 clock cycles since the last falling edge, a timeout occurs and the current command is discarded without affecting memory or the operating mode of the MCU. This is referred to as a soft-reset. This timeout also applies if 512 cycles elapse between 2 consecutive ERASE_FLASH commands. The soft reset is disabled whilst the internal flash mass erase operation is pending completion.

timeouts are also possible if a BDC command is partially issued, or data partially retrieved. Thus if a time greater than 512 BDCSI clock cycles is observed between two consecutive negative edges, a soft-reset occurs causing the partially received command or data retrieved to be discarded. The next negative edge at the BKGD pin, after a soft-reset has occurred, is considered by the target as the start of a new BDC command, or the start of a SYNC request pulse.

5.5 Application Information

5.5.1 Clock Frequency Considerations

Read commands without status and without ACK must consider the frequency relationship between BDCSI and the internal core clock. If the core clock is slow, then the internal access may not have been carried out within the standard 16 BDCSI cycle delay period (DLY). The host must then extend the DLY period or clock frequencies accordingly. Taking internal clock domain synchronizers into account, the minimum number of BDCSI periods required for the DLY is expressed by:

$$\#DLY > 3(f_{(BDCSI\ clock)} / f_{(core\ clock)}) + 4$$

and the minimum core clock frequency with respect to BDCSI clock frequency is expressed by

$$\text{Minimum } f_{(core\ clock)} = (3/(\#DLY \text{ cycles } -4))f_{(BDCSI\ clock)}$$

For the standard 16 period DLY this yields $f_{(core\ clock)} >= (1/4)f_{(BDCSI\ clock)}$

7.3.2.14 Debug Comparator D Control Register (DBGDCTL)

Address: 0x0140

	7	6	5	4	3	2	1	0
R	0	0	INST	0	RW	RWE	reserved	COMPE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 7-17. Debug Comparator D Control Register

Read: Anytime.

Write: If DBG not armed.

Table 7-24. DBGDCTL Field Descriptions

Field[1]	Description
5 INST	**Instruction Select** — This bit configures the comparator to compare PC or data access addresses. 0 Comparator compares addresses of data accesses 1 Comparator compares PC address
3 RW	**Read/Write Comparator Value Bit** — The RW bit controls whether read or write is used in compare for the associated comparator. The RW bit is ignored if RWE is clear or INST is set. 0 Write cycle is matched 1 Read cycle is matched
2 RWE	**Read/Write Enable Bit** — The RWE bit controls whether read or write comparison is enabled for the associated comparator. This bit is ignored if INST is set. 0 Read/Write is not used in comparison 1 Read/Write is used in comparison
0 COMPE	**Enable Bit** — Determines if comparator is enabled 0 The comparator is not enabled 1 The comparator is enabled

1 If the CDCM field selects range mode comparisons, then DBGCCTL bits configure the comparison, DBGDCTL is ignored.

Table 7-25 shows the effect for RWE and RW on the comparison conditions. These bits are ignored if INST is set, because matches based on opcodes reaching the execution stage are data independent.

Table 7-25. Read or Write Comparison Logic Table

RWE Bit	RW Bit	RW Signal	Comment
0	x	0	RW not used in comparison
0	x	1	RW not used in comparison
1	0	0	Write match
1	0	1	No match
1	1	0	No match
1	1	1	Read match

8.2.2.5 ECC Debug Data (ECCDDH, ECCDDL)

Module Base + 0x000C — Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	DDATA[15:8]							
Reset	0	0	0	0	0	0	0	0

Module Base + 0x000D — Access: User read/write

	7	6	5	4	3	2	1	0
R W	DDATA[7:0]							
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 8-6. ECC Debug Data (ECCDDH, ECCDDL)

[1] Read: Anytime
Write: Anytime

Table 8-6. ECCDD Register Field Descriptions

Field	Description
DDATA [23:0]	**ECC Debug Raw Data** — This register contains the raw data which will be written into the system memory during a debug write command or the read data from the debug read command.

8.2.2.6 ECC Debug ECC (ECCDE)

Module Base + 0x000E — Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	DECC[5:0]					
W								
Reset	0	0	0	0	0	0	0	0

[1] Read: Anytime
Write: Anytime

Figure 8-7. ECC Debug ECC (ECCDE)

Table 8-7. ECCDE Field Description

Field	Description
5:0 DECC[5:0]	**ECC Debug ECC** — This register contains the raw ECC value which will be written into the system memory during a debug write command or the ECC read value from the debug read command.

If XOSCLCP is enabled (OSCE=1) $$f_{REF} = \frac{f_{OSC}}{(REFDIV + 1)}$$

If XOSCLCP is disabled (OSCE=0) $$f_{REF} = f_{IRC1M}$$

The REFFRQ[1:0] bits are used to configure the internal PLL filter for optimal stability and lock time. For correct PLL operation the REFFRQ[1:0] bits have to be selected according to the actual REFCLK frequency as shown in Table 9-4.

If IRC1M is selected as REFCLK (OSCE=0) the PLL filter is fixed configured for the 1MHz <= f_{REF} <= 2MHz range. The bits can still be written but will have no effect on the PLL filter configuration.

For OSCE=1, setting the REFFRQ[1:0] bits incorrectly can result in a non functional PLL (no locking and/or insufficient stability).

Table 9-4. Reference Clock Frequency Selection if OSC_LCP is enabled

REFCLK Frequency Ranges (OSCE=1)	REFFRQ[1:0]
1MHz <= f_{REF} <= 2MHz	00
2MHz < f_{REF} <= 6MHz	01
6MHz < f_{REF} <= 12MHz	10
f_{REF} >12MHz	11

9.3.2.26 Reserved Register CPMUTEST2

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in Special Mode can alter the S12CPMU_UHV's functionality.

Module Base + 0x001C

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-35. Reserved Register CPMUTEST2

Read: Anytime

Write: Only in Special Mode

10.5.2.13 ADC Intermediate Result Information Register (ADCIMDRI)

This register is cleared when bit ADC_SR is set or bit ADC_EN is clear.

Module Base + 0x000E

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	CSL_IMD	RVL_IMD	0	0	0	0	0	0	0	0	RIDX_IMD[5:0]					
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 10-16. ADC Intermediate Result Information Register (ADCIMDRI)

Read: Anytime

Write: Never

Table 10-18. ADCIMDRI Field Descriptions

Field	Description
15 CSL_IMD	**Active CSL At Intermediate Event** — This bit indicates the active (used) CSL at the occurrence of a conversion interrupt flag (CON_IF[15:1]) (occurrence of an intermediate result buffer fill event) or when a Sequence Abort Event gets executed. 0 CSL_0 active (used) when a conversion interrupt flag (CON_IF[15:1]) got set. 1 CSL_1 active (used) when a conversion interrupt flag (CON_IF[15:1]) got set.
14 RVL_IMD	**Active RVL At Intermediate Event** — This bit indicates the active (used) RVL buffer at the occurrence of a conversion interrupt flag (CON_IF[15:1]) (occurrence of an intermediate result buffer fill event) or when a Sequence Abort Event gets executed. 0 RVL_0 active (used) when a conversion interrupt flag (CON_IF[15:1]) got set. 1 RVL_1 active (used) when a conversion interrupt flag (CON_IF[15:1]) got set.
5-0 RIDX_IMD[5:0]	**RES_IDX Value At Intermediate Event** — These bits indicate the result index (RES_IDX) value at the occurrence of a conversion interrupt flag (CON_IF[15:1]) (occurrence of an intermediate result buffer fill event) or occurrence of EOL_IF flag or when a Sequence Abort Event gets executed to abort an ongoing conversion (the result index RES_IDX is captured at the occurrence of a result data store). When a Sequence Abort Event has been processed flag SEQAD_IF is set and the RES_IDX value of the last stored result is provided. Hence in case an ongoing conversion is aborted the RES_IDX value captured in RIDX_IMD bits depends on bit STORE_SEQA: - STORE_SEQA =1: The result index of the aborted conversion is provided - STORE_SEQA =0: The result index of the last stored result at abort execution time is provided In case a CSL is aborted while no conversion is ongoing (ADC waiting for a Trigger Event) the last captured result index is provided. In case a Sequence Abort Event was initiated by hardware due to MCU entering Stop Mode or Wait Mode with bit SWAI set, the result index of the last stored result is captured by bits RIDX_IMD but flag SEQAD_IF is not set.

NOTE

The register ADCIMDRI is updated and simultaneously a conversion interrupt flag CON_IF[15:1] occurs when the corresponding conversion command (conversion command with INTFLG_SEL[3:0] set) has been processed and related data has been stored to RAM.

Table 10-24. Analog Input Channel Select

CH_SEL[5]	CH_SEL[4]	CH_SEL[3]	CH_SEL[2]	CH_SEL[1]	CH_SEL[0]	Analog Input Channel
0	0	0	0	0	0	VRL_0/1 (V1, V2, see Table 10-2) VRL_0 (V3, see Table 10-2)
0	0	0	0	0	1	VRH_0/1 (V1, V2, see Table 10-2) VRH_0/1/2 (V3, see Table 10-2)
0	0	0	0	1	0	(VRH_0/1 + VRL_0/1) / 2 (V1, V2, see Table 10-2) (VRH_0/1/2 + VRL_0) / 2 (V3, see Table 10-2)
0	0	0	0	1	1	Reserved
0	0	0	1	0	0	Reserved
0	0	0	1	0	1	Reserved
0	0	0	1	1	0	Reserved
0	0	0	1	1	1	Reserved
0	0	1	0	0	0	Internal_0 (ADC temperature sense)
0	0	1	0	0	1	Internal_1
0	0	1	0	1	0	Internal_2
0	0	1	0	1	1	Internal_3
0	0	1	1	0	0	Internal_4
0	0	1	1	0	1	Internal_5
0	0	1	1	1	0	Internal_6
0	0	1	1	1	1	Internal_7
0	1	0	0	0	0	AN0
0	1	0	0	0	1	AN1
0	1	0	0	1	0	AN2
0	1	0	0	1	1	AN3
0	1	0	1	0	0	AN4
0	1	x	x	x	x	ANx
1	x	x	x	x	x	Reserved

NOTE

ANx in Table 10-24 is the maximum number of implemented analog input channels on the device. Please refer to the device overview of the reference manual for details regarding number of analog input channels.

13.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the MSCAN.

13.3.1 Module Memory Map

Figure 13-3 gives an overview on all registers and their individual bits in the MSCAN memory map. The *register address* results from the addition of *base address* and *address offset*. The *base address* is determined at the MCU level and can be found in the MCU memory map description. The *address offset* is defined at the module level.

The MSCAN occupies 64 bytes in the memory space. The base address of the MSCAN module is determined at the MCU level when the MCU is defined. The register decode map is fixed and begins at the first address of the module address offset.

The detailed register descriptions follow in the order they appear in the register map.

NOTE

The CANTBSEL register is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK=1). This register is writable when not in initialization mode (INITRQ = 0 and INITAK = 0).

Table 13-17. CANTBSEL Register Field Descriptions

Field	Description
2-0 TX[2:0]	**Transmit Buffer Select** — The lowest numbered bit places the respective transmit buffer in the CANTXFG register space (e.g., TX1 = 1 and TX0 = 1 selects transmit buffer TX0; TX1 = 1 and TX0 = 0 selects transmit buffer TX1). Read and write accesses to the selected transmit buffer will be blocked, if the corresponding TXEx bit is cleared and the buffer is scheduled for transmission (see Section 13.3.2.7, “MSCAN Transmitter Flag Register (CANTFLG)”). 0 The associated message buffer is deselected 1 The associated message buffer is selected, if lowest numbered bit

The following gives a short programming example of the usage of the CANTBSEL register:

To get the next available transmit buffer, application software must read the CANTFLG register and write this value back into the CANTBSEL register. In this example Tx buffers TX1 and TX2 are available. The value read from CANTFLG is therefore 0b0000_0110. When writing this value back to CANTBSEL, the Tx buffer TX1 is selected in the CANTXFG because the lowest numbered bit set to 1 is at bit position 1. Reading back this value out of CANTBSEL results in 0b0000_0010, because only the lowest numbered bit position set to 1 is presented. This mechanism eases the application software’s selection of the next available Tx buffer.

- LDAA CANTFLG; value read is 0b0000_0110
- STAA CANTBSEL; value written is 0b0000_0110
- LDAA CANTBSEL; value read is 0b0000_0010

If all transmit message buffers are deselected, no accesses are allowed to the CANTXFG registers.

13.3.2.12 MSCAN Identifier Acceptance Control Register (CANIDAC)

The CANIDAC register is used for identifier acceptance control as described below.

Module Base + 0x000B — Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 13-15. MSCAN Identifier Acceptance Control Register (CANIDAC)

1 Read: Anytime
Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1), except bits IDHITx, which are read-only

Table 13-35. Time Segment Syntax

Syntax	Description
SYNC_SEG	System expects transitions to occur on the CAN bus during this period.
Transmit Point	A node in transmit mode transfers a new value to the CAN bus at this point.
Sample Point	A node in receive mode samples the CAN bus at this point. If the three samples per bit option is selected, then this point marks the position of the third sample.

The synchronization jump width (see the Bosch CAN 2.0A/B specification for details) can be programmed in a range of 1 to 4 time quanta by setting the SJW parameter.

The SYNC_SEG, TSEG1, TSEG2, and SJW parameters are set by programming the MSCAN bus timing registers (CANBTR0, CANBTR1) (see Section 13.3.2.3, “MSCAN Bus Timing Register 0 (CANBTR0)” and Section 13.3.2.4, “MSCAN Bus Timing Register 1 (CANBTR1)”).

Table 13-36 gives an overview of the Bosch CAN 2.0A/B specification compliant segment settings and the related parameter values.

NOTE

It is the user’s responsibility to ensure the bit time settings are in compliance with the CAN standard.

Table 13-36. Bosch CAN 2.0A/B Compliant Bit Time Segment Settings

Time Segment 1	TSEG1	Time Segment 2	TSEG2	Synchronization Jump Width	SJW
5 .. 10	4 .. 9	2	1	1 .. 2	0 .. 1
4 .. 11	3 .. 10	3	2	1 .. 3	0 .. 2
5 .. 12	4 .. 11	4	3	1 .. 4	0 .. 3
6 .. 13	5 .. 12	5	4	1 .. 4	0 .. 3
7 .. 14	6 .. 13	6	5	1 .. 4	0 .. 3
8 .. 15	7 .. 14	7	6	1 .. 4	0 .. 3
9 .. 16	8 .. 15	8	7	1 .. 4	0 .. 3

13.4.4 Modes of Operation

13.4.4.1 Normal System Operating Modes

The MSCAN module behaves as described within this specification in all normal system operating modes. Write restrictions exist for some registers.

Each channel counter can be read at anytime without affecting the count or the operation of the PWM channel.

Any value written to the counter causes the counter to reset to $00, the counter direction to be set to up, the immediate load of both duty and period registers with values from the buffers, and the output to change according to the polarity bit. When the channel is disabled (PWMEx = 0), the counter stops. When a channel becomes enabled (PWMEx = 1), the associated PWM counter continues from the count in the PWMCNTx register. This allows the waveform to continue where it left off when the channel is re-enabled. When the channel is disabled, writing “0” to the period register will cause the counter to reset on the next selected clock.

NOTE

If the user wants to start a new “clean” PWM waveform without any “history” from the old waveform, the user must write to channel counter (PWMCNTx) prior to enabling the PWM channel (PWMEx = 1).

Generally, writes to the counter are done prior to enabling a channel in order to start from a known state. However, writing a counter can also be done while the PWM channel is enabled (counting). The effect is similar to writing the counter when the channel is disabled, except that the new period is started immediately with the output set according to the polarity bit.

NOTE

Writing to the counter while the channel is enabled can cause an irregular PWM cycle to occur.

The counter is cleared at the end of the effective period (see Section 17.4.2.5, “Left Aligned Outputs” and Section 17.4.2.6, “Center Aligned Outputs” for more details).

Table 17-12. PWM Timer Counter Conditions

Counter Clears ($00)	Counter Counts	Counter Stops
When PWMCNTx register written to any value	When PWM channel is enabled (PWMEx = 1). Counts from last value in PWMCNTx.	When PWM channel is disabled (PWMEx = 0)
Effective period ends		

17.4.2.5 Left Aligned Outputs

The PWM timer provides the choice of two types of outputs, left aligned or center aligned. They are selected with the CAEx bits in the PWMCAE register. If the CAEx bit is cleared (CAEx = 0), the corresponding PWM output will be left aligned.

In left aligned output mode, the 8-bit counter is configured as an up counter only. It compares to two registers, a duty register and a period register as shown in the block diagram in Figure 17-16. When the PWM counter matches the duty register the output flip-flop changes state causing the PWM waveform to also change state. A match between the PWM counter and the period register resets the counter and the output flip-flop, as shown in Figure 17-16, as well as performing a load from the double buffer period and duty register to the associated registers, as described in Section 17.4.2.3, “PWM Period and Duty”. The counter counts from 0 to the value in the period register – 1.

18.4.5 Transmitter

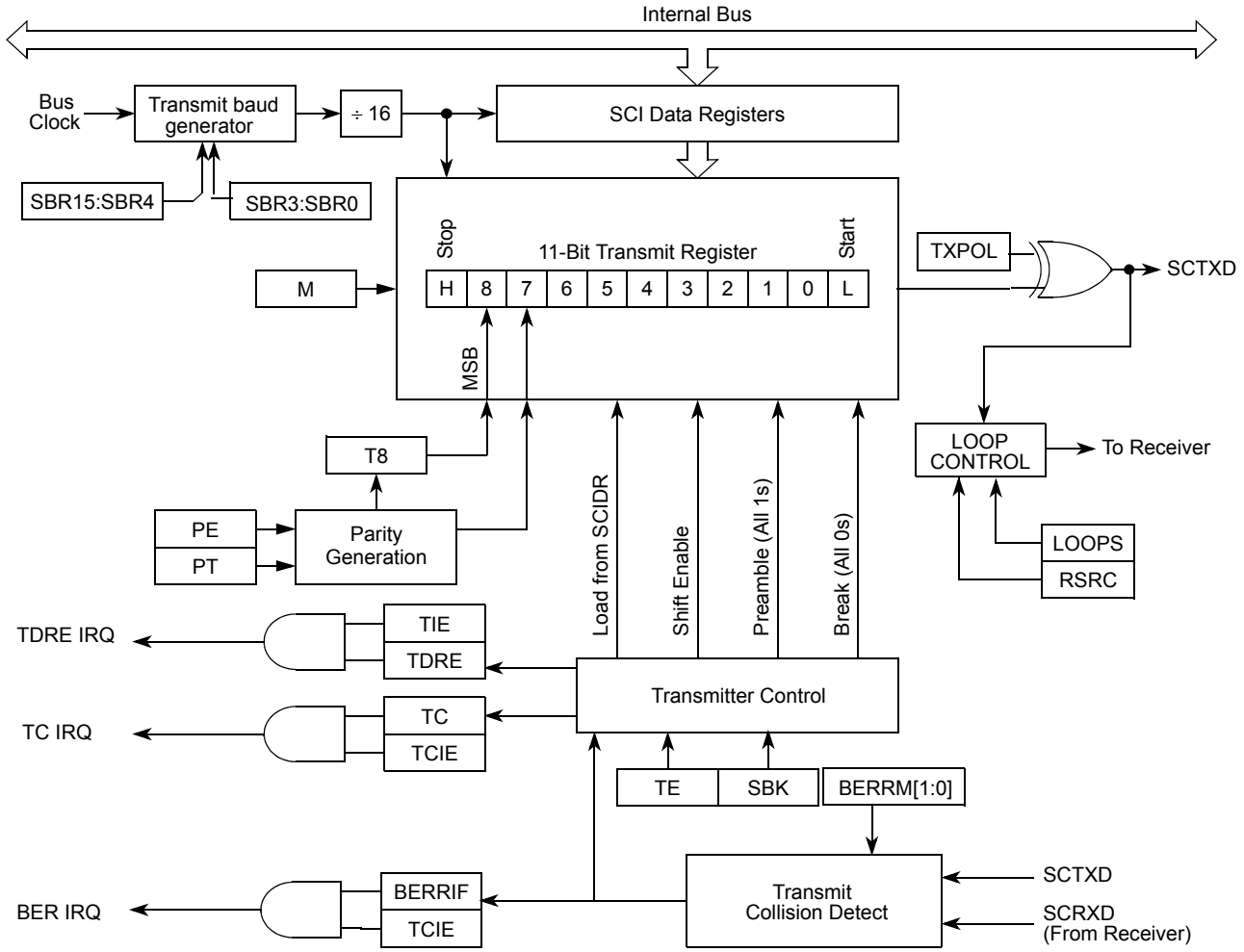


Figure 18-16. Transmitter Block Diagram

18.4.5.1 Transmitter Character Length

The SCI transmitter can accommodate either 8-bit or 9-bit data characters. The state of the M bit in SCI control register 1 (SCICR1) determines the length of data characters. When transmitting 9-bit data, bit T8 in SCI data register high (SCIDRH) is the ninth bit (bit 8).

18.4.5.2 Character Transmission

To transmit data, the MCU writes the data bits to the SCI data registers (SCIDRH/SCIDRL), which in turn are transferred to the transmitter shift register. The transmit shift register then shifts a frame out through the TXD pin, after it has prefaced them with a start bit and appended them with a stop bit. The SCI data registers (SCIDRH and SCIDRL) are the write-only buffers between the internal data bus and the transmit shift register.

20.2.2 IIC_SDA — Serial Data Line Pin

This is the bidirectional serial data line (SDA) of the module, compatible to the IIC bus specification.

20.3 Memory Map and Register Definition

This section provides a detailed description of all memory and registers for the IIC module.

20.3.1 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 IBAD	R	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	0
	W								
0x0001 IBFD	R	IBC7	IBC6	IBC5	IBC4	IBC3	IBC2	IBC1	IBC0
	W								
0x0002 IBCR	R	IBEN	IBIE	MS/$\overline{SL}$	Tx/$\overline{Rx}$	TXAK	0	0	IBSWAI
	W						RSTA		
0x0003 IBSR	R	TCF	IAAS	IBB	IBAL	0	SRW	IBIF	RXAK
	W								
0x0004 IBDR	R	D7	D6	D5	D4	D3	D2	D1	D0
	W								
0x0005 IBCR2	R	GCEN	ADTYPE	0	0	0	ADR10	ADR9	ADR8
	W								

= Unimplemented or Reserved

Figure 20-2. IIC Register Summary

21.3.2.6 LIN Status Register (LPSR)

Module Base + Address 0x0005 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	LPDT	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 21-8. LIN Status Register (LPSR)

[1] Read: Anytime
Write: Never, writes to this register have no effect

Table 21-7. LPSR Field Description

Field	Description
7 LPDT	**LIN Transmitter TxD-dominant timeout Status Bit** — This read-only bit signals that the LPTxD pin is still dominant after a TxD-dominant timeout. As long as the LPTxD is dominant after the timeout the LIN transmitter is shut down and the LPTDIF is set again after attempting to clear it. 0 If there was a TxD-dominant timeout, LPTxD has ceased to be dominant after the timeout. 1 LPTxD is still dominant after a TxD-dominant timeout.

21.3.2.7 LIN Interrupt Enable Register (LPIE)

Module Base + Address 0x0006 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	LPDTIE	LPOCIE	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 21-9. LIN Interrupt Enable Register (LPIE)

[1] Read: Anytime
Write: Anytime

- Automated program and erase algorithm with verify and generation of ECC parity bits
- Fast sector erase and phrase program operation
- Ability to read the P-Flash memory while programming a word in the EEPROM memory
- Flexible protection scheme to prevent accidental program or erase of P-Flash memory

22.1.2.2 EEPROM Features

- The EEPROM memory is composed of one Flash block divided into sectors of 4 bytes
- Single bit fault correction and double bit fault detection within a word during read operations
- Automated program and erase algorithm with verify and generation of ECC parity bits
- Fast sector erase and word program operation
- Protection scheme to prevent accidental program or erase of EEPROM memory
- Ability to program up to four words in a burst sequence

22.1.2.3 Other Flash Module Features

- No external high-voltage power supply required for Flash memory program and erase operations
- Interrupt generation on Flash command completion and Flash error detection
- Security mechanism to prevent unauthorized access to the Flash memory

22.1.3 Block Diagram

The block diagrams of the Flash modules are shown in the following figures.

Table 22-11. FCCOBIX Field Descriptions

Field	Description
2–0 CCOBIX[1:0]	**Common Command Register Index**— The CCOBIX bits are used to indicate how many words of the FCCOB register array are being read or written to. See <st-blue>22.3.2.13 Flash Common Command Object Registers (FCCOB),” for more details.

22.3.2.4 Flash Protection Status Register (FPSTAT)

This Flash register holds the status of the Protection Override feature.

Offset Module Base + 0x0003

	7	6	5	4	3	2	1	0
R	FPOVRD	0	0	0	0	0	0	WSTATACK
W								
Reset	0	0	0	0	0	0	0	1

= Unimplemented or Reserved

Figure 22-8. Flash Protection Status Register (FPSTAT)

All bits in the FPSTAT register are readable but are not writable.

Table 22-12. FPSTAT Field Descriptions

Field	Description
7 FPOVRD	**Flash Protection Override Status** — The FPOVRD bit indicates if the Protection Override feature is currently enabled. See Section 22.4.7.17, “Protection Override Command” for more details. 0 Protection is not overridden 1 Protection is overridden, contents of registers FPROT and/or DFPROT (and effective protection limits determined by their current contents) were determined during execution of command Protection Override
0 WSTATACK	**Wait-State Switch Acknowledge** — The WSTATACK bit indicates that the wait-state configuration is effectively set according to the value configured on bits FCNFG[WSTAT] (see Section 22.3.2.5, “Flash Configuration Register (FCNFG)”). WSTATACK bit is cleared when a change in FCNFG[WSTAT] is requested by writing to those bits, and is set when the Flash has effectively switched to the new wait-state configuration. The application must check the status of WSTATACK bit to make sure it reads as 1 before changing the frequency setup (see Section 22.4.3, “Flash Block Read Access”). 0 Wait-State switch is pending, Flash reads are still happening according to the previous value of FCNFG[WSTAT] 1 Wait-State switch is complete, Flash reads are already working according to the value set on FCNFG[WSTAT]

22.3.2.5 Flash Configuration Register (FCNFG)

The FCNFG register enables the Flash command complete interrupt, control generation of wait-states and forces ECC faults on Flash array read access from the CPU.

maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level.

Table A-3. Absolute Maximum Ratings[1]

Num	Rating	Symbol	Min	Max	Unit
1	Voltage regulator and LINPHY supply voltage	V_{SUP}	-0.3	42	V
2	DC voltage on LIN	V_{LIN}	-32	42	V
3	Voltage Regulator Ballast Connection	V_{BCTL}	-0.3	42	V
4	Supplies VDDA, VDDX	V_{VDDACX}	-0.3	6	V
5	Voltage difference V_{DDX} to V_{DDA}[2]	Δ_{VDDX}	–0.3	0.3	V
6	Voltage difference V_{SSX} to V_{SSA}	Δ_{VSSX}	–0.3	0.3	V
7	Digital I/O input voltage	V_{IN}	–0.3	6.0	V
8	HVI PL0 input voltage	V_{Lx}	–27	42.0	V
9	EXTAL, XTAL [3]	V_{ILV}	–0.3	2.16	V
10	TEST input	V_{TEST}	–0.3	10.0	V
11	Instantaneous maximum current Single pin limit for all digital I/O pins[4]	I_D	–25	+25	mA
12	Continuous current on LIN	I_{LIN}		± 200 [5]	mA
13	Instantaneous maximum current on PP7	I_{PP7}	–80	+25	mA
14	Instantaneous maximum current on PP1, PP3[6] and PP5[6]	I_{PP135}	–30	+80	mA
15	Instantaneous maximum current Single pin limit for EXTAL, XTAL	I_{DL}	–25	+25	mA
16	Storage temperature range	T_{stg}	–65	155	°C

1 Beyond absolute maximum ratings device might be damaged.

2 VDDX and VDDA must be shorted

3 EXTAL, XTAL pins configured for external oscillator operation only

4 All digital I/O pins are internally clamped to V_{SSX} and V_{DDX}, or V_{SSA} and V_{DDA}.

5 The current on the LIN pin is internally limited. Therefore, it should not be possible to reach the 200mA anyway.

6 only applicable for PP3 and PP5 if pin VSSX2 is available

A.1.4 ESD Protection and Latch-up Immunity

All ESD testing is in conformity with CDF-AEC-Q100 stress test qualification for automotive grade integrated circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM) and the Charged-Device Model.

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

O.11 0x05C0-0x05FF TIM0 (continued)

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x05D7	TIM0TC3L	R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x05D8	TIM0TC4H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x05D9	TIM0TC4L	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x05DA	TIM0TC5H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x05DB	TIM0TC5L	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x05DC– 0x05EB	Reserved	R W								
0x05EC	TIM0OCPD	R W	RESERVED	RESERVED	OCPD5	OCPD4	OCPD3	OCPD2	OCPD1	OCPD0
0x05ED	Reserved	R W								
0x05EE	TIM0PTPSR	R W	PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0
0x05EF	Reserved	R W								

O.12 0x0600-0x063F ADC0

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0600	ADC0CTL_0	R W	ADC_EN	ADC_SR	FRZ_MOD	SWAI	ACC_CFG[1:0]		STR_SEQA	MOD_CFG
0x0601	ADC0CTL_1	R W	CSL_BMOD	RVL_BMOD	SMOD_ACC	AUT_RSTA	0	0	0	0
0x0602	ADC0STS	R W	CSL_SEL	RVL_SEL	DBECC_ERR	Reserved	READY	0	0	0
0x0603	ADC0TIM	R W	0	PRS[6:0]						
0x0604	ADC0FMT	R W	DJM	0	0	0	0	SRES[2:0]		
0x0605	ADC0FLWCTL	R W	SEQA	TRIG	RSTA	LDOK	0	0	0	0
0x0606	ADC0EIE	R W	IA_EIE	CMD_EIE	EOL_EIE	Reserved	TRIG_EIE	RSTAR_EIE	LDOK_EIE	0
0x0607	ADC0IE	R W	SEQAD_IE	CONIF_OIE	Reserved	0	0	0	0	0