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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	37
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 11x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	49-UFBGA, WLCSP
Supplier Device Package	49-WLCSP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f302c8y6tr

List of tables

2 Description

The STM32F302x6/8 family is based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 72 MHz and embedding a floating point unit (FPU). The family incorporates high-speed embedded memories (up to 64 Kbytes of Flash memory, 16 Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The devices offer a fast 12-bit ADC (5 Msps), three comparators, an operational amplifier, up to 18 capacitive sensing channels, one DAC channel, a low-power RTC, one general-purpose 32-bit timer, one timer dedicated to motor control, and up to three general-purpose 16-bit timers, and one timer to drive the DAC. They also feature standard and advanced communication interfaces: three I^2Cs, up to three USARTs, up to two SPIs with multiplexed full-duplex I2S, a USB FS device, a CAN, and an infrared transmitter.

The STM32F302x6/8 family operates in the –40 to +85°C and –40 to +105°C temperature ranges from at a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F302x6/8 family offers devices in 32-, 48-, 49- and 64-pin packages.

The set of included peripherals changes with the device chosen.

3 Functional overview

3.1 ARM® Cortex®-M4 core with FPU, embedded Flash and SRAM

The ARM® Cortex®-M4 processor with FPU is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M4 32-bit RISC processor with FPU features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution. Its single-precision FPU speeds up software development by using metalanguage development tools while avoiding saturation.

With its embedded ARM core, the STM32F302x6/8 family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the STM32F302x6/8 family devices.

3.2 Memories

3.2.1 Embedded Flash memory

All STM32F302x6/8 devices feature up to 64 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

3.2.2 Embedded SRAM

STM32F302x6/8 devices feature 16 Kbytes of embedded SRAM.

3.3 Boot modes

At startup, BOOT0 pin and BOOT1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART2 (PA2/PA3) or USB (PA11/PA12) through DFU (device firmware upgrade).

3.11.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC1_IN17. As the V_{BAT} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

3.12 Digital-to-analog converter (DAC)

One 12-bit buffered DAC channel (DAC1_OUT1) can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- One DAC output channel
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- DMA capability
- External triggers for conversion

3.13 Operational amplifier (OPAMP)

The STM32F302x6/8 devices embed one operational amplifier with external or internal follower routing and PGA capability (or even amplifier and filter capability with external components). When the operational amplifier is selected, an external ADC channel is used to enable output measurement.

The operational amplifier features:

- 8.2 MHz bandwidth
- 0.5 mA output capability
- Rail-to-rail input/output
- In PGA mode, the gain can be programmed to be 2, 4, 8 or 16.

3.17 Inter-integrated circuit interfaces (I^2C)

The devices feature three I^2C bus interfaces which can operate in multimaster and slave mode. Each I2C interface can support standard (up to 100 kHz), fast (up to 400 kHz) and fast mode + (up to 1 MHz) modes.

All I^2C interfaces support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

Table 5. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, it provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. It also has a clock domain independent from the CPU clock, allowing the I2Cx (x=1,3) to wake up the MCU from Stop mode on address match.

The I2C interfaces can be served by the DMA controller.

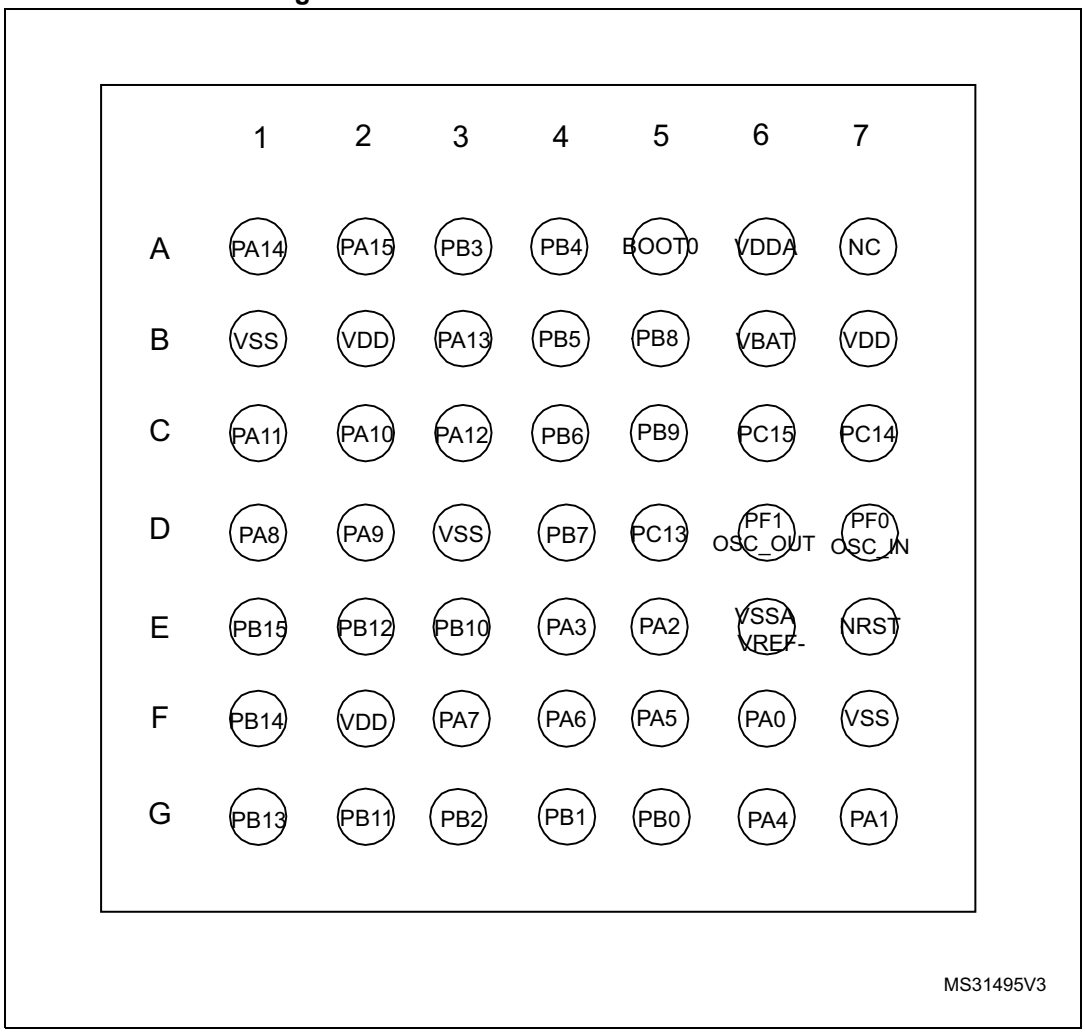
Refer to *Table 6* for the features available in I2C1, I2C2 and I2C3.

Table 6. STM32F302x6/8 I^2C implementation

I2C features(1)	I2C1	I2C2	I2C3
7-bit addressing mode	X	X	X
10-bit addressing mode	X	X	X
Standard mode (up to 100 kbit/s)	X	X	X
Fast mode (up to 400 kbit/s)	X	X	X
Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X	X
Independent clock	X	X	X
SMBus	X	X	X
Wakeup from STOP	X	X	X

1. X = supported.

Figure 7. STM32F302x6/8 WLCSP49 ballout



1. The above figure shows the package top view.
2. NC: Not connected.

Table 12. STM32F302x6/8 pin definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN32	WLCSP49	LQFP48	LQFP64						
7	F6	10	14	PA0 -TAMPER2-WKUP1	I/O	TTa	(2)	TIM2_CH1/TIM2_ETR, TSC_G1_IO1, USART2_CTS, EVENTOUT	ADC1_IN1, RTC_TAMP2, WKUP1
8	G7	11	15	PA1	I/O	TTa	(2)	RTC_REFIN, TIM2_CH2, TSC_G1_IO2, USART2_RTS_DE, TIM15_CH1N, EVENTOUT	ADC1_IN2
9	E5	12	16	PA2	I/O	TTa	(2)	TIM2_CH3, TSC_G1_IO3, USART2_TX, COMP2_OUT, TIM15_CH1, EVENTOUT	ADC1_IN3, COMP2_INM
10	E4	13	17	PA3	I/O	TTa	(2)	TIM2_CH4, TSC_G1_IO4, USART2_RX, TIM15_CH2, EVENTOUT	ADC1_IN4
-	F7	-	18	VSS_4	S	-	-	-	-
-	F2	-	19	VDD_4	S	-	-	-	-
11	G6	14	20	PA4	I/O	TTa	(2)(3)	TSC_G2_IO1, SPI3_NSS/I2S3_WS, USART2_CK, EVENTOUT	ADC1_IN5, DAC1_OUT1, COMP2_INM, COMP4_INM, COMP6_INM
12	F5	15	21	PA5	I/O	TTa	-	TIM2_CH1/TIM2_ETR, TSC_G2_IO2, EVENTOUT	OPAMP2_VINM
13	F4	16	22	PA6	I/O	TTa	(3)	TIM16_CH1, TSC_G2_IO3, TIM1_BKIN, EVENTOUT	ADC1_IN10, OPAMP2_VOUT
14	F3	17	23	PA7	I/O	TTa	-	TIM17_CH1, TSC_G2_IO4, TIM1_CH1N, EVENTOUT	ADC1_IN15, COMP2_INP, OPAMP2_VINP

Table 12. STM32F302x6/8 pin definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN32	WLCSP49	LQFP48	LQFP64						
-	-	-	24	PC4	I/O	TT	-	EVENTOUT, TIM1_ETR, USART1_TX	
-	-	-	25	PC5	I/O	TTa	-	EVENTOUT, TIM15_BKIN, TSC_G3_IO1, USART1_RX	OPAMP2_VINM
15	G5	18	26	PB0	I/O	TTa	-	TSC_G3_IO2, TIM1_CH2N, EVENTOUT	ADC1_IN11, COMP4_INP, OPAMP2_VINP
-	G4	19	27	PB1	I/O	TTa	-	TSC_G3_IO3, TIM1_CH3N, COMP4_OUT, EVENTOUT	ADC1_IN12
-	G3	20	28	PB2	I/O	TTa	-	TSC_G3_IO4, EVENTOUT	COMP4_INM
-	E3	21	29	PB10	I/O	TT	-	TIM2_CH3, TSC_SYNC, USART3_TX, EVENTOUT	
-	G2	22	30	PB11	I/O	TTa	-	TIM2_CH4, TSC_G6_IO1, USART3_RX, EVENTOUT	ADC1_IN14, COMP6_INP
16	D3	23	31	VSS_2	S	-	-	Digital ground	
17	B2	24	32	VDD_2	S	-	-	Digital power supply	
-	E2	25	33	PB12	I/O	TT	-	TSC_G6_IO2, I2C2_SMBAL, SPI2_NSS/I2S2_WS, TIM1_BKIN, USART3_CK, EVENTOUT	
-	G1	26	34	PB13	I/O	TTa	-	TSC_G6_IO3, SPI2_SCK/I2S2_CK, TIM1_CH1N, USART3_CTS, EVENTOUT	ADC1_IN13

Table 15. Alternate functions for Port C

Port & pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SYS_AF	TIM2/TIM15/ TIM16/TIM17/ EVENT	I2C3/TIM1/TIM2 /TIM15	I2C3/TIM15/ TSC	I2C1/I2C2/TIM1/ TIM16/TIM17	SPI2/I2S2/ SPI3/I2S3 Infrared	SPI2/I2S2/SPI3/ I2S3/TIM1/ Infrared	USART1/ USART2/ USART3/CAN/ GPCOMP6
PC0	-	EVENTOUT	TIM1_CH1	-	-	-	-	-
PC1	-	EVENTOUT	TIM1_CH2	-	-	-	-	-
PC2	-	EVENTOUT	TIM1_CH3	-	-	-	-	-
PC3	-	EVENTOUT	TIM1_CH4	-	-	-	TIM1_BKIN2	-
PC4	-	EVENTOUT	TIM1_ETR	-	-	-	-	USART1_TX
PC5	-	EVENTOUT	TIM15_BKIN	TSC_G3_IO1	-	-	-	USART1_RX
PC6	-	EVENTOUT	-	-	-	-	I2S2_MCK	COMP6_OUT
PC7	-	EVENTOUT	-	-	-	-	I2S3_MCK	-
PC8	-	EVENTOUT	-	-	-	-	-	-
PC9	-	EVENTOUT	-	I2C3_SDA	-	I2SCKIN	-	-
PC10	-	EVENTOUT	-	-	-	-	SPI3_SCK/ I2S3_CK	USART3_TX
PC11	-	EVENTOUT	-	-	-	-	SPI3_MISO/ I2S3ext_SD	USART3_RX
PC12	-	EVENTOUT	-	-	-	-	SPI3_MOSI/ I2S3_SD	USART3_CK
PC13	-	-	-	-	TIM1_CH1N	-	-	-
PC14	-	-	-	-	-	-	-	-
PC15	-	-	-	-	-	-	-	-

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 19: Voltage characteristics*, *Table 20: Current characteristics*, and *Table 21: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 19. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA}, V_{BAT} and V_{DD})	-0.3	4.0	V
V_{DD}–V_{DDA}	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	V
V_{IN}(2)	Input voltage on FT and FTf pins	V_{SS} −0.3	V_{DD} + 4.0	V
	Input voltage on TTa and TT pins	V_{SS} −0.3	4.0	
	Input voltage on any other pin	V_{SS} −0.3	4.0	
	Input voltage on Boot0 pin	0	9	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins(3)	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.12: Electrical sensitivity characteristics*		V

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range. The following relationship must be respected between V_{DDA} and V_{DD}:
V_{DDA} must power on before or at the same time as V_{DD} in the power up sequence.
V_{DDA} must be greater than or equal to V_{DD}.
2. V_{IN} maximum must always be respected. Refer to *Table 20: Current characteristics* for the maximum allowed injected current values.
3. Include V_{REF-} pin.

Table 33. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Run mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash	72 MHz	44.8	24.9	mA
			64 MHz	40.0	22.4	
			48 MHz	30.3	17.1	
			32 MHz	20.7	11.9	
			24 MHz	15.8	9.2	
			16 MHz	10.9	6.5	
			8 MHz	5.7	3.55	
			4 MHz	3.43	3.22	
			2 MHz	2.18	1.53	
			1 MHz	1.56	1.19	
			500 kHz	1.25	0.96	
			125 kHz	0.96	0.84	
I_{DDA} (1) (2)	Supply current in Run mode from V_{DDA} supply		72 MHz	237.1		µA
			64 MHz	208.3		
			48 MHz	154.3		
			32 MHz	105.0		
			24 MHz	81.3		
			16 MHz	57.8		
			8 MHz	1.15		
			4 MHz	1.15		
			2 MHz	1.15		
			1 MHz	1.15		
			500 kHz	1.15		
			125 kHz	1.15		

1. V_{DDA} supervisor is OFF.
2. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.

6.3.6 Wakeup time from low-power mode

The wakeup times given in *Table 37* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep mode: the wakeup event is WFE.
- WKUP1 (PA0) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22*.

Table 37. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ @V_{DD}, V_{DD} = V_{DDA}						Max	Unit
			2.0 V	2.4 V	2.7 V	3 V	3.3 V	3.6 V		
t_{WUSTOP}	Wakeup from Stop mode	Regulator in run mode	4.5	4.2	4.1	4.0	3.8	3.8	4.5	µs
		Regulator in low-power mode	8.2	7.0	6.4	6.0	5.7	5.5	9.0	
$t_{WUSTANDBY}$(1)	Wakeup from Standby mode	LSI and IWDG OFF	72.8	63.4	59.2	56.1	53.1	51.3	103	
$t_{WUSLEEP}$	Wakeup from Sleep mode		6						-	CPU clock cycles

1. Guaranteed by characterization results.

Table 38. Wakeup time using USART(1)

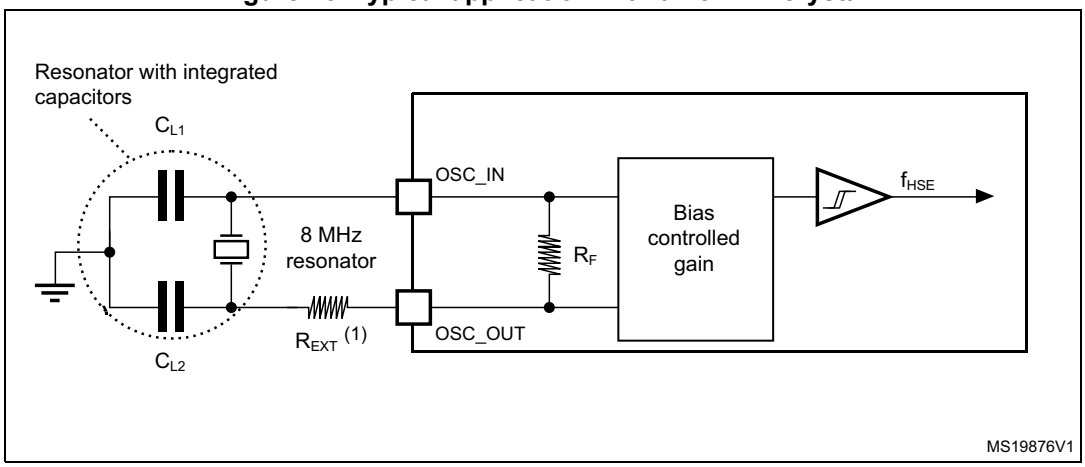
Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$	Wakeup time needed to calculate the maximum USART baud rate allowing to wakeup up from Stop mode when the USART clock source is HSI	Stop mode with main regulator in low-power mode	-	13.125	µs
		Stop mode with main regulator in run mode	-	3.125	

1. Guaranteed by design.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 16*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 16. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

6.3.8 Internal clock source characteristics

The parameters given in *Table 43* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22*.

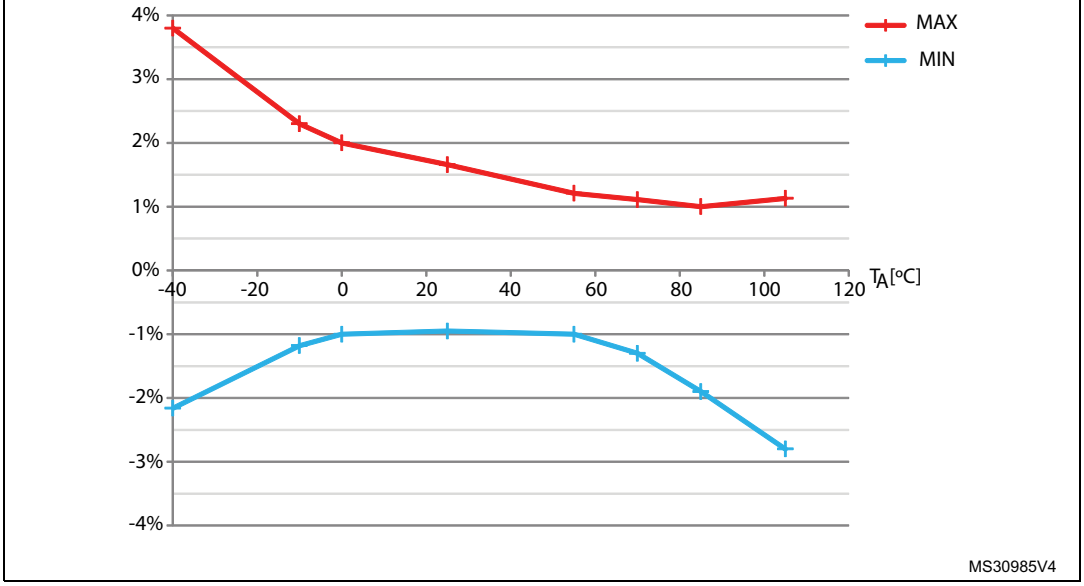
High-speed internal (HSI) RC oscillator

Table 43. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
TRIM	HSI user trimming step	-	-	-	1(2)	%
$DuCy_{(HSI)}$	Duty cycle	-	45(2)	-	55(2)	%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = -40 to 105°C	-2.8(3)	-	3.8(3)	%
		T_A = -10 to 85°C	-1.9(3)	-	2.3(3)	
		T_A = 0 to 85°C	-1.9(3)	-	2(3)	
		T_A = 0 to 70°C	-1.3(3)	-	2(3)	
		T_A = 0 to 55°C	-1(3)	-	2(3)	
		T_A = 25°C(4)	-1	-	1	
$t_{su(HSI)}$	HSI oscillator startup time	-	1(2)	-	2(2)	µs
$I_{DDA(HSI)}$	HSI oscillator power consumption	-	-	80	100(2)	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.
4. Factory calibrated, parts not soldered.

Figure 18. HSI oscillator accuracy characterization results for soldered parts



6.3.10 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 46. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	53.5	60	µs
t_{ERASE}	Page (2 KB) erase time	T_A = –40 to +105 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20	-	40	ms
I_{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA

1. Guaranteed by design.

Table 47. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycles(2) at T_A = 55 °C	20	

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

Table 68. ADC accuracy - limited test conditions(1)(2)

Symbol	Parameter	Conditions			Min (3)	Typ	Max (3)	Unit
ET	Total unadjusted error	ADC clock freq. ≤ 72 MHz Sampling freq. ≤ 5 Msps V_{DDA} = 3.3 V 25°C	Single ended	Fast channel 5.1 Ms	-	±4	±4.5	LSB
				Slow channel 4.8 Ms	-	±5.5	±6	
			Differential	Fast channel 5.1 Ms	-	±3.5	±4	
				Slow channel 4.8 Ms	-	±3.5	±4	
EO	Offset error		Single ended	Fast channel 5.1 Ms	-	±2	±2	
				Slow channel 4.8 Ms	-	±1.5	±2	
			Differential	Fast channel 5.1 Ms	-	±1.5	±2	
				Slow channel 4.8 Ms	-	±1.5	±2	
EG	Gain error		Single ended	Fast channel 5.1 Ms	-	±3	±4	
				Slow channel 4.8 Ms	-	±5	±5.5	
			Differential	Fast channel 5.1 Ms	-	±3	±3	
				Slow channel 4.8 Ms	-	±3	±3.5	
ED	Differential linearity error		Single ended	Fast channel 5.1 Ms	-	±1	±1	
				Slow channel 4.8 Ms	-	±1	±1	
			Differential	Fast channel 5.1 Ms	-	±1	±1	
				Slow channel 4.8 Ms	-	±1	±1	
EL	Integral linearity error		Single ended	Fast channel 5.1 Ms	-	±1.5	±2	
				Slow channel 4.8 Ms	-	±2	±3	
			Differential	Fast channel 5.1 Ms	-	±1.5	±1.5	
				Slow channel 4.8 Ms	-	±1.5	±2	
ENOB (4)	Effective number of bits		Single ended	Fast channel 5.1 Ms	10.8	10.8	-	bit
				Slow channel 4.8 Ms	10.8	10.8	-	
			Differential	Fast channel 5.1 Ms	11.2	11.3	-	
				Slow channel 4.8 Ms	11.2	11.3	-	
SINAD (4)	Signal-to-noise and distortion ratio		Single ended	Fast channel 5.1 Ms	66	67	-	dB
				Slow channel 4.8 Ms	66	67	-	
			Differential	Fast channel 5.1 Ms	69	70	-	
				Slow channel 4.8 Ms	69	70	-	

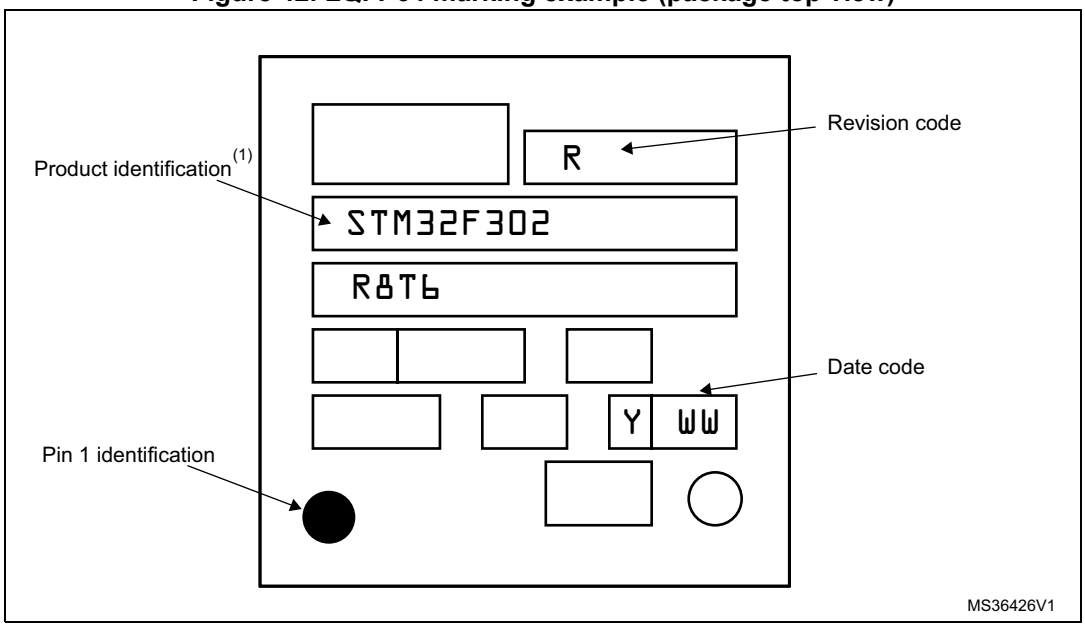
7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 42. LQFP64 marking example (package top view)



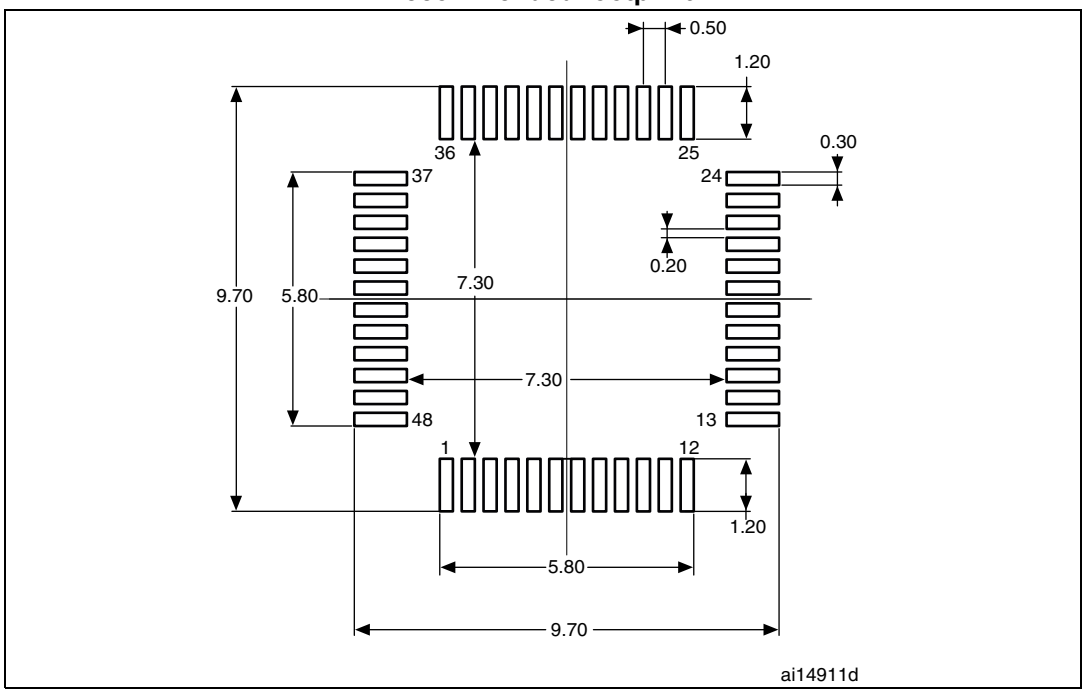
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Table 80. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 44. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.