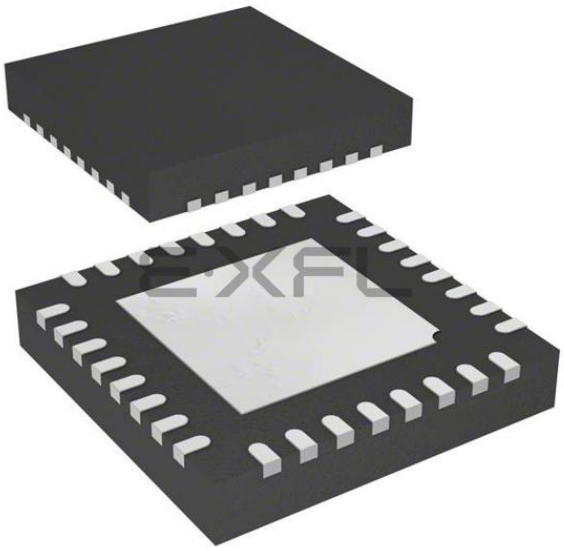

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f302k6u6

Contents

mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

Refer to *Table 8* for the features available in SPI2 and SPI3.

Table 8. STM32F302x6/8 SPI/I2S implementation

SPI features(1)	SPI2	SPI3
Hardware CRC calculation	X	X
Rx/Tx FIFO	X	X
NSS pulse mode	X	X
I2S mode	X	X
TI mode	X	X

1. X = supported.

3.20 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

3.21 Universal serial bus (USB)

The STM32F302x6 STM32F302x8 embeds a full-speed USB device peripheral compliant with the USB specification version 2.0. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up-to 1 KB (the last 256 bytes are used for CAN peripheral if enabled) and suspend/resume support. It requires a precise 48 MHz clock which is generated from the internal main PLL (the clock source must use an HSE crystal oscillator).

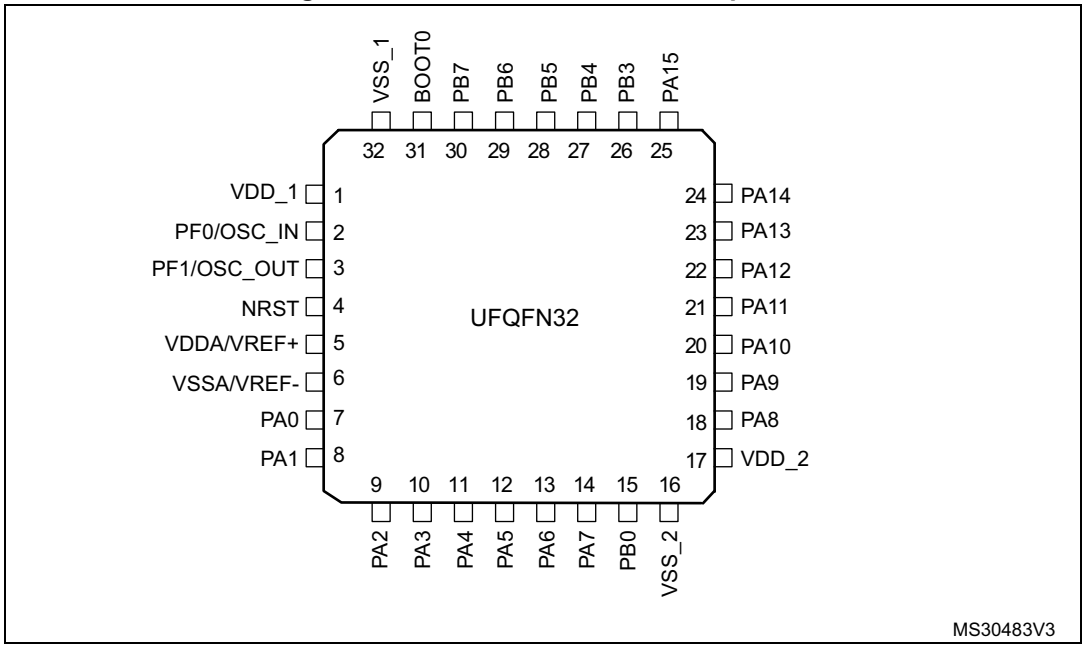
3.22 Touch sensing controller (TSC)

The STM32F302x6/8 devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 18 capacitive sensing channels distributed over 6 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (for example glass, plastic). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

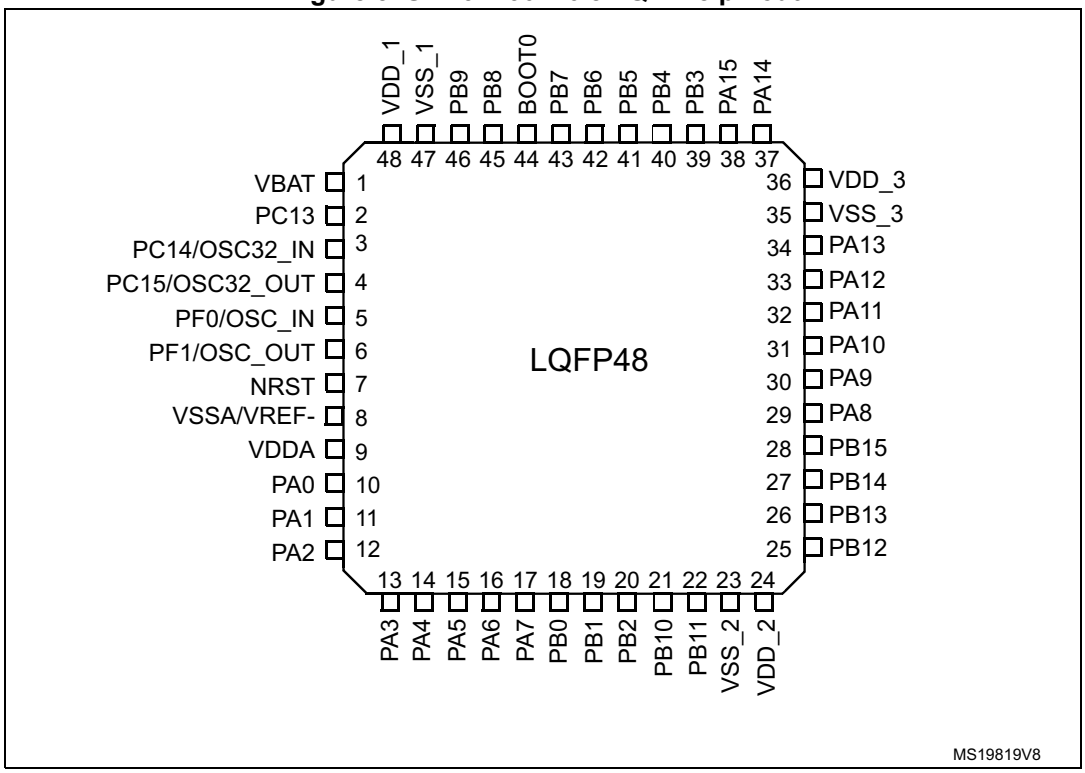
4 Pinouts and pin description

Figure 4. STM32F302x6/8 UFQFN32 pinout



1. The above figure shows the package top view.

Figure 5. STM32F302x6/8 LQFP48 pinout



1. The above figure shows the package top view.

Table 20. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all VDD_x power lines (source)	130	mA
ΣI_{VSS}	Total current out of sum of all VSS_x ground lines (sink)	-130	
I_{VDD}	Maximum current into each V_{DD_x} power line (source)(1)	100	
I_{VSS}	Maximum current out of each V_{SS_x} ground line (sink)(1)	-100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins(2)	80	
	Total output current sourced by sum of all IOs and control pins(2)	-80	
$I_{INJ(PIN)}$	Injected current on TT, FT, FTf and B pins(3)	-5/+0	
	Injected current on TC and RST pin(4)	+/-5	
	Injected current on TTa pins(5)	+/-5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	+/-25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS} and V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins.The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 19: Voltage characteristics* for the maximum allowed input voltage values.
5. A positive injection is induced by $V_{IN} > V_{DDA}$ while a negative injection is induced by $V_{IN} < V_{SS}$. I_{INJ}(PIN) must never be exceeded. Refer also to *Table 19: Voltage characteristics* for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note (2) below *Table 68*.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 21. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

Table 33. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Run mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash	72 MHz	44.8	24.9	mA
			64 MHz	40.0	22.4	
			48 MHz	30.3	17.1	
			32 MHz	20.7	11.9	
			24 MHz	15.8	9.2	
			16 MHz	10.9	6.5	
			8 MHz	5.7	3.55	
			4 MHz	3.43	3.22	
			2 MHz	2.18	1.53	
			1 MHz	1.56	1.19	
			500 kHz	1.25	0.96	
			125 kHz	0.96	0.84	
I_{DDA} (1) (2)	Supply current in Run mode from V_{DDA} supply		72 MHz	237.1		µA
			64 MHz	208.3		
			48 MHz	154.3		
			32 MHz	105.0		
			24 MHz	81.3		
			16 MHz	57.8		
			8 MHz	1.15		
			4 MHz	1.15		
			2 MHz	1.15		
			1 MHz	1.15		
			500 kHz	1.15		
			125 kHz	1.15		

1. V_{DDA} supervisor is OFF.
2. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.

Low-speed external user clock generated from an external source

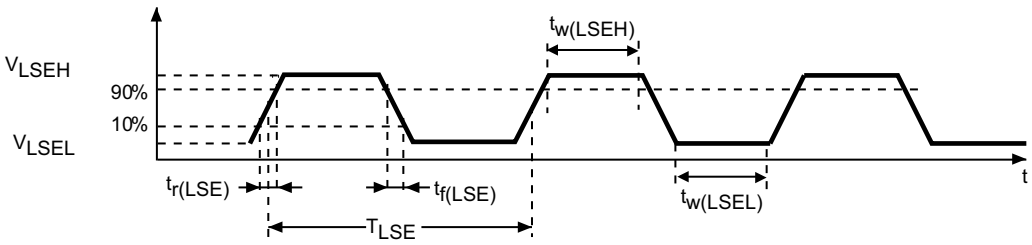
In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 15*

Table 40. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	

1. Guaranteed by design.

Figure 15. Low-speed external clock source AC timing diagram



6.3.10 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 46. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	53.5	60	µs
t_{ERASE}	Page (2 KB) erase time	T_A = –40 to +105 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20	-	40	ms
I_{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA

1. Guaranteed by design.

Table 47. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycles(2) at T_A = 55 °C	20	

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 48*. They are based on the EMS levels and classes defined in application note AN1709.

Table 48. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP64, T_A = +25°C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP64, T_A = +25°C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 49. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/72 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP64 package compliant with IEC 61967-2	0.1 to 30 MHz	5	dBµV
			30 to 130 MHz	6	
			130 MHz to 1GHz	28	
			SAE EMI Level	4	-

6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 50. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Packages	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	All	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1	LQFP64, WLCSP49	C3	250	V
			All other	C4	500	

1. Guaranteed by characterization results.

SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 61* for SPI or in *Table 62* for I²S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 22*.

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 61. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	18	MHz
		Slave mode	-	-	18	
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	0	-	-	
		Slave mode	1	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	6.5	-	-	
$t_{h(SI)}$		Slave mode	2.5	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	8	-	40	
$t_{dis(SO)}$	Data output disable time	Slave mode	8	-	14	
$t_{v(SO)}$	Data output valid time	Slave mode	-	12	27	
$t_{v(MO)}$		Master mode	-	1.5	4	
$t_{h(SO)}$	Data output hold time	Slave mode	7.5	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. Guaranteed by characterization results.

6.3.18 ADC characteristics

Unless otherwise specified, the parameters given in *Table 66* to *Table 68* are guaranteed by design, with conditions summarized in *Table 22*.

Table 66. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC	-	2	-	3.6	V
I_{DDA}	ADC current consumption (see *Figure 31*)	Single-ended mode, 5 MSPS	-	1011.3	1172.0	µA
		Single-ended mode, 1 MSPS	-	214.7	322.3	
		Single-ended mode, 200 KSPS	-	54.7	81.1	
		Differential mode, 5 MSPS	-	1061.5	1243.6	
		Differential mode, 1 MSPS	-	246.6	337.6	
		Differential mode, 200 KSPS	-	56.4	83.0	
f_{ADC}	ADC clock frequency	-	0.14	-	72	MHz
f_S(1)	Sampling rate	Resolution = 12 bits, Fast Channel	0.01	-	5.14	MSPS
		Resolution = 10 bits, Fast Channel	0.012	-	6	
		Resolution = 8 bits, Fast Channel	0.014	-	7.2	
		Resolution = 6 bits, Fast Channel	0.0175	-	9	
f_{TRIG}(1)	External trigger frequency	f_{ADC} = 72 MHz Resolution = 12 bits	-	-	5.14	MHz
		Resolution = 12 bits	-	-	14	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0	-	V_{DDA}	V
R_{AIN}(1)	External input impedance	-	-	-	100	kΩ

Table 68. ADC accuracy - limited test conditions(1)(2) (continued)

Symbol	Parameter	Conditions			Min (3)	Typ	Max (3)	Unit
SNR(4)	Signal-to-noise ratio	ADC clock freq. ≤ 72 MHz Sampling freq ≤ 5 Msps V_{DDA} = 3.3 V 25°C	Single ended	Fast channel 5.1 Ms	66	67	-	dB
				Slow channel 4.8 Ms	66	67	-	
			Differential	Fast channel 5.1 Ms	69	70	-	
				Slow channel 4.8 Ms	69	70	-	
THD(4)	Total harmonic distortion		Single ended	Fast channel 5.1 Ms	-	-80	-80	
				Slow channel 4.8 Ms	-	-78	-77	
			Differential	Fast channel 5.1 Ms	-	-83	-82	
				Slow channel 4.8 Ms	-	-81	-80	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.14* does not affect the ADC accuracy.
3. Guaranteed by characterization results.
4. Value measured with a –0.5dB Full Scale 50kHz sine wave input signal.

Table 72. Comparator characteristics(1)(2) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{S_SC}	V_{REFINT} scaler startup time from power down	V_{REFINT} scaler activation after device power on	-	-	1(3)	s
		Next activations	-	-	0.2	ms
t_{START}	Comparator startup time	$V_{DDA} \geq 2.7$ V	-	-	4	µs
		$V_{DDA} < 2.7$ V	-	-	10	
t_D	Propagation delay for 200 mV step with 100 mV overdrive	$V_{DDA} \geq 2.7$ V	-	25	28	ns
		$V_{DDA} < 2.7$ V	-	28	30	
	Propagation delay for full range step with 100 mV overdrive	$V_{DDA} \geq 2.7$ V	-	32	35	
		$V_{DDA} < 2.7$ V	-	35	40	
V_{OFFSET}	Comparator offset error	$V_{DDA} \geq 2.7$ V	-	±5	±10	mV
		$V_{DDA} < 2.7$ V	-	-	±25	
TV_{OFFSET}	Total offset variation	Full temperature range	-	-	3	mV
$I_{DD(COMP)}$	COMP current consumption	-	-	400	600	µA

1. Guaranteed by design.
2. The comparators do not have built-in hysteresis.
3. For more details and conditions, see *Figure 35: Maximum VREFINT scaler startup time from power down*.

Figure 35. Maximum V_{REFINT} scaler startup time from power down

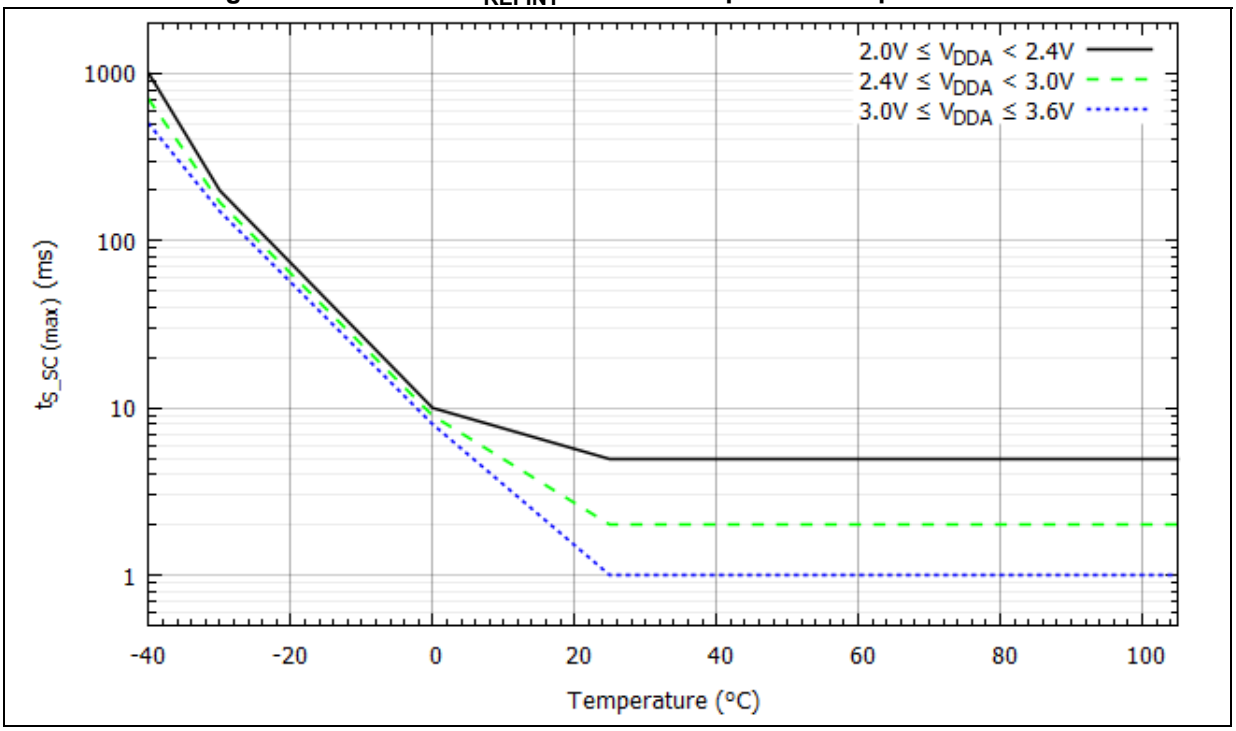


Figure 36. OPAMP Voltage Noise versus Frequency

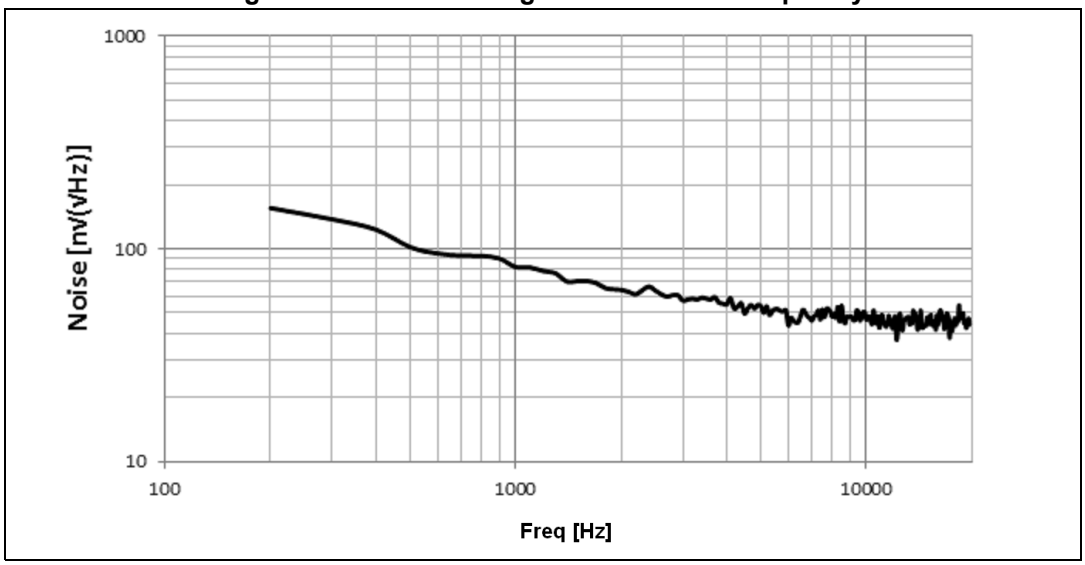
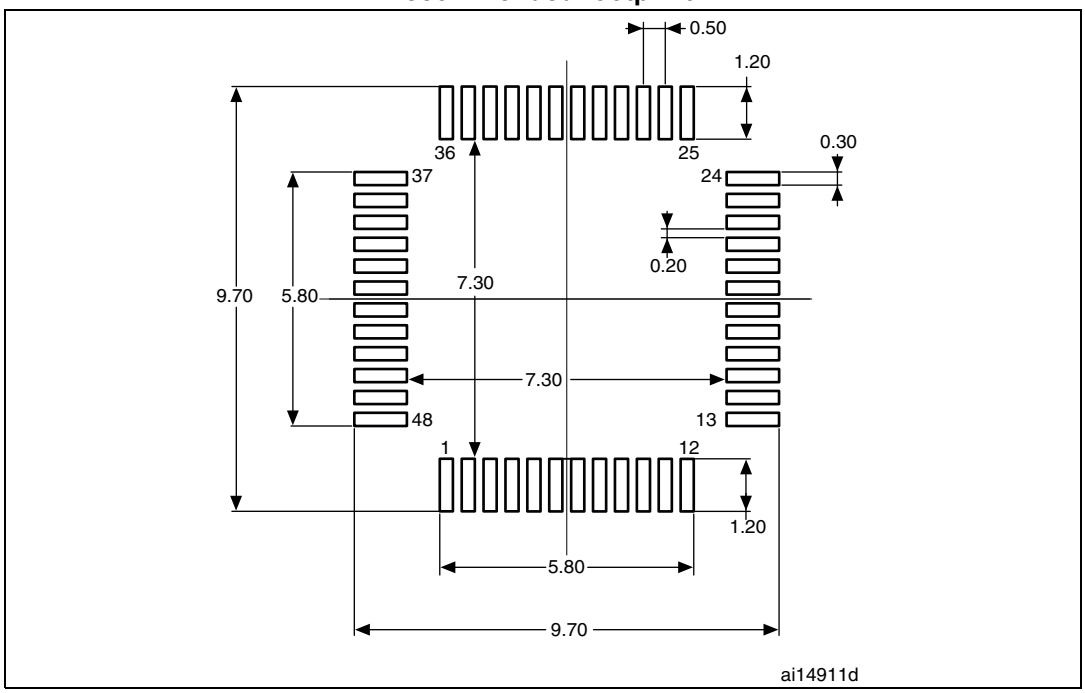


Table 80. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 44. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Table 84. Document revision history (continued)

Date	Revision	Changes
10-Feb-2015	4	Updated: – the values for External clock (HSE bypass) at 48 MHz in *Table 28: Typical and maximum current consumption from VDD supply at VDD = 3.6V* – *Table 41: HSE oscillator characteristics* – *Table 46: Flash memory characteristics* – *Table 72: Comparator characteristics* Added: – *Figure 35: Maximum VREFINT scaler startup time from power down*
04-Jun-2015	5	Updated: – AF9 value for PA1, PA3 and PA9 in *Table 13: Alternate functions for Port A*, – the structure of *Section 7: Package information*.
22-Jul-2016	6	Updated footnotes on: – All document's tables by removing the "not tested in production" specification – *Table 12: STM32F302x6/8 pin definitions* – *Table 19: Voltage characteristics* – *Table 72: Comparator characteristics* – *Figure 4: STM32F302x6/8 UFQFN32 pinout* – *Figure 5: STM32F302x6/8 LQFP48 pinout* – *Figure 6: STM32F302x6/8 LQFP64 pinout* – *Figure 7: STM32F302x6/8 WLCSP49 ballout* – *Figure 24: Recommended NRST pin protection* – *Figure 46: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline* Updated tables: – Updated V_{REFINT} line on *Table 26: Embedded internal reference voltage* – Updated "Conditions" column on *Table 42: LSE oscillator characteristics (fLSE = 32.768 kHz)* – Added CMIR and t_{STAB} lines on *Table 66: ADC characteristics* – Updated R_{LOAD} line on *Table 71: DAC characteristics* – Updated VOH_{SAT} and VOL_{SAT} lines on *Table 73: Operational amplifier characteristics* Updated figures: – *Figure 2: Clock tree* – *Figure 7: STM32F302x6/8 WLCSP49 ballout* – *Figure 21: Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port* – *Figure 24: Recommended NRST pin protection* Added: – *Table 38: Wakeup time using USART* Updated name of *Section 8: Ordering information*