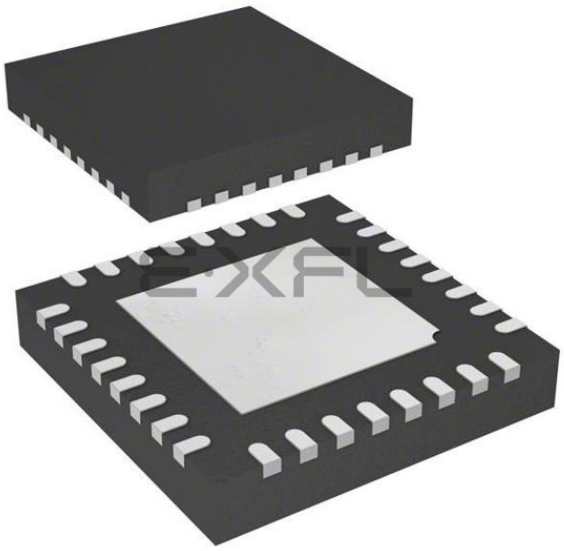

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	24
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f302k8u6

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F302x6/8 microcontrollers.

This datasheet should be read in conjunction with the STM32F302xB/C/D/E and STM32F302x6/8 advanced ARM®-based 32-bit MCUs reference manual (RM0365). The reference manual is available from the STMicroelectronics website *www.st.com*.

For information on the ARM® Cortex®-M4 core, please refer to the Cortex®-M4 Technical Reference Manual, available from ARM website www.arm.com.

2 Description

The STM32F302x6/8 family is based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 72 MHz and embedding a floating point unit (FPU). The family incorporates high-speed embedded memories (up to 64 Kbytes of Flash memory, 16 Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

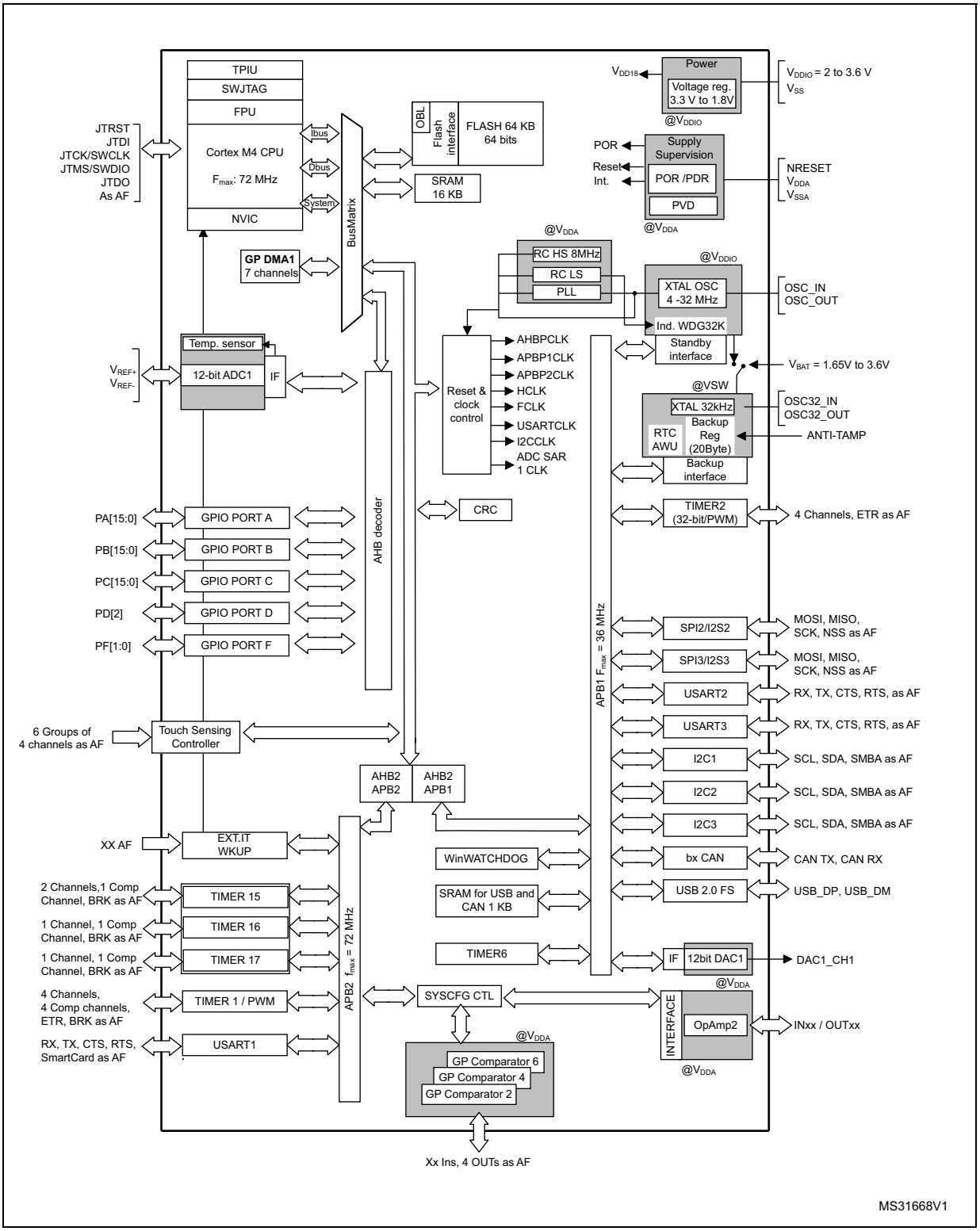
The devices offer a fast 12-bit ADC (5 Msps), three comparators, an operational amplifier, up to 18 capacitive sensing channels, one DAC channel, a low-power RTC, one general-purpose 32-bit timer, one timer dedicated to motor control, and up to three general-purpose 16-bit timers, and one timer to drive the DAC. They also feature standard and advanced communication interfaces: three I^2Cs, up to three USARTs, up to two SPIs with multiplexed full-duplex I2S, a USB FS device, a CAN, and an infrared transmitter.

The STM32F302x6/8 family operates in the –40 to +85°C and –40 to +105°C temperature ranges from at a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F302x6/8 family offers devices in 32-, 48-, 49- and 64-pin packages.

The set of included peripherals changes with the device chosen.

Figure 1. DS9896 block diagram



1. AF: alternate function on I/O pins.

3 Functional overview

3.1 ARM® Cortex®-M4 core with FPU, embedded Flash and SRAM

The ARM® Cortex®-M4 processor with FPU is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M4 32-bit RISC processor with FPU features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution. Its single-precision FPU speeds up software development by using metalanguage development tools while avoiding saturation.

With its embedded ARM core, the STM32F302x6/8 family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the STM32F302x6/8 family devices.

3.2 Memories

3.2.1 Embedded Flash memory

All STM32F302x6/8 devices feature up to 64 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

3.2.2 Embedded SRAM

STM32F302x6/8 devices feature 16 Kbytes of embedded SRAM.

3.3 Boot modes

At startup, BOOT0 pin and BOOT1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART2 (PA2/PA3) or USB (PA11/PA12) through DFU (device firmware upgrade).

3.4 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

3.5 Power management

3.5.1 Power supply schemes

- V_{SS}, V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. It is provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: external analog power supply for ADC, DAC, comparators, operational amplifier, reset blocks, RCs and PLL. The minimum voltage to be applied to V_{DDA} differs from one analog peripheral to another. *Table 2* provides the summary of the V_{DDA} ranges for analog peripherals. The V_{DDA} voltage level must always be greater than or equal to the V_{DD} voltage level and must be provided first.

Table 2. External analog supply values for analog peripherals

Analog peripheral	Minimum V_{DDA} supply	Maximum V_{DDA} supply
ADC/COMP	2.0 V	3.6 V
DAC/OPAMP	2.4 V	3.6 V

- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

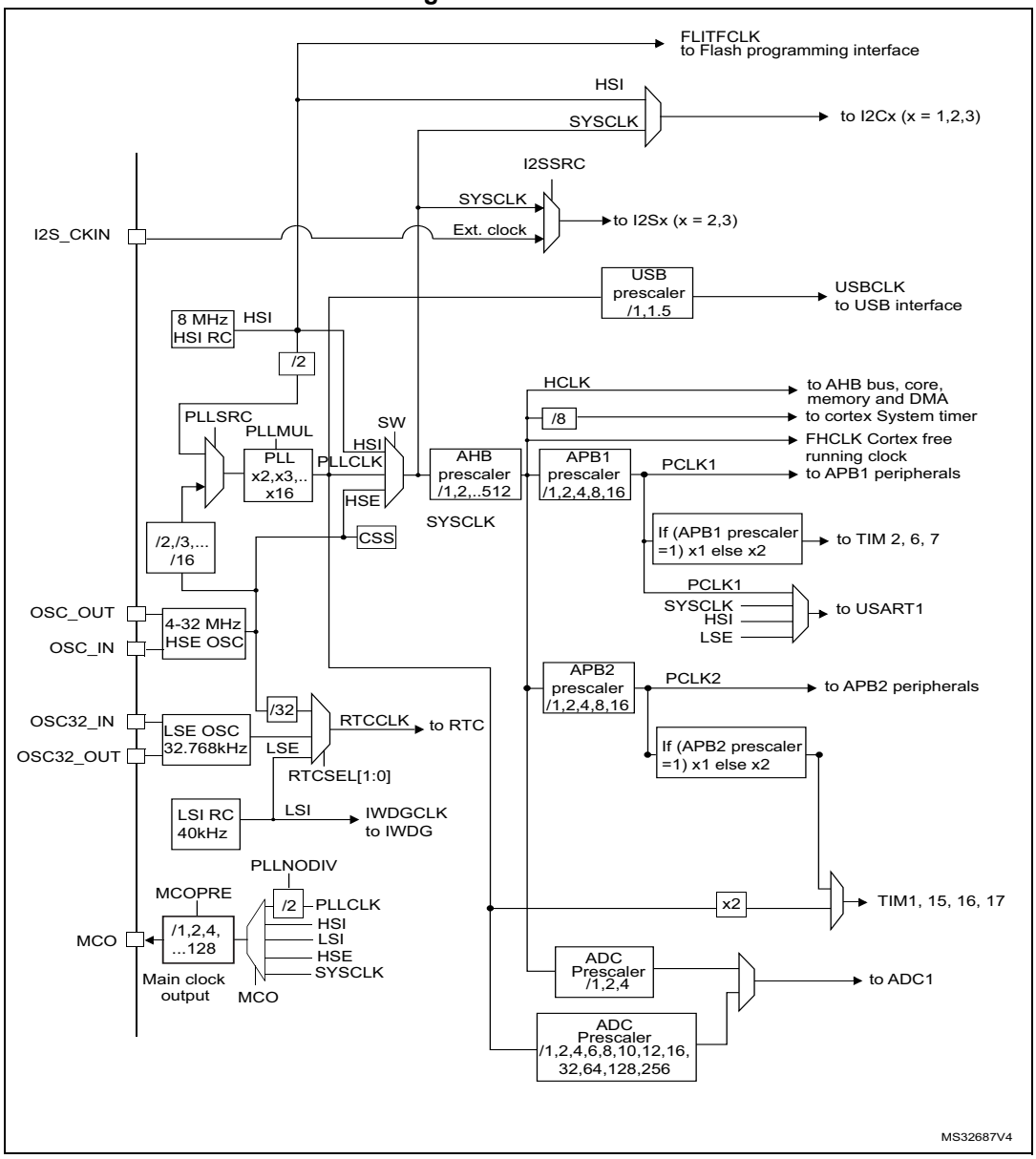
3.5.2 Power supply supervisor

The device has an integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

Figure 2. Clock tree



3.15.1 Advanced timer (TIM1)

The advanced-control timer can each be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIM timers (described in *Section 3.15.2* using the same architecture, so the advanced-control timers can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

3.15.2 General-purpose timers (TIM2, TIM15, TIM16, TIM17)

There are up to four synchronizable general-purpose timers embedded in the STM32F302x6/8 devices (see *Table 4* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

TIM2

TIM2 has a 32-bit auto-reload up/downcounter and 32-bit prescaler

It features 4 independent channels for input capture/output compare, PWM or one-pulse mode output. It can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

The counter can be frozen in debug mode.

It has independent DMA request generation and supports quadrature encoders.

TIM15, TIM16 and TIM 17

These three timers general-purpose timers with mid-range features:

They have 16-bit auto-reload upcounters and 16-bit prescalers.

- TIM15 has 2 channels and 1 complementary channel
- TIM16 and TIM17 have 1 channel and 1 complementary channel

All channels can be used for input capture/output compare, PWM or one-pulse mode output.

The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

The counters can be frozen in debug mode.

3.24 Development support

3.24.1 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

Table 12. STM32F302x6/8 pin definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN32	WLCSP49	LQFP48	LQFP64						
7	F6	10	14	PA0 -TAMPER2-WKUP1	I/O	TTa	(2)	TIM2_CH1/TIM2_ETR, TSC_G1_IO1, USART2_CTS, EVENTOUT	ADC1_IN1, RTC_TAMP2, WKUP1
8	G7	11	15	PA1	I/O	TTa	(2)	RTC_REFIN, TIM2_CH2, TSC_G1_IO2, USART2_RTS_DE, TIM15_CH1N, EVENTOUT	ADC1_IN2
9	E5	12	16	PA2	I/O	TTa	(2)	TIM2_CH3, TSC_G1_IO3, USART2_TX, COMP2_OUT, TIM15_CH1, EVENTOUT	ADC1_IN3, COMP2_INM
10	E4	13	17	PA3	I/O	TTa	(2)	TIM2_CH4, TSC_G1_IO4, USART2_RX, TIM15_CH2, EVENTOUT	ADC1_IN4
-	F7	-	18	VSS_4	S	-	-	-	-
-	F2	-	19	VDD_4	S	-	-	-	-
11	G6	14	20	PA4	I/O	TTa	(2)(3)	TSC_G2_IO1, SPI3_NSS/I2S3_WS, USART2_CK, EVENTOUT	ADC1_IN5, DAC1_OUT1, COMP2_INM, COMP4_INM, COMP6_INM
12	F5	15	21	PA5	I/O	TTa	-	TIM2_CH1/TIM2_ETR, TSC_G2_IO2, EVENTOUT	OPAMP2_VINM
13	F4	16	22	PA6	I/O	TTa	(3)	TIM16_CH1, TSC_G2_IO3, TIM1_BKIN, EVENTOUT	ADC1_IN10, OPAMP2_VOUT
14	F3	17	23	PA7	I/O	TTa	-	TIM17_CH1, TSC_G2_IO4, TIM1_CH1N, EVENTOUT	ADC1_IN15, COMP2_INP, OPAMP2_VINP

Table 12. STM32F302x6/8 pin definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN32	WLCSP49	LQFP48	LQFP64						
-	F1	27	35	PB14	I/O	TTa	-	TIM15_CH1, TSC_G6_IO4, SPI2_MISO/I2S2ext_SD, TIM1_CH2N, USART3_RTS_DE, EVENTOUT	OPAMP2_VINP
-	E1	28	36	PB15	I/O	TTa	-	RTC_REFIN, TIM15_CH2, TIM15_CH1N, TIM1_CH3N, SPI2_MOSI/I2S2_SD, EVENTOUT	COMP6_INM
-	-	-	37	PC6	I/O	FT	-	EVENTOUT, I2S2_MCK, COMP6_OUT	-
-	-	-	38	PC7	I/O	FT	-	EVENTOUT, I2S3_MCK	-
-	-	-	39	PC8	I/O	FT	-	EVENTOUT	-
-	-	-	40	PC9	I/O	FTf	-	EVENTOUT, I2C3_SDA, I2SCKIN	-
18	D1	29	41	PA8	I/O	FT	-	MCO, I2C3_SCL, I2C2_SMBAL, I2S2_MCK, TIM1_CH1, USART1_CK, EVENTOUT	-
19	D2	30	42	PA9	I/O	FTf	-	I2C3_SMBAL, TSC_G4_IO1, I2C2_SCL, I2S3_MCK, TIM1_CH2, USART1_TX, TIM15_BKIN, TIM2_CH3, EVENTOUT	-

Table 12. STM32F302x6/8 pin definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN32	WLCSP49	LQFP48	LQFP64						
-	-	-	51	PC10	I/O	FT	-	EVENTOUT, SPI3_SCK/I2S3_CK, USART3_TX	-
-	-	-	52	PC11	I/O	FT	-	EVENTOUT, SPI3_MISO/I2S3ext_SD, USART3_RX	-
-	-	-	53	PC12	I/O	FT	-	EVENTOUT, SPI3_MOSI/I2S3_SD, USART3_CK	-
-	-	-	54	PD2	I/O	FT	-	EVENTOUT	-
26	A3	39	55	PB3	I/O	FT	-	JTDO-TRACESWO, TIM2_CH2, TSC_G5_IO1, SPI3_SCK/I2S3_CK, USART2_TX, EVENTOUT	-
27	A4	40	56	PB4	I/O	FT	-	JTRST, TIM16_CH1, TSC_G5_IO2, SPI3_MISO/I2S3ext_SD, USART2_RX, TIM17_BKIN, EVENTOUT	-
28	B4	41	57	PB5	I/O	FT	-	TIM16_BKIN, I2C1_SMBAI, SPI3_MOSI/I2S3_SD, USART2_CK, I2C3_SDA, TIM17_CH1, EVENTOUT	-
29	C4	42	58	PB6	I/O	FTf	-	TIM16_CH1N, TSC_G5_IO3, I2C1_SCL, USART1_TX, EVENTOUT	-
30	D4	43	59	PB7	I/O	FTf	-	TIM17_CH1N, TSC_G5_IO4, I2C1_SDA, USART1_RX, EVENTOUT	-

Table 20. Current characteristics

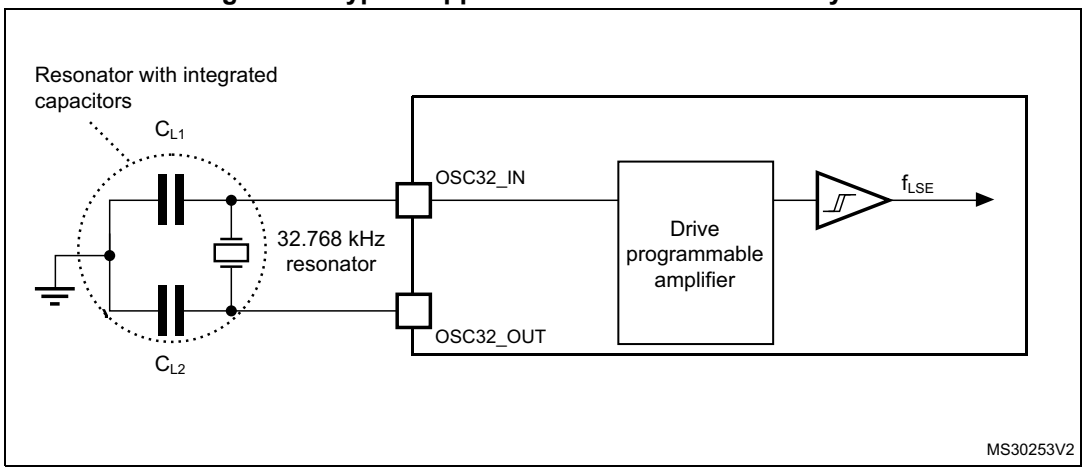
Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all VDD_x power lines (source)	130	mA
ΣI_{VSS}	Total current out of sum of all VSS_x ground lines (sink)	-130	
I_{VDD}	Maximum current into each V_{DD_x} power line (source)(1)	100	
I_{VSS}	Maximum current out of each V_{SS_x} ground line (sink)(1)	-100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins(2)	80	
	Total output current sourced by sum of all IOs and control pins(2)	-80	
$I_{INJ(PIN)}$	Injected current on TT, FT, FTf and B pins(3)	-5/+0	
	Injected current on TC and RST pin(4)	+/-5	
	Injected current on TTa pins(5)	+/-5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	+/-25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS} and V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins.The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 19: Voltage characteristics* for the maximum allowed input voltage values.
5. A positive injection is induced by $V_{IN} > V_{DDA}$ while a negative injection is induced by $V_{IN} < V_{SS}$. I_{INJ}(PIN) must never be exceeded. Refer also to *Table 19: Voltage characteristics* for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note (2) below *Table 68*.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 21. Thermal characteristics

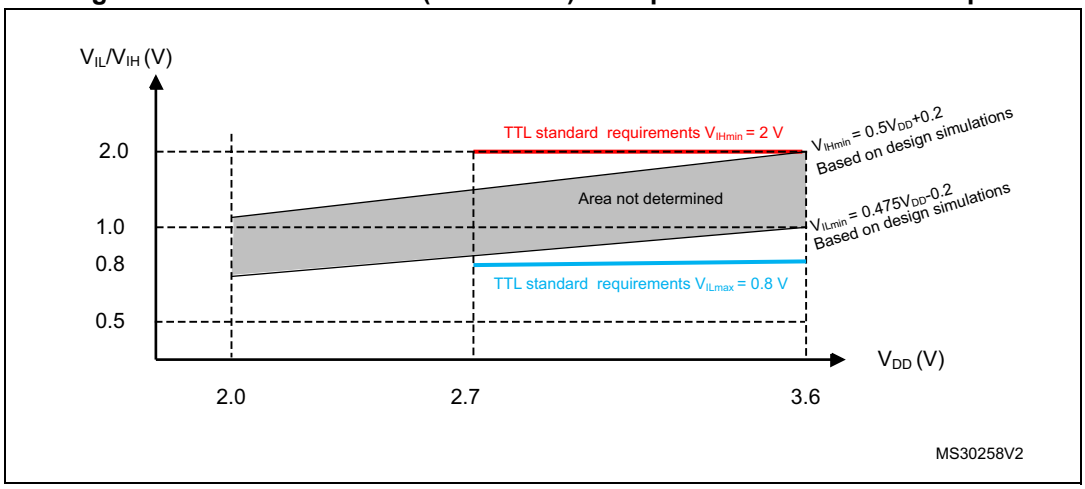
Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

Figure 17. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

Figure 22. Five volt tolerant (FT and FTf) I/O input characteristics - TTL port



USB characteristics

Table 63. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design.

Table 64. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels					
V_{DD}	USB operating voltage(2)		3.0(3)	3.6	V
V_{DI}(4)	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	V
V_{CM}(4)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(4)	Single ended receiver threshold		1.3	2.0	
Output levels					
V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(5)	-	0.3	V
V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(5)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. The STM32F3xxx USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
4. Guaranteed by design.
5. R_L is the load connected on the USB drivers.

Figure 30. USB timings: definition of data signal rise and fall time

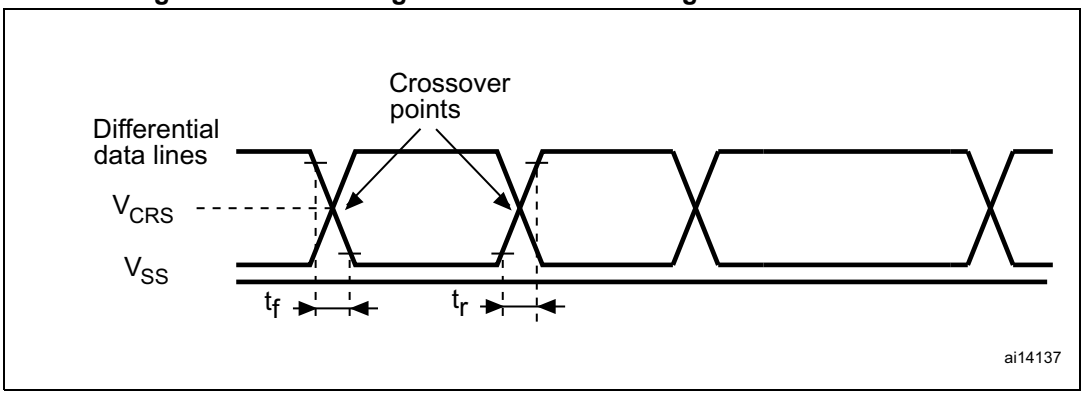
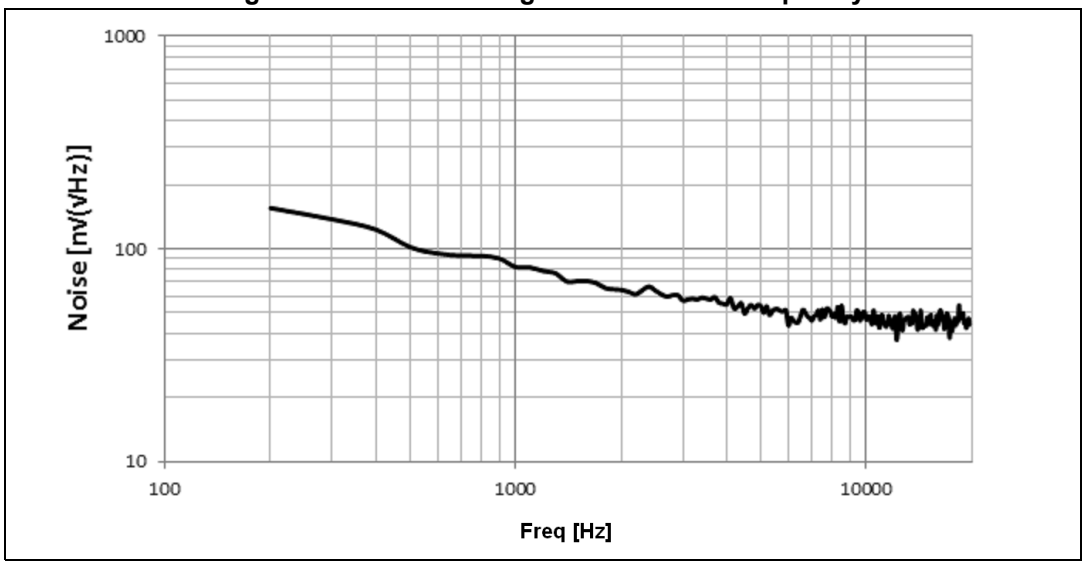


Table 65. USB: Full-speed electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver characteristics						
t_r	Rise time(2)	C_L = 50 pF	4	-	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	-	20	ns

Figure 36. OPAMP Voltage Noise versus Frequency



6.3.22 Temperature sensor characteristics

Table 74. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L (1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START} (1)	Startup time	4	-	10	µs
T_{S_temp} (1)(2)	ADC sampling time when reading the temperature	2.2	-	-	µs

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

Table 75. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C V_{DDA}= 3.3 V	0x1FFF F7C2 - 0x1FFF F7C3

6.3.23 V_{BAT} monitoring characteristics

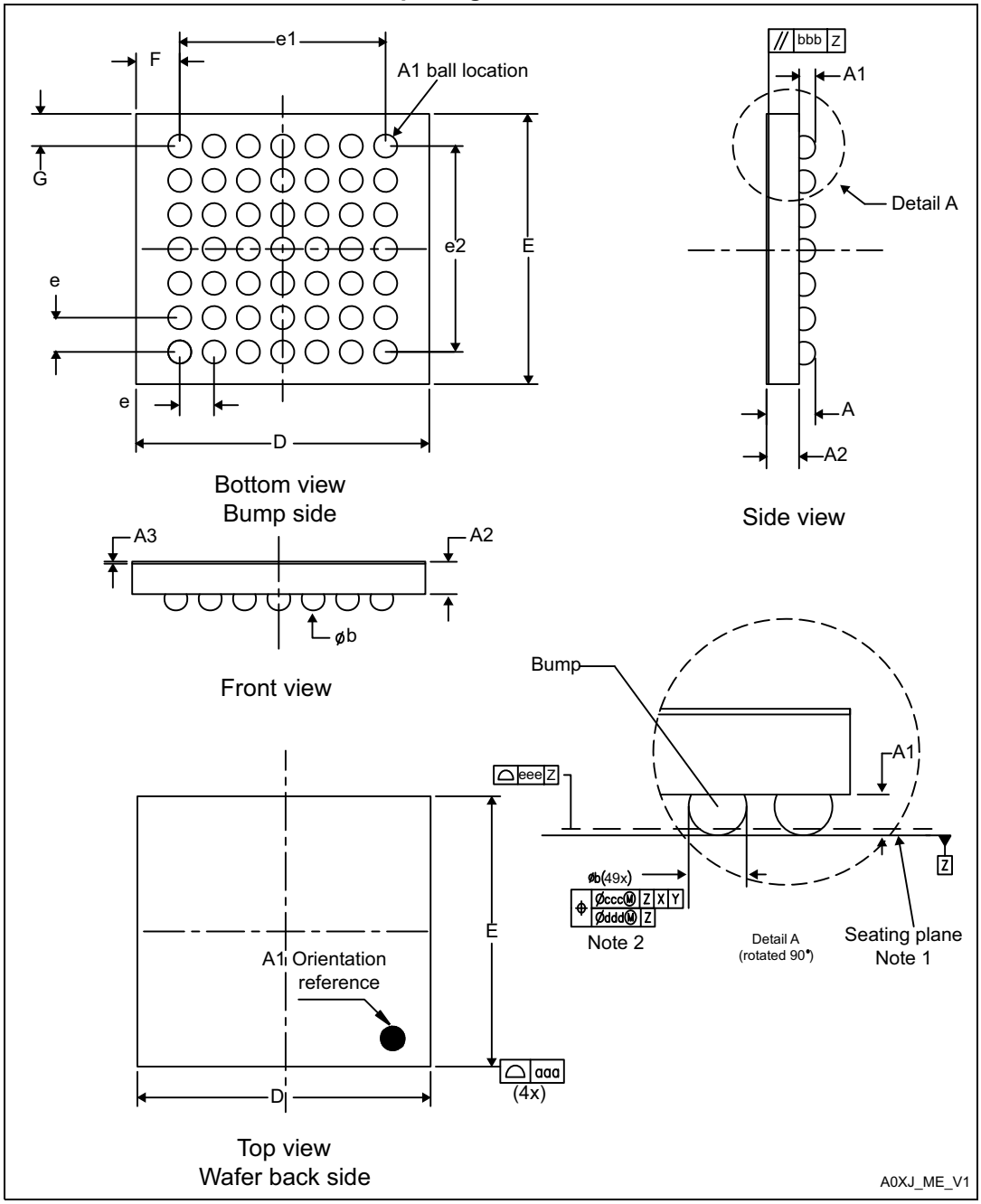
Table 76. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	2	-	
Er(1)	Error on Q	-1	-	+1	%
T_{S_vbat} (1)(2)	ADC sampling time when reading the V_{BAT} 1mV accuracy	2.2	-	-	µs

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

7.1 WLCSP49 package information

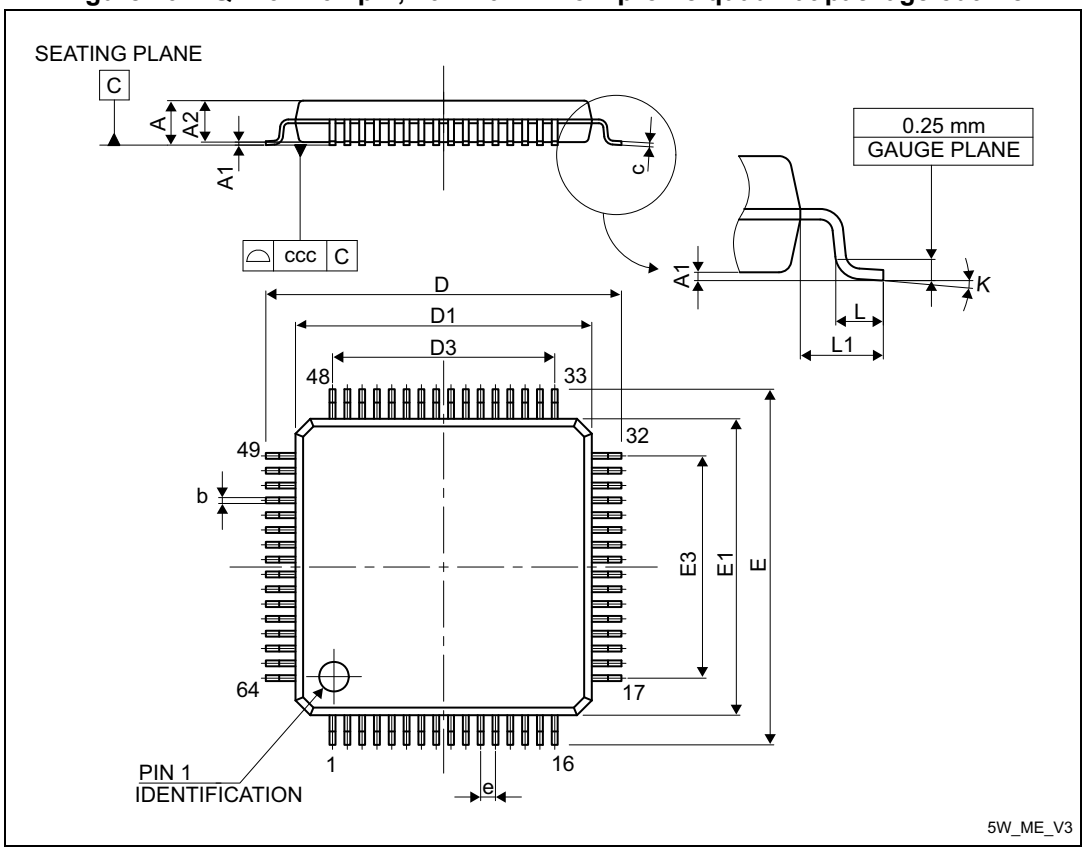
Figure 37. WLCSP49 - 49-pin, 3.417 x 3.151 mm, 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.

7.2 LQFP64 package information

Figure 40. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 79. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 115 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 9 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 9 × 8 mA × 0.4 V = 28.8 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 28.8 mW:

P_{Dmax} = 70 + 28.8 = 98.8 mW

Thus: P_{Dmax} = 98.8 mW

Using the values obtained in *Table 82* T_{Jmax} is calculated as follows:

– For LQFP100, 45°C/W

T_{Jmax} = 115°C + (45°C/W × 98.8 mW) = 115 °C + 4.44°C = 119.44°C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 8: Ordering information*).