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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 15x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f302r6t6tr

Contents

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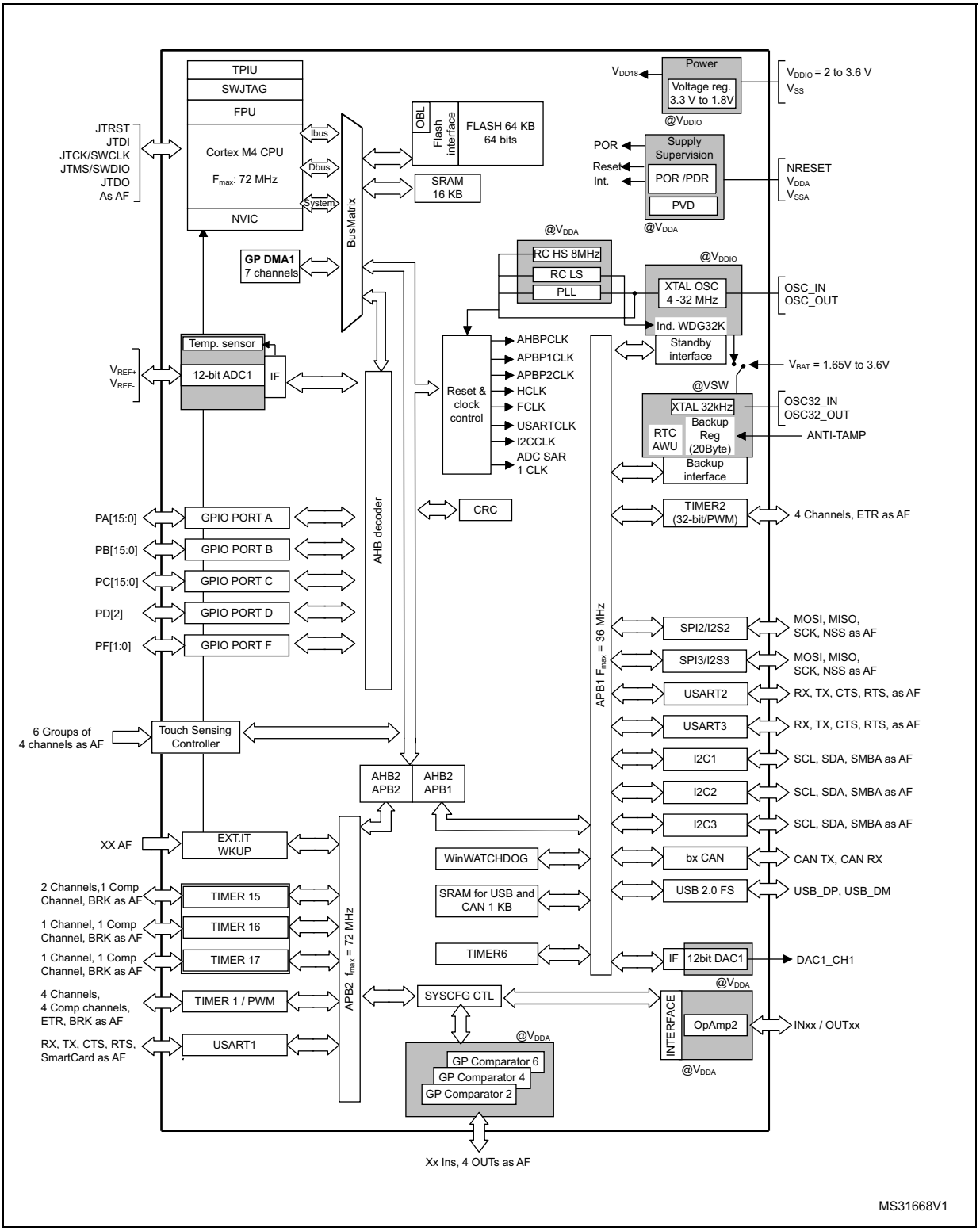
1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F302x6/8 microcontrollers.

This datasheet should be read in conjunction with the STM32F302xB/C/D/E and STM32F302x6/8 advanced ARM®-based 32-bit MCUs reference manual (RM0365). The reference manual is available from the STMicroelectronics website *www.st.com*.

For information on the ARM® Cortex®-M4 core, please refer to the Cortex®-M4 Technical Reference Manual, available from ARM website www.arm.com.

Figure 1. DS9896 block diagram



1. AF: alternate function on I/O pins.

3.18 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F302x6/8 devices have three embedded universal synchronous receiver transmitters (USART1, USART2 and USART3).

The USART interfaces are able to communicate at speeds of up to 9 Mbit/s.

All USARTs support hardware management of the CTS and RTS signals, multiprocessor communication mode, single-wire half-duplex communication mode and synchronous mode.

USART1 supports SmartCard mode, IrDA SIR ENDEC, LIN Master capability and autobaudrate detection.

All USART interfaces can be served by the DMA controller.

Refer to *Table 7* for the features available in all USARTs interfaces.

Table 7. USART features

USART modes/features(1)	USART1	USART2	USART3
Hardware flow control for modem	X	X	X
Continuous communication using DMA	X	X	X
Multiprocessor communication	X	X	X
Synchronous mode	X	X	X
SmartCard mode	X	-	-
Single-wire half-duplex communication	X	X	X
IrDA SIR ENDEC block	X	-	-
LIN mode	X	-	-
Dual clock domain and wakeup from Stop mode	X	-	-
Receiver timeout interrupt	X	-	-
Modbus communication	X	-	-
Auto baud rate detection	X	-	-
Driver Enable	X	X	X

1. X = supported.

3.19 Serial peripheral interfaces (SPI)/Inter-integrated sound interfaces (I2S)

Two SPI interfaces (SPI2 and SPI3) allow communication up to 18 Mbit/s in slave and master modes in full-duplex and simplex modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

Two standard I2S interfaces (multiplexed with SPI2 and SPI3) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I2S interfaces is/are configured in master

mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

Refer to *Table 8* for the features available in SPI2 and SPI3.

Table 8. STM32F302x6/8 SPI/I2S implementation

SPI features(1)	SPI2	SPI3
Hardware CRC calculation	X	X
Rx/Tx FIFO	X	X
NSS pulse mode	X	X
I2S mode	X	X
TI mode	X	X

1. X = supported.

3.20 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

3.21 Universal serial bus (USB)

The STM32F302x6 STM32F302x8 embeds a full-speed USB device peripheral compliant with the USB specification version 2.0. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up-to 1 KB (the last 256 bytes are used for CAN peripheral if enabled) and suspend/resume support. It requires a precise 48 MHz clock which is generated from the internal main PLL (the clock source must use an HSE crystal oscillator).

3.22 Touch sensing controller (TSC)

The STM32F302x6/8 devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 18 capacitive sensing channels distributed over 6 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (for example glass, plastic). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

Table 10. No. of capacitive sensing channels available on STM32F302x6/8 devices (continued)

Analog I/O group	Number of capacitive sensing channels		
	STM32F302Rx	STM32F302Cx	STM32F302Kx
G6	3	3	0
Number of capacitive sensing channels	18	17	13

3.23 Infrared transmitter

The STM32F302x6/8 devices provide an infrared transmitter solution. The solution is based on internal connections between TIM16 and TIM17 as shown in the figure below.

TIM17 is used to provide the carrier frequency and TIM16 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate the infrared remote control signals, TIM16 channel 1 and TIM17 channel 1 must be properly configured to generate correct waveforms. All standard IR pulse modulation modes can be obtained by programming the two timers output compare channels.

Figure 3. Infrared transmitter

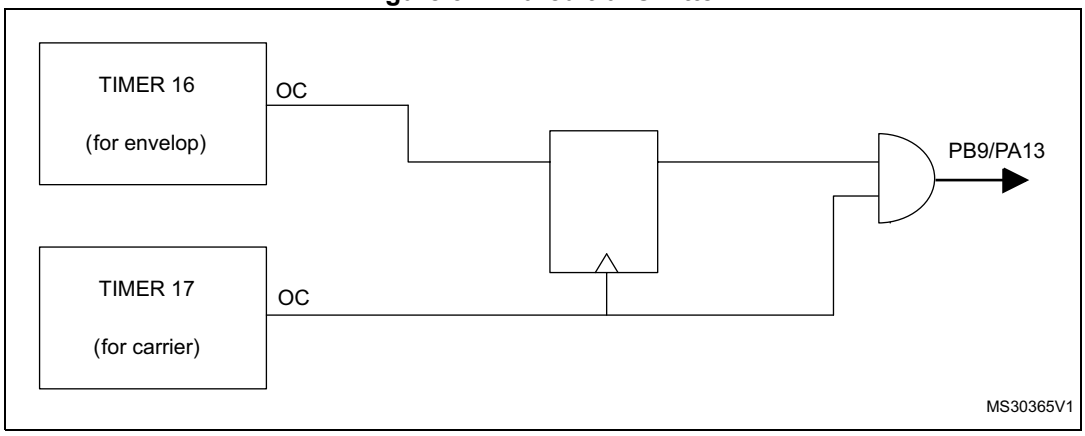


Table 12. STM32F302x6/8 pin definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN32	WLCSP49	LQFP48	LQFP64						
-	-	-	24	PC4	I/O	TT	-	EVENTOUT, TIM1_ETR, USART1_TX	
-	-	-	25	PC5	I/O	TTa	-	EVENTOUT, TIM15_BKIN, TSC_G3_IO1, USART1_RX	OPAMP2_VINM
15	G5	18	26	PB0	I/O	TTa	-	TSC_G3_IO2, TIM1_CH2N, EVENTOUT	ADC1_IN11, COMP4_INP, OPAMP2_VINP
-	G4	19	27	PB1	I/O	TTa	-	TSC_G3_IO3, TIM1_CH3N, COMP4_OUT, EVENTOUT	ADC1_IN12
-	G3	20	28	PB2	I/O	TTa	-	TSC_G3_IO4, EVENTOUT	COMP4_INM
-	E3	21	29	PB10	I/O	TT	-	TIM2_CH3, TSC_SYNC, USART3_TX, EVENTOUT	
-	G2	22	30	PB11	I/O	TTa	-	TIM2_CH4, TSC_G6_IO1, USART3_RX, EVENTOUT	ADC1_IN14, COMP6_INP
16	D3	23	31	VSS_2	S	-	-	Digital ground	
17	B2	24	32	VDD_2	S	-	-	Digital power supply	
-	E2	25	33	PB12	I/O	TT	-	TSC_G6_IO2, I2C2_SMBAL, SPI2_NSS/I2S2_WS, TIM1_BKIN, USART3_CK, EVENTOUT	
-	G1	26	34	PB13	I/O	TTa	-	TSC_G6_IO3, SPI2_SCK/I2S2_CK, TIM1_CH1N, USART3_CTS, EVENTOUT	ADC1_IN13

Table 13. Alternate functions for Port A

Port & pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	SYS_AF	TIM2/TIM15/TIM16 /TIM17/EVENT	I2C3/TIM1/TIM2/TIM15	I2C3/TIM15/TSC	I2C1/I2C2/TIM1/ TIM16/TIM17	SPI2/I2S2/ SPI3/I2S3/Infrared	SPI2/I2S2/SPI3/ I2S3/TIM1/Infrared	USART1/USART2/USART3/ CAN/GPCOMP6	I2C3/GPCOMP2 /GPCOMP4/GPCOMP6	CAN/TIM1/TIM15	TIM2/TIM17	TIM1	TIM1	-	-	EVENT
PA0	-	TIM2 _CH1/ TIM2 _ETR	-	TSC _G1_IO1	-	-	-	USART2 _CTS	-	-	-	-	-	-	-	EVENT OUT
PA1	RTC _REFIN	TIM2 _CH2	-	TSC _G1_IO2	-	-	-	USART2 _RTS_D E	-	TIM15 _CH1N	-	-	-	-	-	EVENT OUT
PA2	-	TIM2 _CH3	-	TSC _G1_IO3	-	-	-	USART2 _TX	COMP2 _OUT	TIM15 _CH1	-	-	-	-	-	EVENT OUT
PA3	-	TIM2 _CH4	-	TSC _G1_IO4	-	-	-	USART2 _RX	-	TIM15 _CH2	-	-	-	-	-	EVENT OUT
PA4	-	-	-	TSC _G2_IO1	-	-	SPI3_NSS/ I2S3_WS	USART2 _CK	-	-	-	-	-	-	-	EVENT OUT
PA5	-	TIM2 _CH1/ TIM2 _ETR	-	TSC _G2_IO2	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PA6	-	TIM16 _CH1	-	TSC _G2_IO3	-	-	TIM1_BKIN	-	-	-	-	-	-	-	-	EVENT OUT
PA7	-	TIM17 _CH1	-	TSC _G2_IO4	-	-	TIM1 _CH1N	-	-	-	-	-	-	-	-	EVENT OUT
PA8	MCO	-	-	I2C3 _SCL	I2C2 _SMBAL	I2S2 _MCK	TIM1_CH1	USART1 _CK	-	-	-	-	-	-	-	EVENT OUT

Table 14. Alternate functions for Port B

Port & pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	SYS_AF	TIM2/TIM15/TIM16 /TIM17/EVENT	I2C3/TIM1/TIM2/TIM15	I2C3/TIM15/TSC	I2C1/I2C2/TIM1/ TIM16/TIM17	SPI2/I2S2/ SPI3/I2S3/Infrared	SPI2/I2S2/SPI3/ I2S3/TIM1/Infrared	USART1/USART2/USART3/ CAN/GPCOMP6	I2C3/GPCOMP2 /GPCOMP4/GPCOMP6	CAN/TIM1/TIM15	TIM2/TIM17	TIM1	TIM1	-	-	EVENT
PB0	-	-	-	TSC _G3_IO2	-	-	TIM1 _CH2N	-	-	-	-	-	-	-	-	EVENT OUT
PB1	-	-	-	TSC _G3_IO3	-	-	TIM1 _CH3N	-	COMP4_ OUT	-	-	-	-	-	-	EVENT OUT
PB2				TSC _G3_IO4	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PB3	JTDO-TRACE SWO	TIM2 _CH2	-	TSC _G5_IO1	-	-	SPI3_SC K/I2S3_ CK	USART2 _TX	-	-	-	-	-	-	-	EVENT OUT
PB4	JTRST	TIM16 _CH1	-	TSC _G5_IO2	-	-	SPI3_MI SO/I2S3 _SD	USART2 _RX	-	-	TIM17 _BKIN	-	-	-	-	EVENT OUT
PB5	-	TIM16 _BKIN	-	-	I2C1 _SMBAI	-	SPI3 _MOSI/ I2S3ext_ SD	USART2 _CK	I2C3 _SDA	-	TIM17 _CH1	-	-	-	-	EVENT OUT
PB6	-	TIM16 _CH1N	-	TSC _G5_IO3	I2C1 _SCL	-	-	USART1 _TX	-	-	-	-	-	-	-	EVENT OUT
PB7	-	TIM17 _CH1N	-	TSC _G5_IO4	I2C1 _SDA	-	-	USART1 _RX	-	-	-	-	-	-	-	EVENT OUT
PB8	-	TIM16 _CH1	-	TSC _SYNC	I2C1 _SCL	-	-	USART3 _RX	-	CAN _RX	-	-	TIM1 _BKIN	-	-	EVENT OUT

Table 18. STM32F302x6 STM32F302x8 peripheral register boundary addresses (continued)(1)

Bus	Boundary address	Size (bytes)	Peripheral
APB1	0x4000 7800 - 0x4000 7BFF	9 K	I2C3
	0x4000 7400 - 0x4000 77FF	1 K	DAC1
	0x4000 7000 - 0x4000 73FF	1 K	PWR
	0x4000 6C00 - 0x4000 6FFF	1 K	Reserved
	0x4000 6800 - 0x4000 6BFF	1 K	Reserved
	0x4000 6400 - 0x4000 67FF	1 K	bxCAN
	0x4000 6000 - 0x4000 63FF	1 K	USB/CAN SRAM
	0x4000 5C00 - 0x4000 5FFF	1 K	USB device FS
	0x4000 5800 - 0x4000 5BFF	1 K	I2C2
	0x4000 5400 - 0x4000 57FF	1 K	I2C1
	0x4000 5000 - 0x4000 53FF	1 K	Reserved
	0x4000 4C00 - 0x4000 4FFF	1 K	Reserved
	0x4000 4800 - 0x4000 4BFF	1 K	USART3
	0x4000 4400 - 0x4000 47FF	1 K	USART2
	0x4000 4000 - 0x4000 43FF	1 K	I2S3ext
	0x4000 3C00 - 0x4000 3FFF	1 K	SPI3/I2S3
	0x4000 3800 - 0x4000 3BFF	1 K	SPI2/I2S2
	0x4000 3400 - 0x4000 37FF	1 K	I2S2ext
	0x4000 3000 - 0x4000 33FF	1 K	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 K	WWDG
	0x4000 2800 - 0x4000 2BFF	1 K	RTC
	0x4000 1400 - 0x4000 27FF	5 K	Reserved
	0x4000 1000 - 0x4000 13FF	1 K	TIM6
	0x4000 0C00 - 0x4000 0FFF	1 K	Reserved
	0x4000 0800 - 0x4000 0BFF	1 K	Reserved
	0x4000 0400 - 0x4000 07FF	1 K	Reserved
	0x4000 0000 - 0x4000 03FF	1 K	TIM2
	0x2000 A000 - 3FFF FFFF	~512 M	Reserved
	0x2000 0000 - 0x2000 9FFF	40 K	SRAM
	0x1FFF F800 - 0x1FFF FFFF	2 K	Option bytes
	0x1FFF D800 - 0x1FFF F7FF	8 K	System memory
	0x0804 0000 - 0x1FFF D7FF	~384 M	Reserved
	0x0800 0000 - 0x0800 FFFF	64 K	Main Flash memory

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA}= 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 9. Pin loading conditions

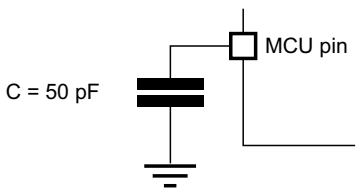
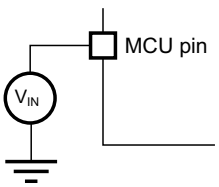


Figure 10. Pin input voltage



6.1.7 Current consumption measurement

Figure 12. Current consumption measurement scheme

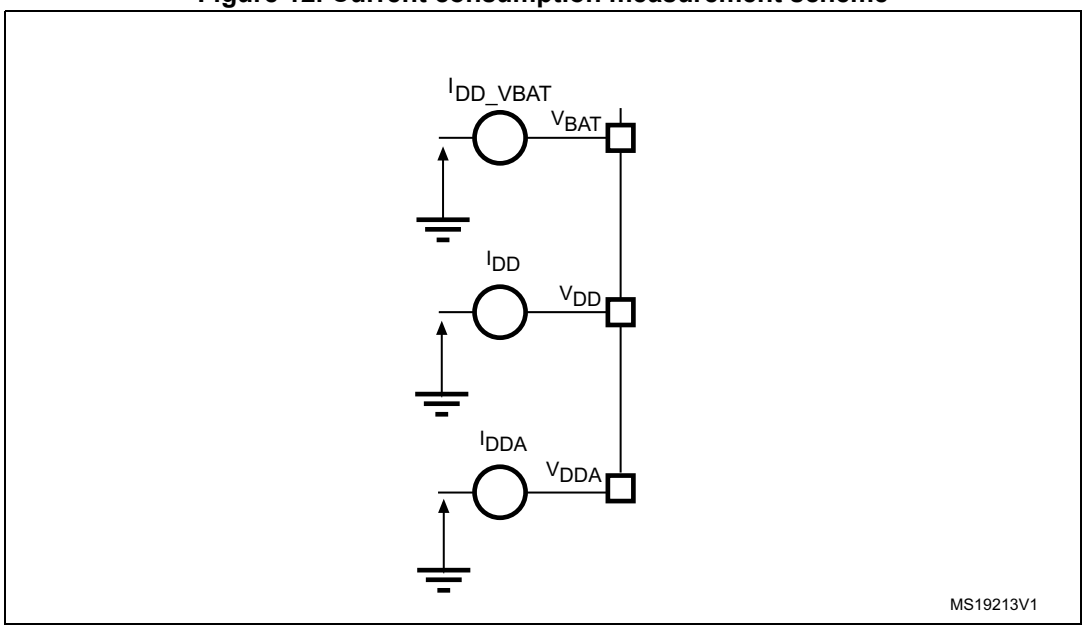


Table 20. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all VDD_x power lines (source)	130	mA
ΣI_{VSS}	Total current out of sum of all VSS_x ground lines (sink)	-130	
I_{VDD}	Maximum current into each V_{DD_x} power line (source)(1)	100	
I_{VSS}	Maximum current out of each V_{SS_x} ground line (sink)(1)	-100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins(2)	80	
	Total output current sourced by sum of all IOs and control pins(2)	-80	
$I_{INJ(PIN)}$	Injected current on TT, FT, FTf and B pins(3)	-5/+0	
	Injected current on TC and RST pin(4)	+/-5	
	Injected current on TTa pins(5)	+/-5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	+/-25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS} and V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins.The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 19: Voltage characteristics* for the maximum allowed input voltage values.
5. A positive injection is induced by $V_{IN} > V_{DDA}$ while a negative injection is induced by $V_{IN} < V_{SS}$. I_{INJ}(PIN) must never be exceeded. Refer also to *Table 19: Voltage characteristics* for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note (2) below *Table 68*.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 21. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 24 MHz,1 wait state from 24 to 48 MHz and 2 wait states from 48 to 72 MHz)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK2} = f_{HCLK}$ and $f_{PCLK1} = f_{HCLK/2}$
- When $f_{HCLK} > 8$ MHz, the PLL is ON and the PLL input is equal to HSI/2 (4 MHz) or HSE (8 MHz) in bypass mode.

The parameters given in *Table 28* to *Table 34* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22*.

Table 28. Typical and maximum current consumption from VDD supply at VDD = 3.6V

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(1)			Typ	Max @ T_A(1)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Run mode, executing from Flash	External clock (HSE bypass)	72 MHz	45.7	48.6	50.0	52.0	25.5	27.5	28.1	28.8	mA
			64 MHz	40.6	43.6	44.5	46.4	22.7	24.6	25.2	25.9	
			48 MHz	30.8	33.6	34.1	35.5	17.3	19.0	19.5	20.0	
			32 MHz	21.0	22.9	23.5	25.6	11.7	13.2	13.7	14.1	
			24 MHz	16.0	16.8	18.0	18.9	9.0	10.4	10.8	11.4	
			8 MHz	5.4	5.6	6.1	7.2	3.3	3.3	3.8	4.2	
			1 MHz	1.1	1.2	1.7	2.7	0.8	0.9	1.3	1.6	
		Internal clock (HSI)	64 MHz	37.6	41.3	42.9	44.7	22.5	24.7	25.0	25.8	
			48 MHz	28.7	32.3	33.1	34.0	17.2	19.1	19.4	19.6	
			32 MHz	19.5	22.0	23.4	24.6	11.5	12.9	13.5	13.7	
			24 MHz	14.9	16.6	17.9	18.4	6.0	7.0	7.4	7.9	
			8 MHz	5.2	5.5	6.4	7.0	3.2	3.8	4.3	4.7	

Table 28. Typical and maximum current consumption from VDD supply at VDD = 3.6V (continued)

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(1)			Typ	Max @ T_A(1)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Run mode, executing from RAM	External clock (HSE bypass)	72 MHz	45.8	49.1(2)	50.1	51.4(2)	25.1	27.3(2)	28.0	28.6(2)	mA
			64 MHz	40.8	43.6	44.9	46.9	22.3	24.1	25.0	25.5	
			48 MHz	30.2	32.9	33.5	34.8	17.0	18.7	19.1	19.6	
			32 MHz	20.5	23.1	24.1	25.4	11.1	12.2	13.2	13.3	
			24 MHz	15.4	17.1	18.3	19.5	8.5	9.7	10.1	10.2	
			8 MHz	5.0	5.9	6.3	6.9	3.1	3.7	4.1	4.7	
			1 MHz	0.8	1.1	1.9	2.6	0.5	0.8	1.2	1.4	
		Internal clock (HSI)	64 MHz	37.3	41.1	41.8	43.3	22.0	23.8	24.4	24.9	
			48 MHz	28.0	31.1	31.6	33.2	16.4	18.0	18.3	18.6	
			32 MHz	18.8	21.3	22.1	23.1	10.9	11.9	12.8	13.1	
			24 MHz	14.2	15.9	16.8	17.9	5.5	6.4	6.7	7.3	
			8 MHz	4.8	5.1	6.0	6.5	2.9	3.5	4.1	4.2	
I_{DD}	Supply current in Sleep mode, executing from Flash or RAM	External clock (HSE bypass)	72 MHz	30.0	32.8(2)	33.1	34.1(2)	5.9	6.8(2)	6.9	7.4(2)	
			64 MHz	26.7	29.2	29.6	30.5	5.3	5.9	6.2	6.7	
			48 MHz	16.7	18.5	19.0	19.7	3.6	4.5	4.5	5.3	
			32 MHz	13.3	14.9	15.3	15.4	2.9	3.7	3.8	4.3	
			24 MHz	10.2	11.4	12.0	12.3	2.2	2.7	2.9	3.2	
			8 MHz	3.6	4.4	4.8	5.3	0.9	1.2	1.5	2.1	
			1 MHz	0.5	0.8	1.1	1.3	0.1	0.4	0.8	0.8	
		Internal clock (HSI)	64 MHz	23.2	25.3	25.6	26.2	5.0	5.7	6.1	6.2	mA
			48 MHz	17.5	19.2	19.4	19.9	3.9	4.7	4.8	5.3	
			32 MHz	11.7	12.9	13.2	13.3	2.6	3.4	3.6	4.2	
			24 MHz	8.9	10.2	10.6	10.8	1.4	2.1	2.4	2.7	
			8 MHz	3.4	4.0	4.6	5.1	0.7	1.1	1.4	1.9	

1. Guaranteed by characterization results.
2. Data based on characterization results and tested in production with code executing from RAM.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 53: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 36: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

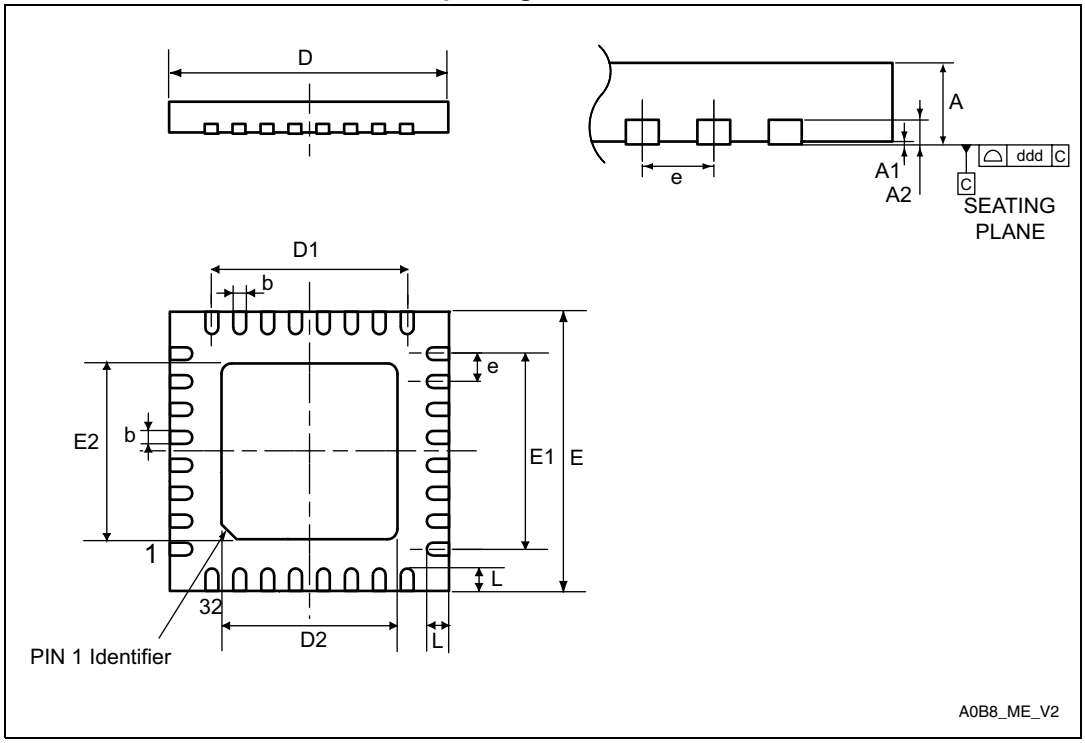
Table 73. Operational amplifier characteristics(1) (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
PGA gain	Non inverting gain value	-	-	2	-	-
			-	4	-	
			-	8	-	
			-	16	-	
$R_{network}$	R2/R1 internal resistance values in PGA mode (3)	Gain=2	-	5.4/5.4	-	kΩ
		Gain=4	-	16.2/5.4	-	
		Gain=8	-	37.8/5.4	-	
		Gain=16	-	40.5/2.7	-	
PGA gain error	PGA gain error	-	-1%	-	1%	%
I_{bias}	OPAMP input bias current	-	-	-	±0.2(4)	µA
PGA BW	PGA bandwidth for different non inverting gain	PGA Gain = 2, Cload = 50pF, Rload = 4 KΩ	-	4	-	MHz
		PGA Gain = 4, Cload = 50pF, Rload = 4 KΩ	-	2	-	
		PGA Gain = 8, Cload = 50pF, Rload = 4 KΩ	-	1	-	
		PGA Gain = 16, Cload = 50pF, Rload = 4 KΩ	-	0.5	-	
V_n	Voltage noise density	@ 1KHz, Output loaded with 4 KΩ	-	109	-	$\frac{nV}{\sqrt{Hz}}$
		@ 10KHz, Output loaded with 4 KΩ	-	43	-	

1. Guaranteed by design.
2. The saturation voltage can also be limited by the I_{LOAD} (drive current).
3. R2 is the internal resistance between OPAMP output and OPAMP inverting input.
   R1 is the internal resistance between OPAMP inverting input and ground.
   The PGA gain =1+R2/R1
4. Mostly TTa I/O leakage, when used in analog mode.

7.4 UFQFPN32 package information

Figure 46. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. This pad is used for the device ground and must be connected. It is referred to as pin 0 in Table: Pin definitions.

8 Ordering information

Table 83. Ordering information scheme

Example: STM32 F 302 K 8 T 6 xxx

Device family

STM32 = ARM®-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

302 = STM32F302xx, 2.0 to 3.6 V operating voltage

Pin count

K = 32 pins

C = 48 or 49 pins

R = 64 pins

Flash memory size

6 = 32 Kbytes of Flash memory

8 = 64 Kbytes of Flash memory

Package

T = LQFP

Y= WLCSP

U= UFQFPN

Temperature range

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

Options

xxx = programmed parts

TR = tape and reel