STMicroelectronics - STM32F302RET7TR Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	51
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f302ret7tr

3.8 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allows I/O toggling up to 36 MHz.

3.9 Direct memory access (DMA)

The flexible general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each of the 7 DMA channels is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, timers, DAC and ADC.

3.10 Interrupts and events

3.10.1 Nested vectored interrupt controller (NVIC)

The STM32F302x6/8 devices embed a nested vectored interrupt controller (NVIC) able to handle up to 60 maskable interrupt channels and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.11 Fast analog-to-digital converter (ADC)

An analog-to-digital converter, with selectable resolution between 12 and 6 bit, is embedded in the STM32F302x6/8 family devices. The ADC has up to 15 external channels performing conversions in single-shot or scan modes. Channels can be configured to be either single-ended input or differential input. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Single-shunt phase current reading techniques.

The ADC can be served by the DMA controller.

Three analog watchdogs are available. The analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) and the advanced-control timer (TIM1) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

3.11.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

3.11.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC1_IN18 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

3.11.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC1_IN17. As the V_{BAT} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

3.12 Digital-to-analog converter (DAC)

One 12-bit buffered DAC channel (DAC1_OUT1) can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- One DAC output channel
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- DMA capability
- External triggers for conversion

3.13 Operational amplifier (OPAMP)

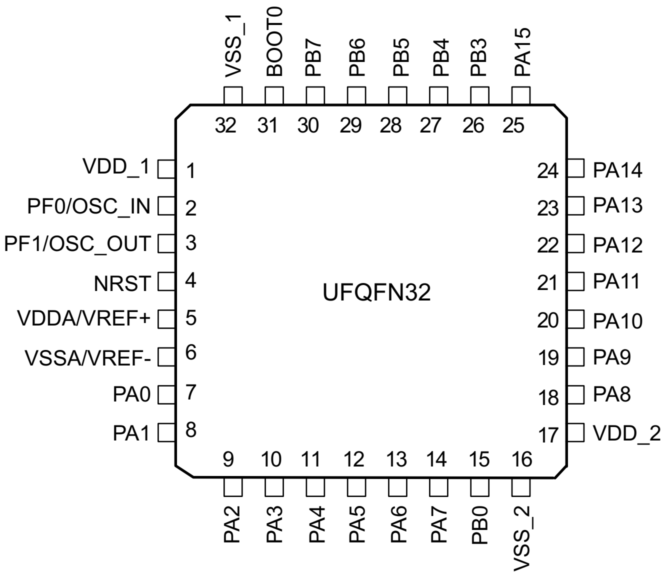
The STM32F302x6/8 devices embed one operational amplifier with external or internal follower routing and PGA capability (or even amplifier and filter capability with external components). When the operational amplifier is selected, an external ADC channel is used to enable output measurement.

The operational amplifier features:

- 8.2 MHz bandwidth
- 0.5 mA output capability
- Rail-to-rail input/output
- In PGA mode, the gain can be programmed to be 2, 4, 8 or 16.

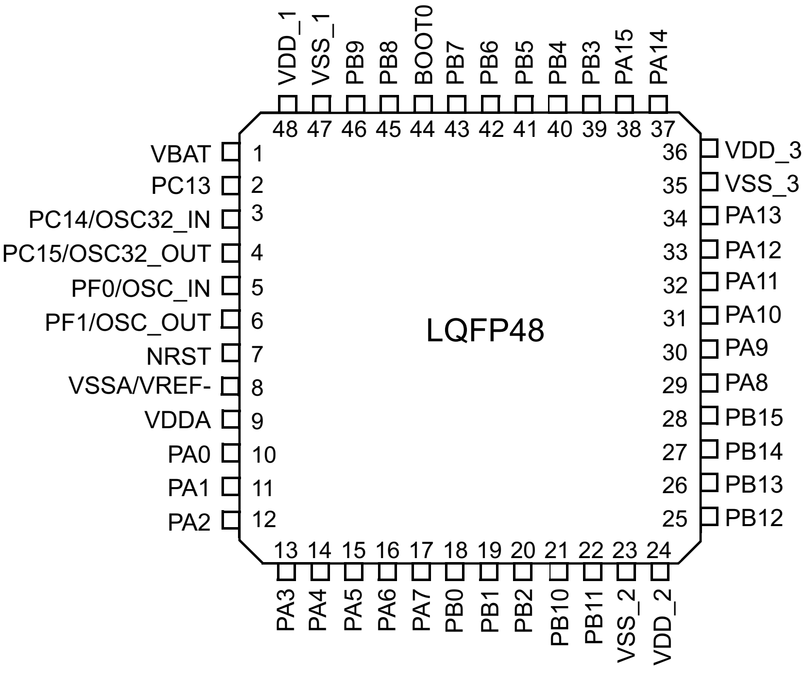
4 Pinouts and pin description

Figure 4. STM32F302x6/8 UFQFN32 pinout



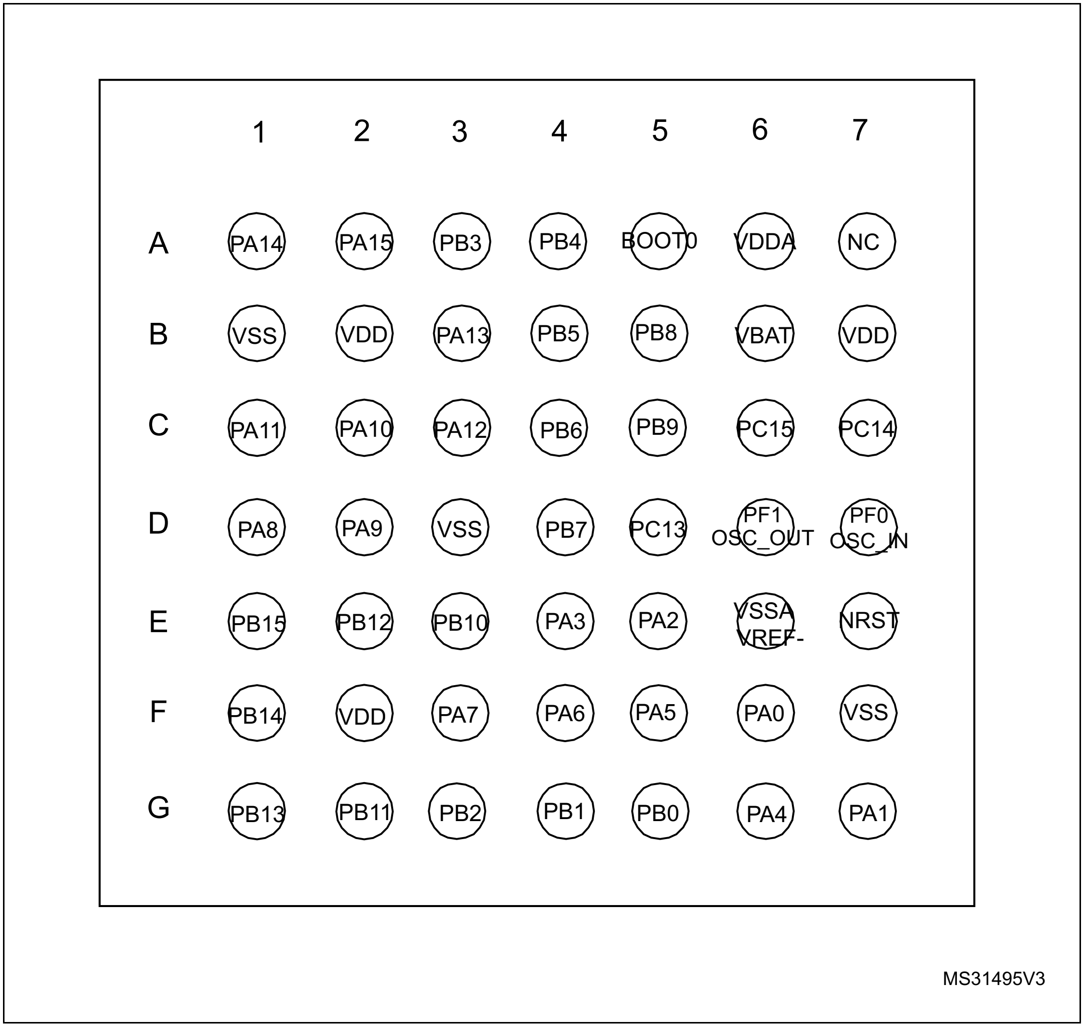
1. The above figure shows the package top view.

Figure 5. STM32F302x6/8 LQFP48 pinout



1. The above figure shows the package top view.

Figure 7. STM32F302x6/8 WLCSP49 ballout



	1	2	3	4	5	6	7
A	PA14	PA15	PB3	PB4	BOOT0	VDDA	NC
B	VSS	VDD	PA13	PB5	PB8	VBAT	VDD
C	PA11	PA10	PA12	PB6	PB9	PC15	PC14
D	PA8	PA9	VSS	PB7	PC13	PF1 OSC_OUT	PF0 OSC_IN
E	PB15	PB12	PB10	PA3	PA2	VSSA VREF-	NRST
F	PB14	VDD	PA7	PA6	PA5	PA0	VSS
G	PB13	PB11	PB2	PB1	PB0	PA4	PA1

1. The above figure shows the package top view.
2. NC: Not connected.

Table 12. STM32F302x6/8 pin definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN32	WLCSP49	LQFP48	LQFP64						
-	-	-	24	PC4	I/O	TT	-	EVENTOUT, TIM1_ETR, USART1_TX	
-	-	-	25	PC5	I/O	TTa	-	EVENTOUT, TIM15_BKIN, TSC_G3_IO1, USART1_RX	OPAMP2_VINM
15	G5	18	26	PB0	I/O	TTa	-	TSC_G3_IO2, TIM1_CH2N, EVENTOUT	ADC1_IN11, COMP4_INP, OPAMP2_VINP
-	G4	19	27	PB1	I/O	TTa	-	TSC_G3_IO3, TIM1_CH3N, COMP4_OUT, EVENTOUT	ADC1_IN12
-	G3	20	28	PB2	I/O	TTa	-	TSC_G3_IO4, EVENTOUT	COMP4_INM
-	E3	21	29	PB10	I/O	TT	-	TIM2_CH3, TSC_SYNC, USART3_TX, EVENTOUT	
-	G2	22	30	PB11	I/O	TTa	-	TIM2_CH4, TSC_G6_IO1, USART3_RX, EVENTOUT	ADC1_IN14, COMP6_INP
16	D3	23	31	VSS_2	S	-	-	Digital ground	
17	B2	24	32	VDD_2	S	-	-	Digital power supply	
-	E2	25	33	PB12	I/O	TT	-	TSC_G6_IO2, I2C2_SMBAL, SPI2_NSS/I2S2_WS, TIM1_BKIN, USART3_CK, EVENTOUT	
-	G1	26	34	PB13	I/O	TTa	-	TSC_G6_IO3, SPI2_SCK/I2S2_CK, TIM1_CH1N, USART3_CTS, EVENTOUT	ADC1_IN13

Table 14. Alternate functions for Port B

Port & pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	SYS_AF	TIM2/TIM15/TIM16 /TIM17/EVENT	I2C3/TIM1/TIM2/TIM15	I2C3/TIM15/TSC	I2C1/I2C2/TIM1/ TIM16/TIM17	SPI2/I2S2/ SPI3/I2S3/Infrared	SPI2/I2S2/SPI3/ I2S3/TIM1/Infrared	USART1/USART2/USART3/ CAN/GPCOMP6	I2C3/GPCOMP2 /GPCOMP4/GPCOMP6	CAN/TIM1/TIM15	TIM2/TIM17	TIM1	TIM1	-	-	EVENT
PB0	-	-	-	TSC _G3_IO2	-	-	TIM1 _CH2N	-	-	-	-	-	-	-	-	EVENT OUT
PB1	-	-	-	TSC _G3_IO3	-	-	TIM1 _CH3N	-	COMP4_ OUT	-	-	-	-	-	-	EVENT OUT
PB2				TSC _G3_IO4	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PB3	JTDO-TRACE SWO	TIM2 _CH2	-	TSC _G5_IO1	-	-	SPI3_SCK/I2S3_ CK	USART2 _TX	-	-	-	-	-	-	-	EVENT OUT
PB4	JTRST	TIM16 _CH1	-	TSC _G5_IO2	-	-	SPI3_MISO/I2S3 _SD	USART2 _RX	-	-	TIM17 _BKIN	-	-	-	-	EVENT OUT
PB5	-	TIM16 _BKIN	-	-	I2C1 _SMBAI	-	SPI3 _MOSI/ I2S3ext_ SD	USART2 _CK	I2C3 _SDA	-	TIM17 _CH1	-	-	-	-	EVENT OUT
PB6	-	TIM16 _CH1N	-	TSC _G5_IO3	I2C1 _SCL	-	-	USART1 _TX	-	-	-	-	-	-	-	EVENT OUT
PB7	-	TIM17 _CH1N	-	TSC _G5_IO4	I2C1 _SDA	-	-	USART1 _RX	-	-	-	-	-	-	-	EVENT OUT
PB8	-	TIM16 _CH1	-	TSC _SYNC	I2C1 _SCL	-	-	USART3 _RX	-	CAN _RX	-	-	TIM1 _BKIN	-	-	EVENT OUT

Table 16. Alternate functions for Port D

Port & pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SYS_AF	TIM2/TIM15/ TIM16/TIM17/ EVENT	I2C3/TIM1/TIM2/ TIM15	I2C3/TIM15/TSC	I2C1/I2C2/TIM1/ TIM16/TIM17	SPI2/I2S2/ SPI3/I2S3/ Infrared	SPI2/I2S2/SPI3/ I2S3/TIM1/ Infrared	USART1/ USART2/ USART3/CAN/ GPCOMP6
PD2	-	EVENTOUT	-	-	-	-	-	-

Table 17. Alternate functions for Port F

Port & pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SYS_AF	TIM2/TIM15/ TIM16/TIM17/ EVENT	I2C3/TIM1/TIM2/ TIM15	I2C3/TIM15/TSC	I2C1/I2C2/TIM1/ TIM16/TIM17	SPI2/I2S2/ SPI3/I2S3/ Infrared	SPI2/I2S2/SPI3/ I2S3/TIM1/ Infrared	USART1/USAR T2/USART3/ CAN/GPCOMP6
PF0	-	-	-	-	I2C2_SDA	SPI2_NSS/ I2S2_WS	TIM1_CH3N	-
PF1	-	-	-	-	I2C2_SCL	SPI2_SCK/ I2S2_CK	-	-

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 19: Voltage characteristics*, *Table 20: Current characteristics*, and *Table 21: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 19. Voltage characteristics[1]

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including $V_{DDA,}$ V_{BAT} and V_{DD})	-0.3	4.0	V
V_{DD}–V_{DDA}	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	V
V_{IN}[2]	Input voltage on FT and FTf pins	V_{SS} –0.3	V_{DD} + 4.0	V
	Input voltage on TTa and TT pins	V_{SS} –0.3	4.0	
	Input voltage on any other pin	V_{SS} –0.3	4.0	
	Input voltage on Boot0 pin	0	9	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between all the different ground pins[3]	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.12: Electrical sensitivity characteristics*		V

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range. The following relationship must be respected between V_{DDA} and V_{DD}:
   V_{DDA} must power on before or at the same time as V_{DD} in the power up sequence.
   V_{DDA} must be greater than or equal to V_{DD}.
2. V_{IN} maximum must always be respected. Refer to *Table 20: Current characteristics* for the maximum allowed injected current values.
3. Include V_{REF-} pin.

Table 29. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Parameter	Conditions (1)	f_{HCLK}	V_{DDA} = 2.4 V				V_{DDA} = 3.6 V				Unit
				Typ	Max @ T_A(2)			Typ	Max @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run mode, code executing from Flash or RAM	HSE bypass	72 MHz	231	254(3)	266	271(3)	251	274(3)	294	300(3)	µA
			64 MHz	203	226	239	243	222	245	261	266	
			48 MHz	153	174	182	186	165	185	198	203	
			32 MHz	105	124	131	133	114	132	141	143	
			24 MHz	82	98	104	105	89	106	111	113	
			8 MHz	3.1	4.1	4.1	5.1	3.6	4.7	5.2	5.5	
			1 MHz	3.1	4.1	4.1	5.1	3.6	4.7	5.2	5.5	
		HSI clock	64 MHz	270	294	307	312	296	322	338	343	
			48 MHz	219	242	253	257	240	263	276	281	
			32 MHz	171	192	201	203	188	209	219	222	
			24 MHz	148	169	175	177	163	182	190	193	
			8 MHz	69	84	87	87	79	92	94	96	

1. Current consumption from the V_{DDA} supply is independent of whether the peripherals are on or off. Furthermore when the PLL is off, I_{DDA} is independent from the frequency.
2. Guaranteed by characterization results.
3. Data based on characterization results and tested in production with code executing from RAM.

Table 30. Typical and maximum V_{DD} consumption in Stop and Standby modes

Symbol	Parameter	Conditions	Typ @V_{DD} (V_{DD}=V_{DDA})						Max(1)			Unit
			2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, all oscillators OFF	16.92	17.09	17.16	17.27	17.39	17.50	29.7	359.1	564.5	µA
		Regulator in low-power mode, all oscillators OFF	5.29	5.46	5.55	5.70	5.73	5.95	16.40	267.1	407.4	
	Supply current in Standby mode	LSI ON and IWDG ON	0.80	0.93	1.11	1.19	1.31	1.41	-	-	-	
		LSI OFF and IWDG OFF	0.63	0.76	0.84	0.95	1.02	1.10	5.00	6.30	12.60	

1. Guaranteed by characterization results.

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- all I/O pins are in analog input configuration
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature at 25°C and $V_{DD} = V_{DDA} = 3.3$ V.

Table 36. Peripheral current consumption

Peripheral	Typical consumption[1]	Unit
	I_{DD}	
BusMatrix [2]	11.3	µA/MHz
DMA1	6.7	
CRC	2.0	
GPIOA	8.5	
GPIOB	8.3	
GPIOC	8.6	
GPIOD	1.5	
GPIOF	1.0	
TSC	4.7	
ADC1	15.9	
APB2-Bridge [3]	2.7	
SYSCFG	3.2	
TIM1	27.6	
USART1	21.0	
TIM15	14.3	
TIM16	10.1	
TIM17	10.4	
APB1-Bridge [3]	5.8	
TIM2	40.7	
TIM6	7.4	
WWDG	4.6	
SPI2	35.2	
SPI3	34.2	
USART2	13.9	
USART3	13.1	
I2C1	9.4	
I2C2	9.4	
USB	17.4	
CAN	28.8	
PWR	4.5	
DAC	8.3	
I2C3	10.5	

1. The power consumption of the analog part (I_{DDA}) of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.
2. BusMatrix is automatically active when at least one master is ON (CPU or DMA1).
3. The APBx bridge is automatically active when at least one peripheral is ON on the same bus.

Low-speed external user clock generated from an external source

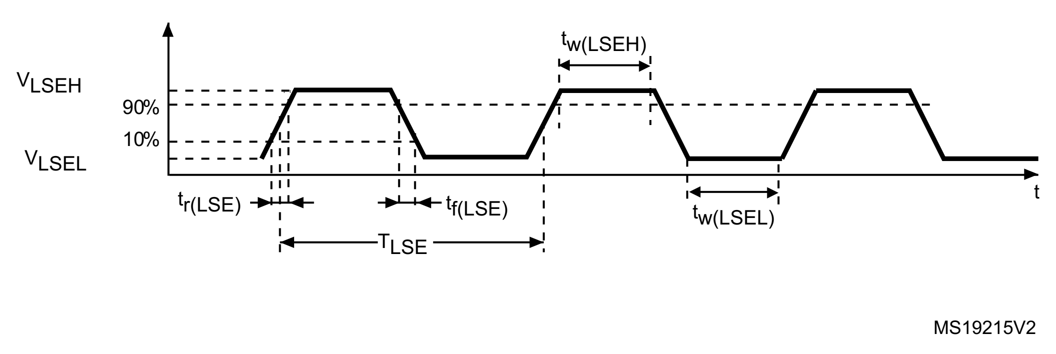
In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 15*

Table 40. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	

1. Guaranteed by design.

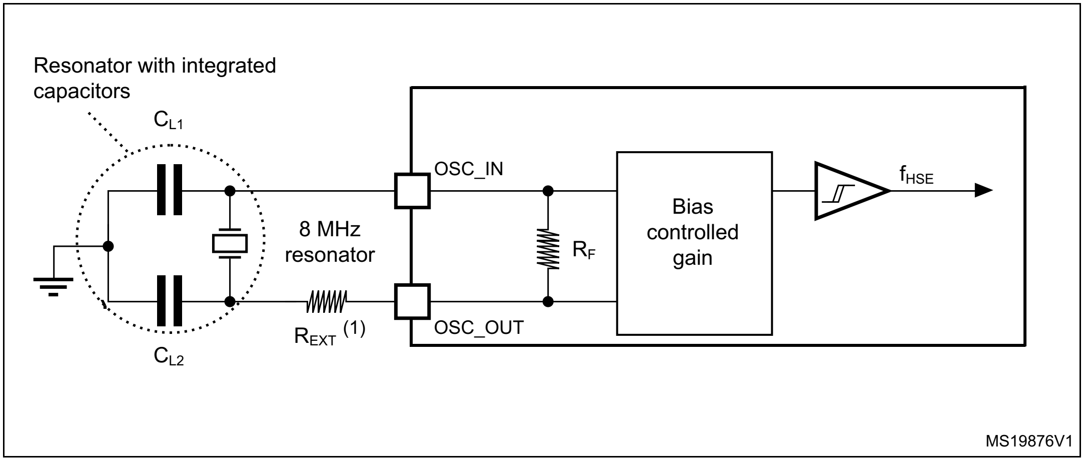
Figure 15. Low-speed external clock source AC timing diagram



For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 16*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 16. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 42*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

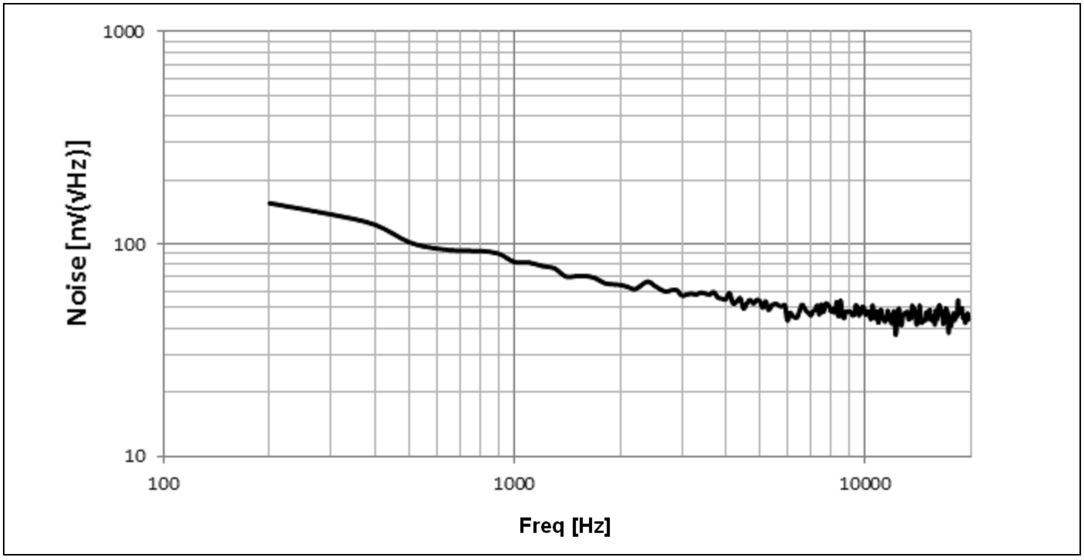
Table 42. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
I_{DD}	LSE current consumption	LSEDRV[1:0]=00 lower driving capability	-	0.5	0.9	µA
		LSEDRV[1:0]=10 medium low driving capability	-	-	1	
		LSEDRV[1:0]=01 medium high driving capability	-	-	1.3	
		LSEDRV[1:0]=11 higher driving capability	-	-	1.6	
g_m	Oscillator transconductance	LSEDRV[1:0]=00 lower driving capability	5	-	-	µA/V
		LSEDRV[1:0]=10 medium low driving capability	8	-	-	
		LSEDRV[1:0]=01 medium high driving capability	15	-	-	
		LSEDRV[1:0]=11 higher driving capability	25	-	-	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

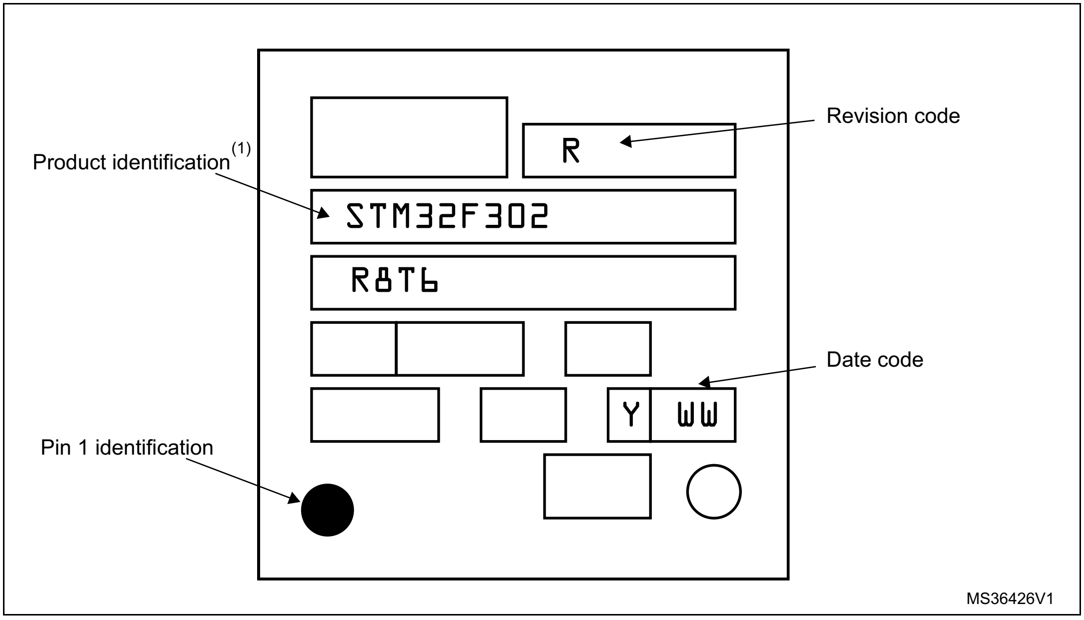
Figure 36. OPAMP Voltage Noise versus Frequency



Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

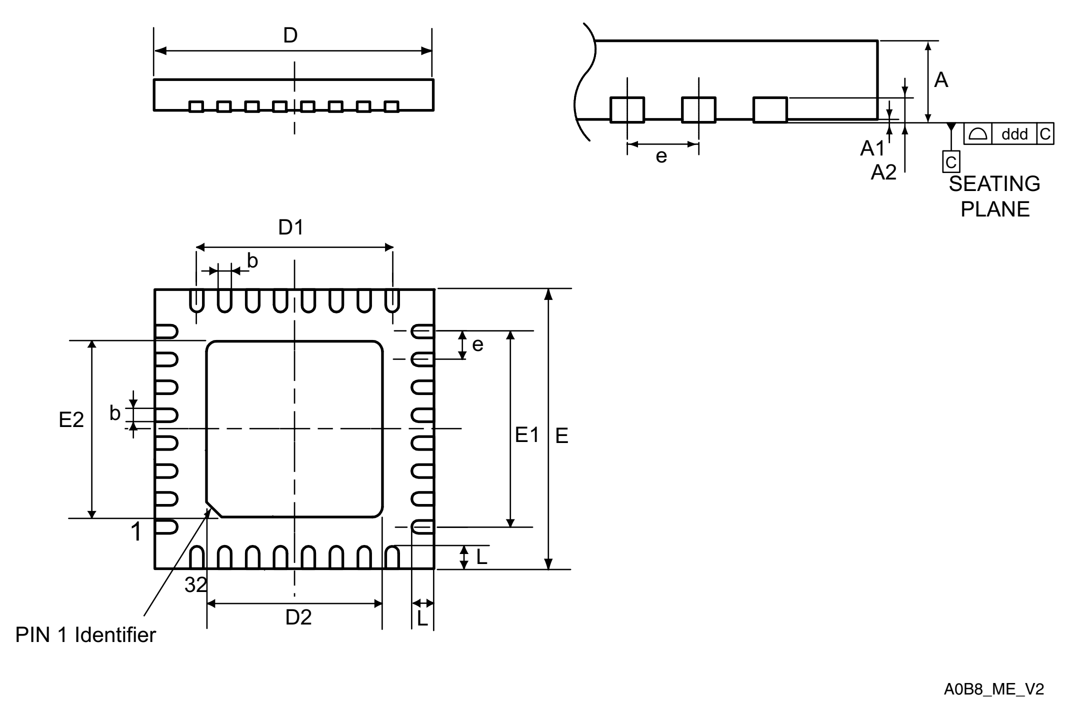
Figure 42. LQFP64 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.4 UFQFPN32 package information

Figure 46. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline



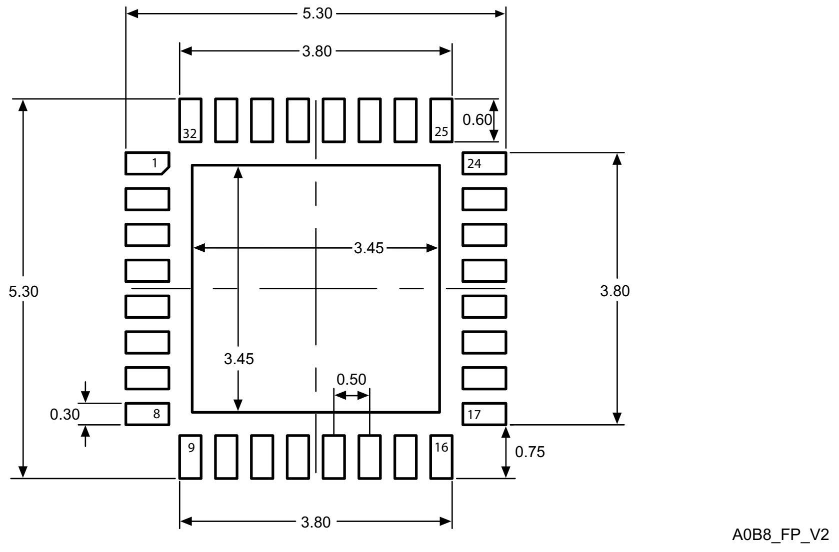
1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. This pad is used for the device ground and must be connected. It is referred to as pin 0 in Table: Pin definitions.

Table 81. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	0.230	0.280	0.0071	0.0091	0.0110
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	3.500	3.600	0.1339	0.1378	0.1417
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E	4.900	5.000	5.100	0.1929	0.1969	0.2008
E1	3.400	3.500	3.600	0.1339	0.1378	0.1417
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 47. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.