STMicroelectronics - STM32F302VCT7TR Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	87
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 17x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f302vct7tr

Email: info@E-XFL.COM
Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Table 1. STM32F302x6/8 device features and peripheral counts

Peripheral		STM32F302Kx		STM32F302Cx		STM32F302Rx	
Flash (Kbytes)		32	64	32	64	32	64
SRAM (Kbytes)		16					
Timers	Advanced control	1 (16-bit)					
	General purpose	3 (16-bit) 1 (32 bit)					
	Basic	1					
	SysTick timer	1					
	Watchdog timers (independent, window)	2					
	PWM channels (all)(1)	16		18			
	PWM channels (except complementary)	10		12			
Comm. interfaces	SPI/I2S	2					
	I^2C	3					
	USART	2		3			
	USB 2.0 FS	1					
	CAN 2.0B	1					
GPIOs	Normal I/Os (TC, TTa)	9		20		26	
	5-Volt tolerant I/Os (FT, FT1)	15		17		25	
DMA channels		7					
Capacitive sensing channels		13		17		18	
12-bit ADC Number of channels		1 8		1 11		1 15	
12-bit DAC channels		1					
Analog comparator		2		3		3	
Operational amplifier		1					
CPU frequency		72 MHz					
Operating voltage		2.0 to 3.6 V					
Operating temperature		Ambient operating temperature: - 40 to 85 °C / - 40 to 105 °C Junction temperature: - 40 to 125 °C					
Packages		UFQFPN32		LQFP48, WLCSP49		LQFP64	

1. This total number considers also the PWMs generated on the complementary output channels.

3.11.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC1_IN17. As the V_{BAT} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

3.12 Digital-to-analog converter (DAC)

One 12-bit buffered DAC channel (DAC1_OUT1) can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- One DAC output channel
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- DMA capability
- External triggers for conversion

3.13 Operational amplifier (OPAMP)

The STM32F302x6/8 devices embed one operational amplifier with external or internal follower routing and PGA capability (or even amplifier and filter capability with external components). When the operational amplifier is selected, an external ADC channel is used to enable output measurement.

The operational amplifier features:

- 8.2 MHz bandwidth
- 0.5 mA output capability
- Rail-to-rail input/output
- In PGA mode, the gain can be programmed to be 2, 4, 8 or 16.

Table 9. Capacitive sensing GPIOs available on STM32F302x6/8 devices

Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0
	TSC_G1_IO2	PA1
	TSC_G1_IO3	PA2
	TSC_G1_IO4	PA3
2	TSC_G2_IO1	PA4
	TSC_G2_IO2	PA5
	TSC_G2_IO3	PA6
	TSC_G2_IO4	PA7
3	TSC_G3_IO1	PC5
	TSC_G3_IO2	PB0
	TSC_G3_IO3	PB1
	TSC_G3_IO4	PB2
4	TSC_G4_IO1	PA9
	TSC_G4_IO2	PA10
	TSC_G4_IO3	PA13
	TSC_G4_IO4	PA14
5	TSC_G5_IO1	PB3
	TSC_G5_IO2	PB4
	TSC_G5_IO3	PB6
	TSC_G5_IO4	PB7
6	TSC_G6_IO1	PB11
	TSC_G6_IO2	PB12
	TSC_G6_IO3	PB13
	TSC_G6_IO4	PB14

Table 10. No. of capacitive sensing channels available on STM32F302x6/8 devices

Analog I/O group	Number of capacitive sensing channels		
	STM32F302Rx	STM32F302Cx	STM32F302Kx
G1	3	3	3
G2	3	3	3
G3	3	2	1
G4	3	3	3
G5	3	3	3

Table 15. Alternate functions for Port C

Port & pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SYS_AF	TIM2/TIM15/ TIM16/TIM17/ EVENT	I2C3/TIM1/TIM2 /TIM15	I2C3/TIM15/ TSC	I2C1/I2C2/TIM1/ TIM16/TIM17	SPI2/I2S2/ SPI3/I2S3 Infrared	SPI2/I2S2/SPI3/ I2S3/TIM1/ Infrared	USART1/ USART2/ USART3/CAN/ GPCOMP6
PC0	-	EVENTOUT	TIM1_CH1	-	-	-	-	-
PC1	-	EVENTOUT	TIM1_CH2	-	-	-	-	-
PC2	-	EVENTOUT	TIM1_CH3	-	-	-	-	-
PC3	-	EVENTOUT	TIM1_CH4	-	-	-	TIM1_BKIN2	-
PC4	-	EVENTOUT	TIM1_ETR	-	-	-	-	USART1_TX
PC5	-	EVENTOUT	TIM15_BKIN	TSC_G3_IO1	-	-	-	USART1_RX
PC6	-	EVENTOUT	-	-	-	-	I2S2_MCK	COMP6_OUT
PC7	-	EVENTOUT	-	-	-	-	I2S3_MCK	-
PC8	-	EVENTOUT	-	-	-	-	-	-
PC9	-	EVENTOUT	-	I2C3_SDA	-	I2SCKIN	-	-
PC10	-	EVENTOUT	-	-	-	-	SPI3_SCK/ I2S3_CK	USART3_TX
PC11	-	EVENTOUT	-	-	-	-	SPI3_MISO/ I2S3ext_SD	USART3_RX
PC12	-	EVENTOUT	-	-	-	-	SPI3_MOSI/ I2S3_SD	USART3_CK
PC13	-	-	-	-	TIM1_CH1N	-	-	-
PC14	-	-	-	-	-	-	-	-
PC15	-	-	-	-	-	-	-	-

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 23* are derived from tests performed under the ambient temperature condition summarized in *Table 22*.

Table 23. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		20	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		20	∞	

6.3.3 Embedded reset and power control block characteristics

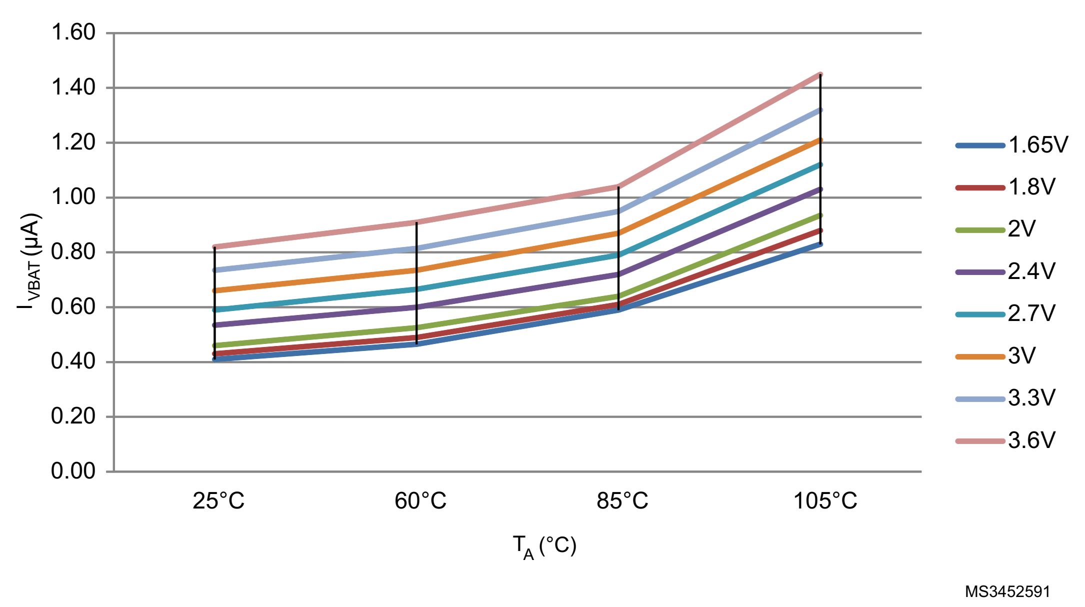
The parameters given in *Table 24* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22*.

Table 24. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{POR/PDR}$(1)	Power on/power down reset threshold	Falling edge	1.8(2)	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$(1)	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$(3)	POR reset temporization	-	1.5	2.5	4.5	ms

1. The PDR detector monitors V_{DD} and also V_{DDA} (if kept enabled in the option bytes). The POR detector monitors only V_{DD}.
2. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
3. Based on characterization, not tested in production.

Figure 13. Typical V_{BAT} current consumption (LSE and RTC ON/LSEDRV[1:0] = ‘00’)



Typical current consumption

The MCU is placed under the following conditions:

- $V_{DD} = V_{DDA} = 3.3$ V
- All I/O pins available on each package are in analog input configuration
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait states from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 MHz to 72 MHz), and Flash prefetch is ON
- When the peripherals are enabled, $f_{APB1} = f_{AHB/2}$, $f_{APB2} = f_{AHB}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8,16 and 64 is used for the frequencies 4 MHz, 2 MHz, 1 MHz, 500 kHz and 125 kHz respectively.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 53: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see*Table 36: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

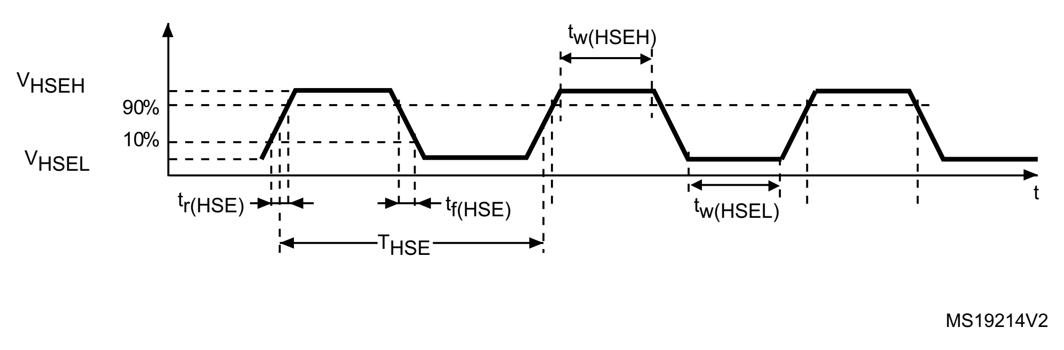
In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 14*.

Table 39. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency[1]	-	1	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time[1]		15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time[1]		-	-	20	

1. Guaranteed by design.

Figure 14. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

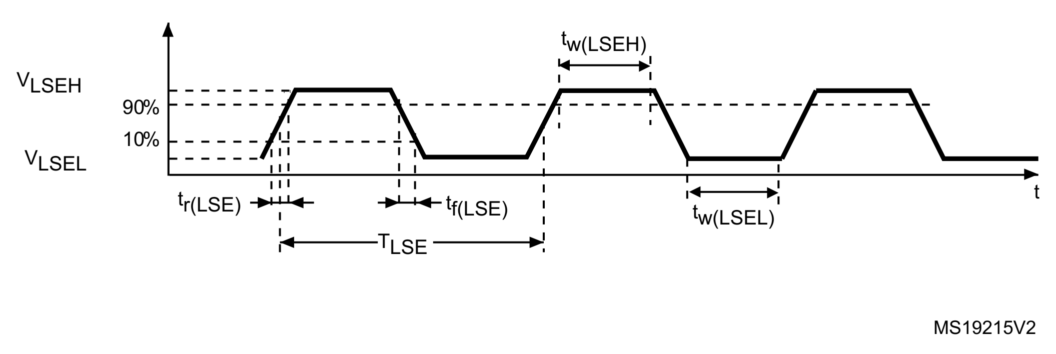
In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 15*

Table 40. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	

1. Guaranteed by design.

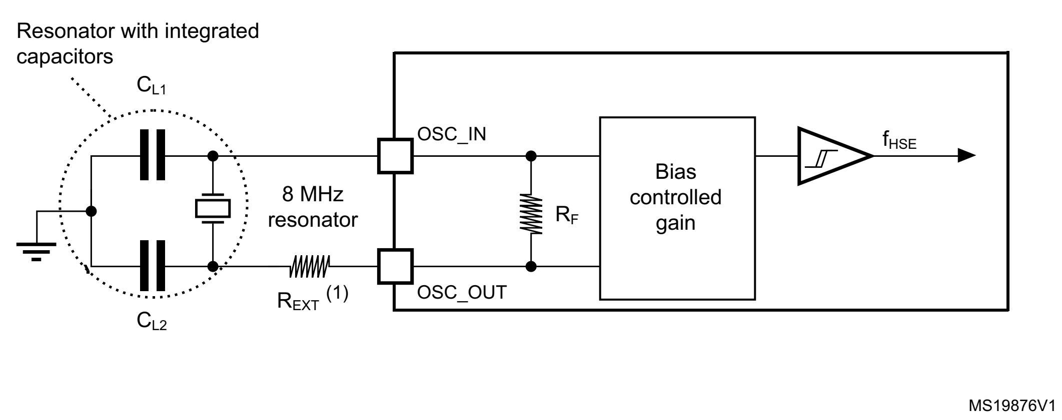
Figure 15. Low-speed external clock source AC timing diagram



For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 16*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

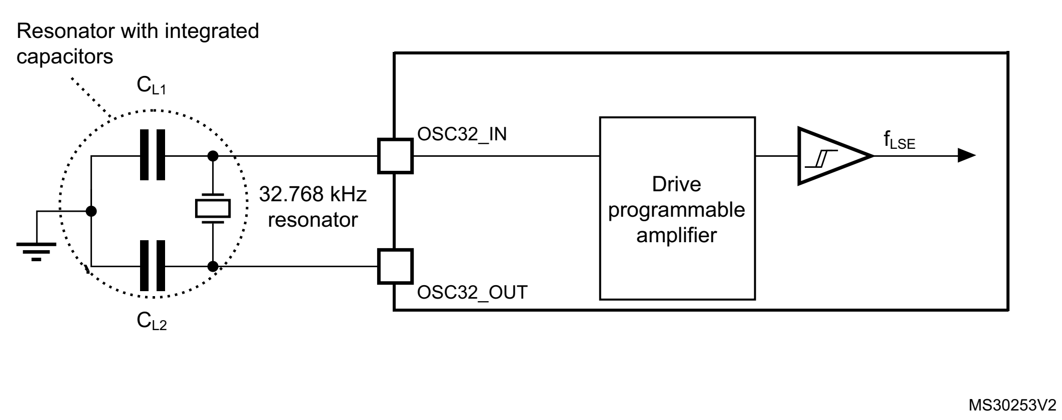
Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 16. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Figure 17. Typical application with a 32.768 kHz crystal



Note: *An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.*

Low-speed internal (LSI) RC oscillator

Table 44. LSI oscillator characteristics[1]

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	50	kHz
$t_{su(LSI)}$[2]	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$[2]	LSI oscillator power consumption	-	0.75	1.2	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design.

6.3.9 PLL characteristics

The parameters given in *Table 45* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22*.

Table 45. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL input clock[1]	1[2]	-	24[2]	MHz
	PLL input clock duty cycle	40[2]	-	60[2]	%
f_{PLL_OUT}	PLL multiplier output clock	16[2]	-	72	MHz
t_{LOCK}	PLL lock time	-	-	200[2]	µs
Jitter	Cycle-to-cycle jitter	-	-	300[2]	ps

1. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.
2. Guaranteed by design.

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 48*. They are based on the EMS levels and classes defined in application note AN1709.

Table 48. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP64, T_A = +25°C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP64, T_A = +25°C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

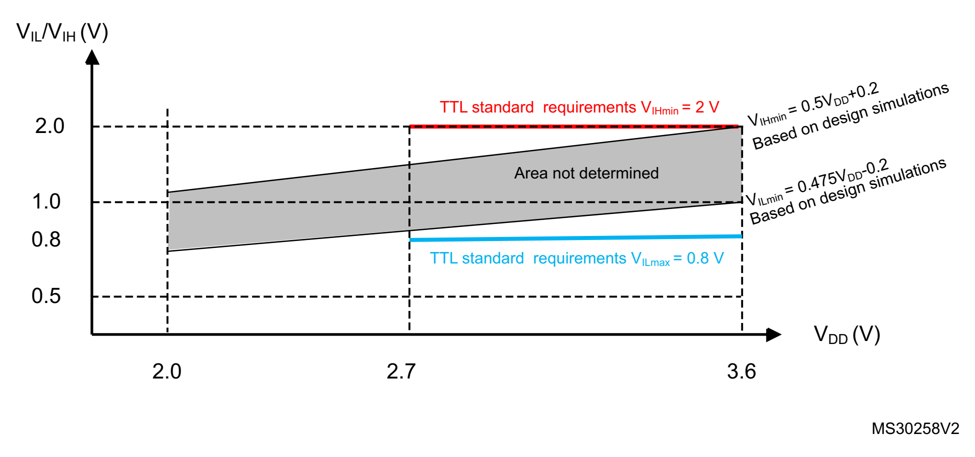
Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Figure 22. Five volt tolerant (FT and FTf) I/O input characteristics - TTL port



6.3.17 Communications interfaces

I^2C interface characteristics

The I2C interface meets the timings requirements of the I^2C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I2C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.14: I/O port characteristics* for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 60. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

1. Guaranteed by design.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

Figure 25. SPI timing diagram - slave mode and CPHA = 0

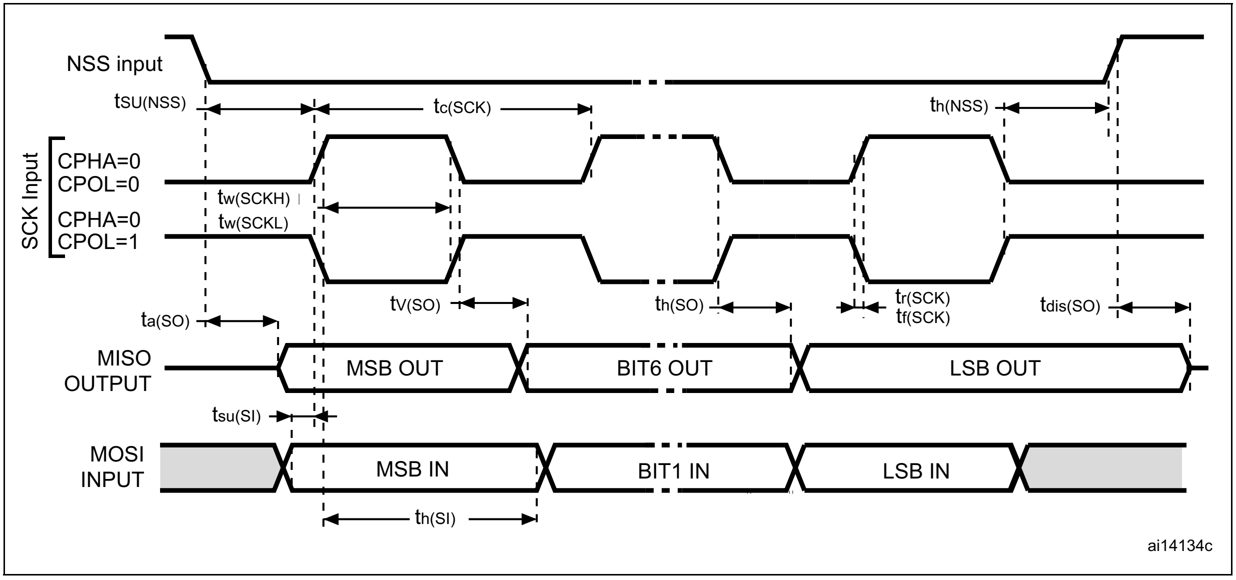
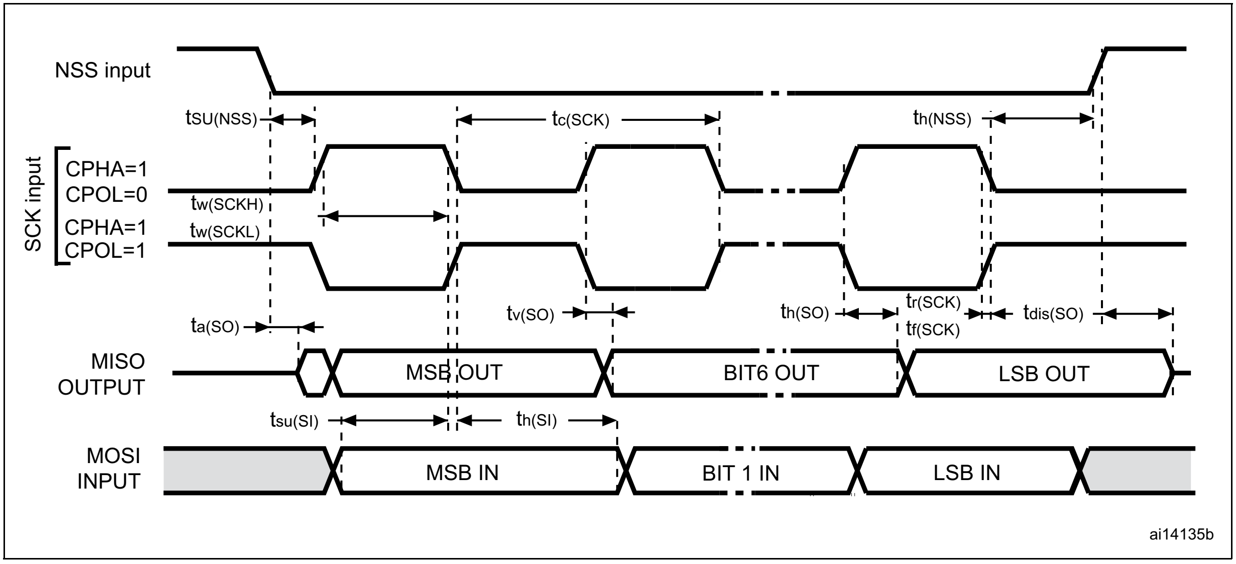


Figure 26. SPI timing diagram - slave mode and CPHA = 1[(1)]



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

USB characteristics

Table 63. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design.

Table 64. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels					
V_{DD}	USB operating voltage(2)		3.0(3)	3.6	V
V_{DI}(4)	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	V
V_{CM}(4)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(4)	Single ended receiver threshold		1.3	2.0	
Output levels					
V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(5)	-	0.3	V
V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(5)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. The STM32F3xxx USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
4. Guaranteed by design.
5. R_L is the load connected on the USB drivers.

Figure 30. USB timings: definition of data signal rise and fall time

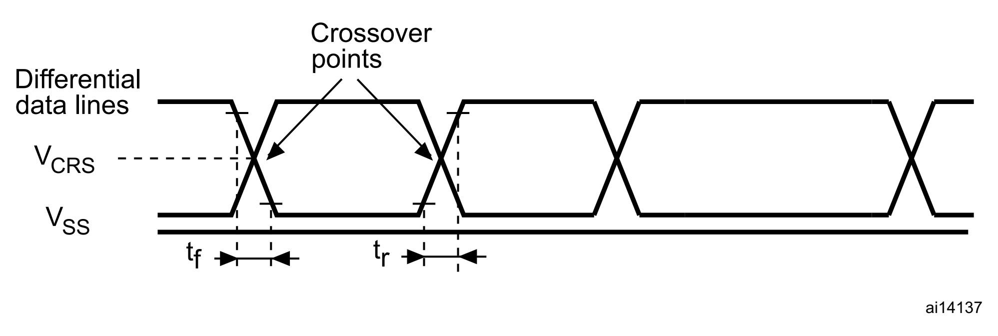


Table 65. USB: Full-speed electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver characteristics						
t_r	Rise time(2)	C_L = 50 pF	4	-	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	-	20	ns

Figure 31 illustrates the ADC current consumption as per the clock frequency in single-ended and differential modes.

Figure 31. ADC typical current consumption in single-ended and differential modes

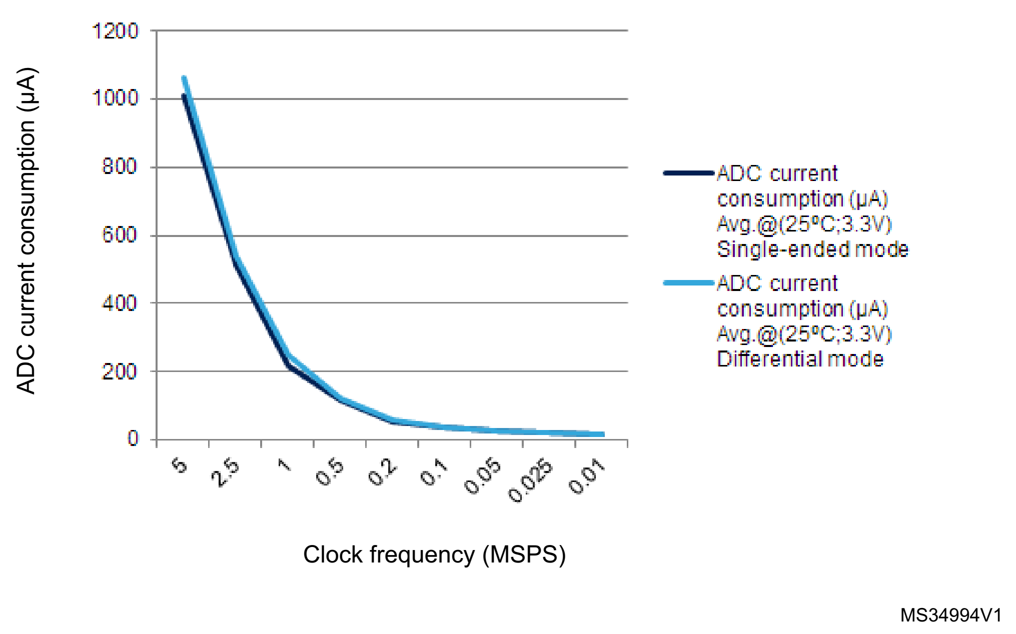


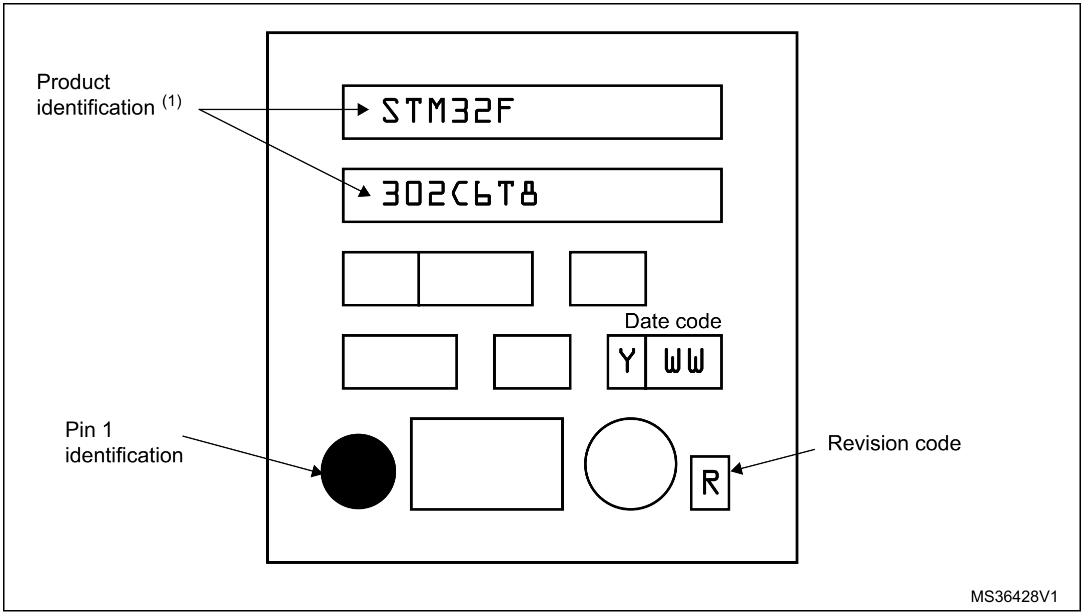
Table 67. Maximum ADC R_{AIN} [1]

Resolution	Sampling cycle @ 72 MHz	Sampling time [ns] @ 72 MHz	R_{AIN} max (kΩ)		
			Fast channels[2]	Slow channels	Other channels[3]
12 bits	1.5	20.83	0.018	NA	NA
	2.5	34.72	0.150	NA	0.022
	4.5	62.50	0.470	0.220	0.180
	7.5	104.17	0.820	0.560	0.470
	19.5	270.83	2.70	1.80	1.50
	61.5	854.17	8.20	6.80	4.70
	181.5	2520.83	22.0	18.0	15.0
	601.5	8354.17	82.0	68.0	47.0

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 45. LQFP48 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.