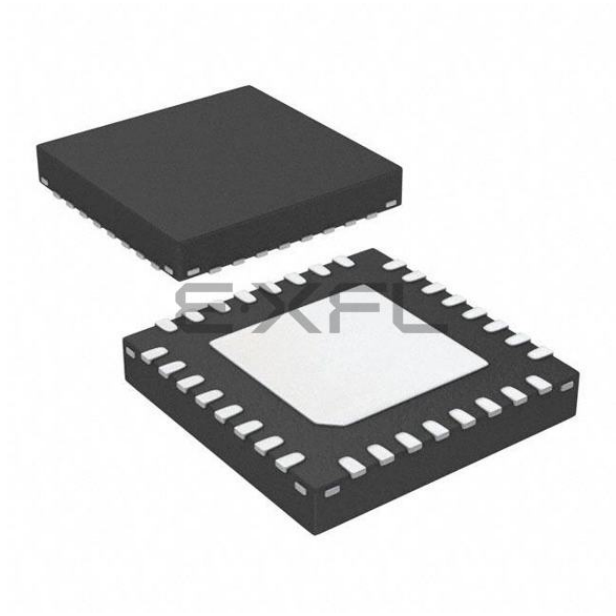

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	24
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/m0516zbn

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LIST OF FIGURES

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- Up to two sets of UART device
- Programmable baud-rate generator
- Buffered receiver and transmitter, each with 15 bytes FIFO
- Optional flow control function (CTS and RTS)
- Supports IrDA(SIR) function
- Supports RS485 function
- Supports LIN function

- SPI
  - Up to two sets of SPI device.
  - Supports master/slave mode
  - Full duplex synchronous serial data transfer
  - Provide 3 wire function
  - Variable length of transfer data from 1 to 32 bits
  - MSB or LSB first data transfer
  - Rx latching data can be either at rising edge or at falling edge of serial clock
  - Tx sending data can be either at rising edge or at falling edge of serial clock
  - Supports Byte suspend mode in 32-bit transmission
- I^2C
  - Supports master/slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master).
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.

3 BLOCK DIAGRAM

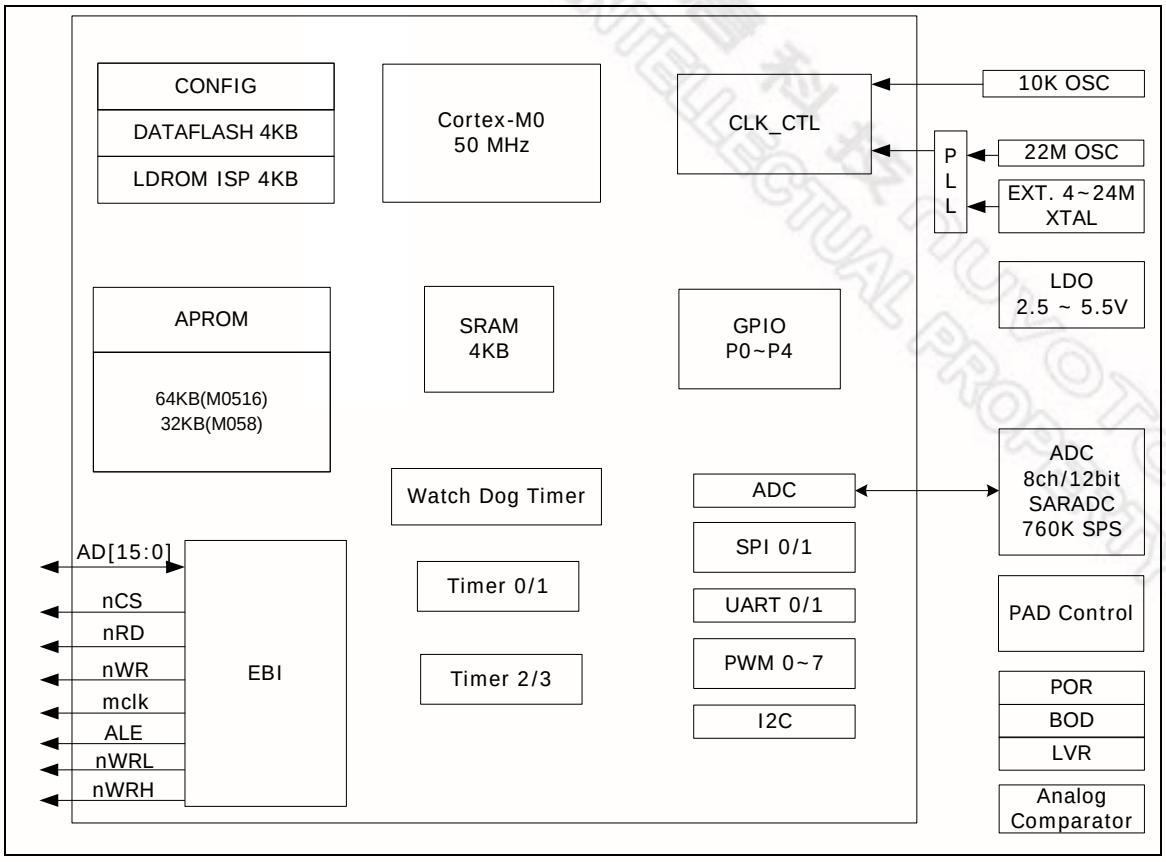

Figure 3-1 NuMicro™ M051 Series Block Diagram

5 PIN CONFIGURATION

5.1 QFN 33 pin

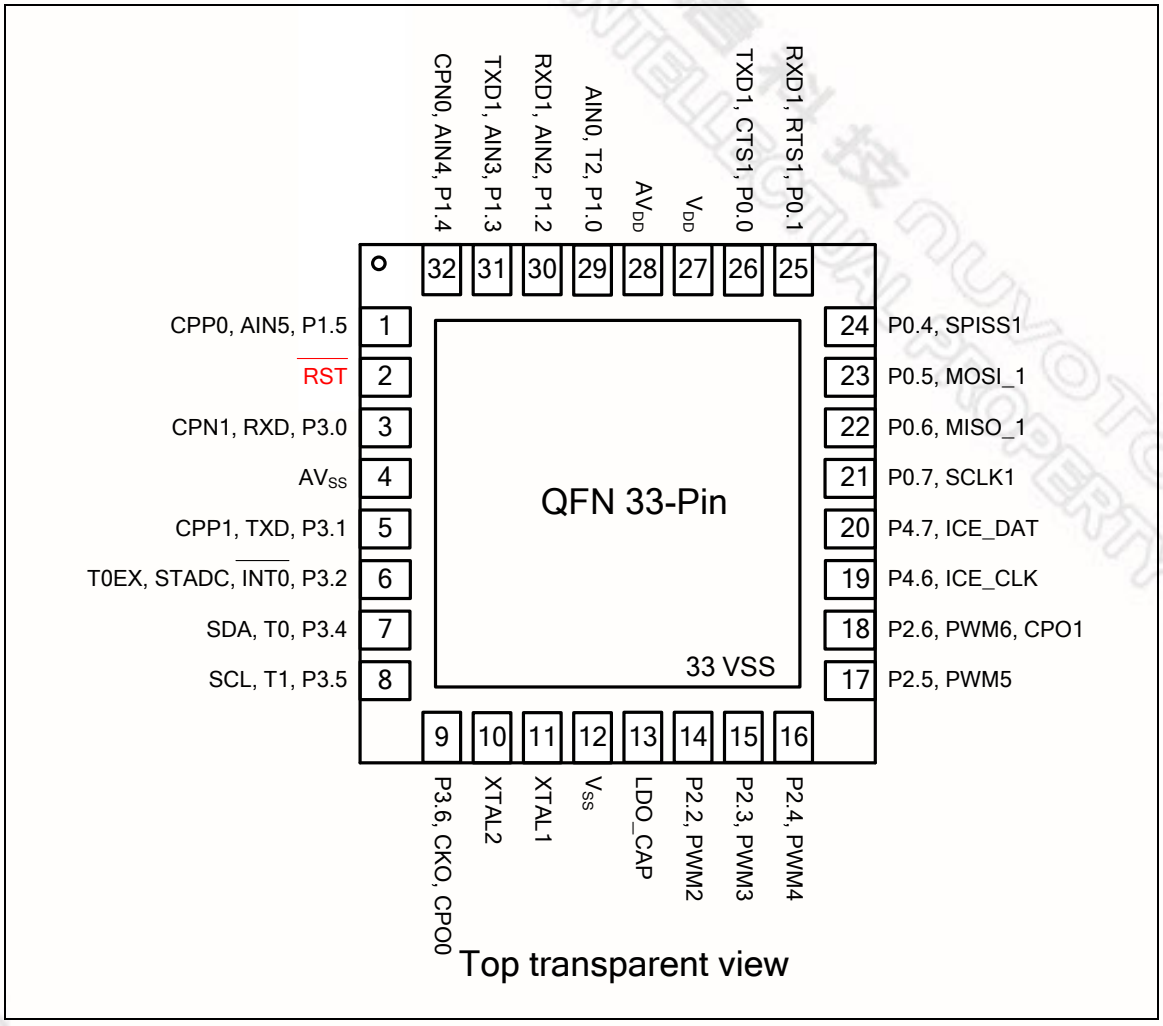

Figure 5-1 NuMicro™ M051 Series QFN33 Pin Diagram

- Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling.
- C Application Binary Interface compliant exception model.
  This is the ARMv6-M, C Application Binary Interface(C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers.
- Low power sleep-mode entry using Wait For Interrupt (WFI), Wait For Event(WFE) instructions, or the return from interrupt sleep-on-exit feature.

NVIC features:

- 32 external interrupt inputs, each with four levels of priority.
- Dedicated non-Maskable Interrupt (NMI) input.
- Support for both level-sensitive and pulse-sensitive interrupt lines
- Wake-up Interrupt Controller (WIC), supports ultra-low power sleep mode.

Debug support:

- Four hardware breakpoints.
- Two watchpoints.
- Program Counter Sampling Register (PCSR) for non-intrusive code profiling.
- Single step and vector catch capabilities.

Bus interfaces:

- Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory.
- Single 32-bit slave port that supports the DAP (Debug Access Port).

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6.3 Clock Controller

6.3.1 Overview

The clock controller generates the clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip will not enter power-down mode until CPU sets the power down enable bit (PWR_DOWN_EN) and Cortex-M0 core executes the WFI instruction. After that, chip enter power-down mode and wait for wake-up interrupt source triggered to leave power-down mode. In the power down mode, the clock controller turns off the external crystal and internal 22.1184 MHz oscillator to reduce the overall system power consumption.

6.3.2 Clock Generator Block Diagram

The clock generator consists of 4 sources which list below:

- One external 4~24 MHz crystal
- One internal 22.1184 MHz RC oscillator
- One programmable PLL FOUT(PLL source consists of external 4~24 MHz crystal and internal 22.1184M)
- One internal 10 kHz oscillator

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6.4 General Purpose I/O

6.4.1 Overview

There are 40 General Purpose I/O pins shared with special feature functions in this MCU. The 40 pins are arranged in 5 ports named with P0, P1, P2, P3 and P4. Each port equips maximum 8 pins. Each one of the 40 pins is independent and has the corresponding register bits to control the pin mode function and data

The I/O type of each of I/O pins can be software configured individually as input, output, open-drain or quasi-bidirectional mode. The all pins of I/O type stay in quasi-bidirectional mode and port data register Px_DOUT[7:0] resets to 0x000_00FF. Each I/O pin equips a very weakly individual pull-up resistor which is about 110KΩ~300KΩ for V_{DD} is from 5.0V to 2.5V.

6.4.1.1 Input Mode Explanation

Set Px_PMD(PMDn[1:0]) to 00b the Px[n] pin is in Input mode and the I/O pin is in tri-state(high impedance) without output drive capability. The Px_PIN value reflects the status of the corresponding port pins.

6.4.1.2 Output Mode Explanation

Set Px_PMD(PMDn[1:0]) to 2'b01 the Px[n] pin is in Output mode and the I/O pin supports digital output function with source/sink current capability. The bit value in the corresponding bit [n] of Px_DOUT is driven on the pin.

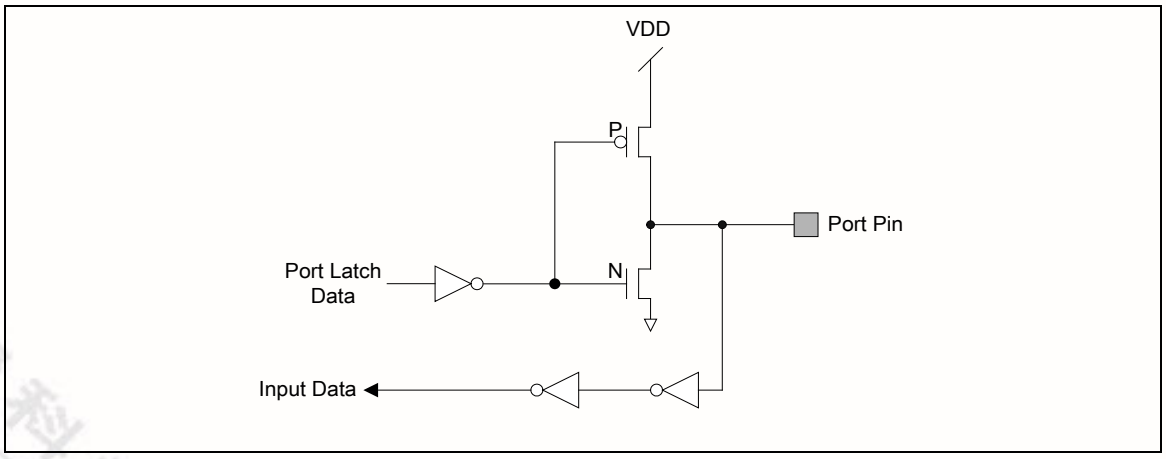

Figure 6-10 Push-Pull Output

6.7 Serial Peripheral Interface (SPI)

6.7.1 Overview

The Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol which operates in full duplex mode. Devices communicate in master/slave mode with 4-wire bi-direction interface. NuMicro M051™ series contains up to two sets of SPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each set of SPI controller can be set as a master, it also can be configured as a slave device controlled by an off-chip master device. This controller supports a variable serial clock for special application.

6.7.2 Features

- Up to two sets of SPI controller
- Support master or slave mode operation
- Configurable bit length up to 32-bit of a transfer word and configurable word numbers up to 2 of a transaction, so the maximum bit length is 64-bit for each data transfer
- Provide burst mode operation, transmit/receive can be transferred up to two times word transaction in one transfer
- Support MSB or LSB first transfer
- Support byte reorder function
- Support byte or word suspend mode
- Support two programmable serial clock frequencies in master mode
- Support three wire, no slave select signal, bi-direction interface
- The SPI clock rate can be configured to equal the system clock rate

6.11 Analog-to-Digital Converter (ADC)

6.11.1 Overview

NuMicro M051™ series contain one 12-bit successive approximation analog-to-digital converters (SAR A/D converter) with 8 input channels. The A/D converter supports four operation modes: single, burst, single-cycle scan and continuous scan mode. The A/D converters can be started by software and external STADC/P3.2 pin.

6.11.2 Features

- Analog input voltage range: 0~AV_{DD} (Max to 5.0V).
- 12-bit resolution and 10-bit accuracy is guaranteed.
- Up to 8 single-end analog input channels or 4 differential analog input channels.
- Maximum ADC clock frequency is 16 MHz.
- Up to 760k SPS conversion rate.
- Four operating modes
  - Single mode: A/D conversion is performed one time on a specified channel.
  - Single-cycle scan mode: A/D conversion is performed one cycle on all specified channels with the sequence from the lowest numbered channel to the highest numbered channel.
  - Continuous scan mode: A/D converter continuously performs Single-cycle scan mode until software stops A/D conversion.
  - Burst mode: A/D conversion will sample and convert the specified single channel and sequentially store in FIFO.
- An A/D conversion can be started by
  - Software Write 1 to ADST bit
  - External pin STADC
- Conversion results are held in data registers for each channel with valid and overrun indicators.
- Conversion result can be compared with specify value and user can select whether to generate an interrupt when conversion result matches the compare register setting.

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6.13 Flash Memory Controller (FMC)

6.13.1 Overview

NuMicro M051™ series equips with 32K/64K bytes on chip embedded Flash EEPROM for application program memory (APROM) that can be updated through ISP/IAP procedure. In System Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip power on Cortex-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in Config0. By the way, NuMicro M051™ series also provide additional 4K bytes DATA Flash for user to store some application depended data before chip power off in 64/32K bytes APROM model.

6.13.2 Features

- Run up to 50 MHz with zero wait state for continuous address read access
- 32/64KB application program memory (APROM)
- 4KB in system programming (ISP) loader program memory (LDROM)
- Fixed 4KB data flash with 512 bytes page erase unit
- In System Program (ISP)/In Application Program (IAP) to update on chip Flash EPROM

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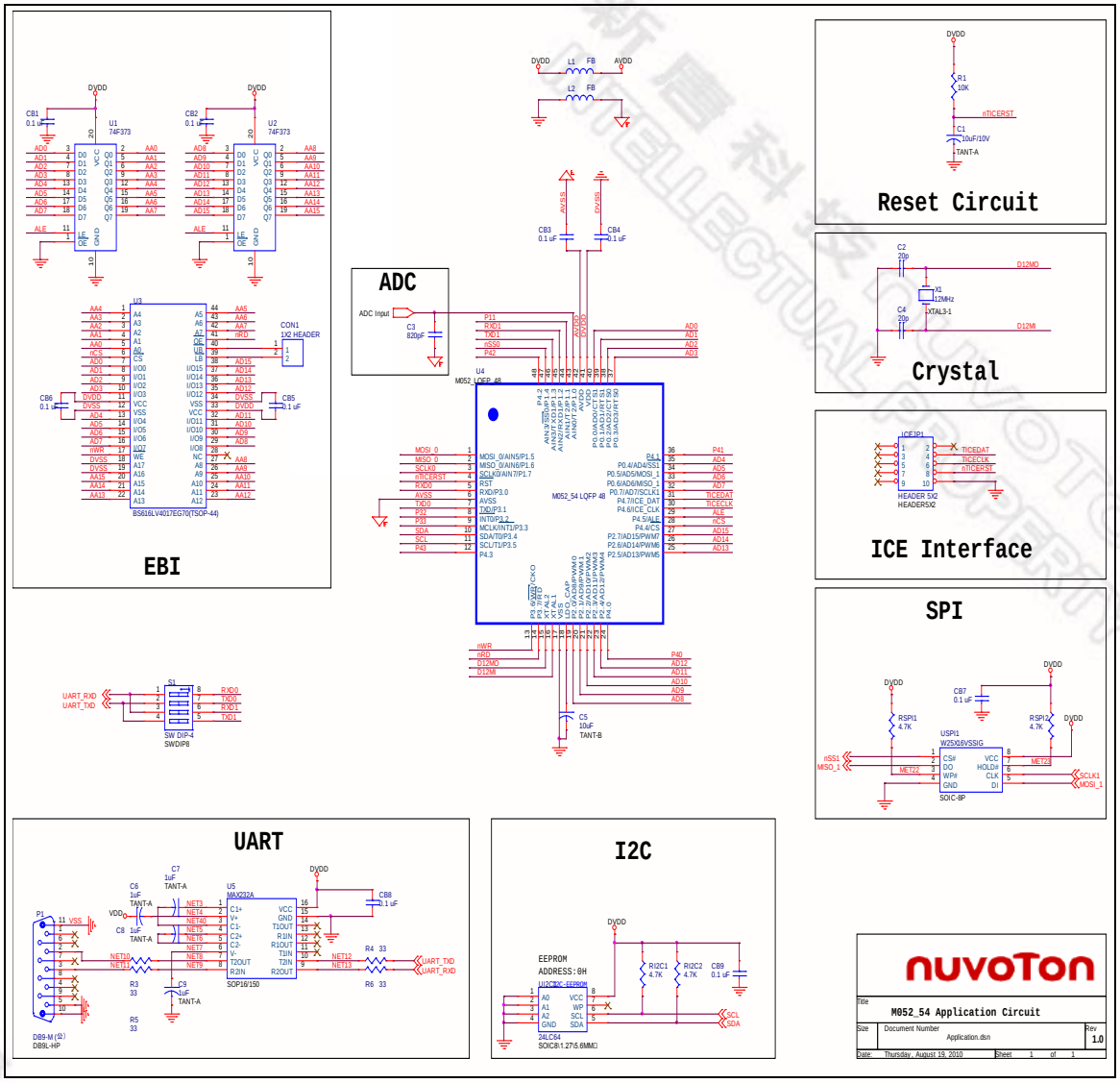
7 TYPICAL APPLICATION CIRCUIT



8.2 DC Electrical Characteristics

(V_{DD} -V_{SS}=2.5~5.5V, TA = 25°C, F_{OSC} = 50 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	2.5		5.5	V	V_{DD} =2.5V ~ 5.5V up to 50 MHz
LDO Output Voltage	V_{LDO}	1.7	1.8	1.9	V	V_{DD} ≥ 2.5V
Band Gap Analog Input	V_{BG}	-5%	1.20	+5%	V	V_{DD} =2.5V ~ 5.5V
Analog Operating Voltage	AV_{DD}	0		V_{DD}	V	
Analog Reference Voltage	Vref	0		AV_{DD}	V	
Operating Current Normal Run Mode @ 50 MHz	IDD1		20.6		mA	V_{DD} = 5.5V@50MHz, enable all IP and PLL, XTAL=12MHz
	IDD2		14.4		mA	V_{DD} =5.5V@50MHz, disable all IP and enable PLL, XTAL=12MHz
	IDD3		18.9		mA	V_{DD} = 3.3V@50MHz, enable all IP and PLL, XTAL=12MHz
	IDD4		12.8		mA	V_{DD} = 3.3V@50MHz, disable all IP and enable PLL, XTAL=12MHz
Operating Current Normal Run Mode @ 22Mhz	IDD5		6.2		mA	V_{DD} = 5.5V@22MHz, enable all IP and IRC22M, disable PLL
	IDD6		3.4		mA	V_{DD} =5.5V@22MHz, disable all IP and enable IRC22M, disable PLL
	IDD7		6.1		mA	V_{DD} = 3.3V@22MHz, enable all IP and IRC22M, disable PLL
	IDD8		3.4		mA	V_{DD} = 3.3V@22MHz, disable all IP and enable IRC22M, disable PLL
Operating Current Normal Run Mode @ 12Mhz	IDD9		5.3		mA	V_{DD} = 5.5V@12MHz, enable all IP and disable PLL, XTAL=12MHz
	IDD10		3.7		mA	V_{DD} = 5.5V@12MHz, disable all IP and disable PLL, XTAL=12MHz
	IDD11		4.0		mA	V_{DD} = 3.3V@12MHz, enable all IP and disable PLL, XTAL=12MHz

8.3.4 Internal 22.1184 MHz RC Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Center Frequency	-	-	22.1184		MHz
Calibrated Internal Oscillator Frequency	+25□C; V_{DD} =5V	-3	-	+3	%
	-40□C~+85□C; V_{DD}=2.5V~5.5V	-5	-	+5	%
Operating current	V_{DD} =5V	-	500	-	uA

8.3.5 Internal 10kHz RC Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage[1]	-	2.5	-	5.5	V
Center Frequency	-	-	10	-	kHz
Calibrated Internal Oscillator Frequency	+25□C; V_{DD} =5V	-30	-	+30	%
	-40□C~+85□C; V_{DD}=2.5V~5.5V	-50	-	+50	%
Operating current	V_{DD} =5V	-	5	-	uA

Notes:

1. Internal operation voltage comes from LDO.

8.4.2 Specification of LDO & Power management

RAMETER	MIN	TYP	MAX	UNIT	NOTE
Input Voltage	2.5	5	5.5	V	V_{DD} input voltage
Output Voltage	-10%	1.8	+10%	V	LDO output voltage
Temperature	-40	25	85	℃	
C	-	1u	-	F	Resr=1ohm

Note:

1. It is recommended a 100nF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.
2. For ensuring power stability, a 1uF or higher capacitor must be connected between LDO pin and the closest V_{SS} pin of the device.

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8.4.3 Specification of Low Voltage Reset

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	2.5	5	5.5	V
Temperature	-	-40	25	85	℃
Quiescent current	V_{DD} =5.5V	-	-	5	uA
Threshold voltage	Temperature=25°	1.7	2.0	2.3	V
	Temperature=-40°	-	2.3	-	V
	Temperature=85°	-	1.8	-	V
Hysteresis	-	0	0	0	V

8.4.4 Specification of Brown-Out Detector

Parameter	Condition	Min.	Typ.	Max.	Unit
Operation voltage	-	2.5	-	5.5	V
Quiescent current	AV_{DD} =5.5V	-	-	140	μA
Temperature	-	-40	25	85	℃
Brown-Out voltage	BOV_VL[1:0]=11	4.1	4.3	4.5	V
	BOV_VL [1:0]=10	3.5	3.7	3.9	V
	BOV_VL [1:0]=01	2.5	2.7	2.9	V
	BOV_VL [1:0]=00	2.0	2.2	2.4	V
Hysteresis	-	30m	-	150m	V

8.4.5 Specification of Power-On Reset (5V)

Parameter	Condition	Min.	Typ.	Max.	Unit
Temperature	-	-40	25	85	℃
Reset voltage	V+	-	2	-	V

Quiescent current	Vin>reset voltage	-	1	-	nA

8.4.6 Specification of Temperature Sensor

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltage[1]		1.62	1.8	1.98	V
Temperature		-40	-	85	℃
Gain		-1.72	-1.76	-1.80	mV/℃
Offset	Temp=0 ℃	717	725	733	mV

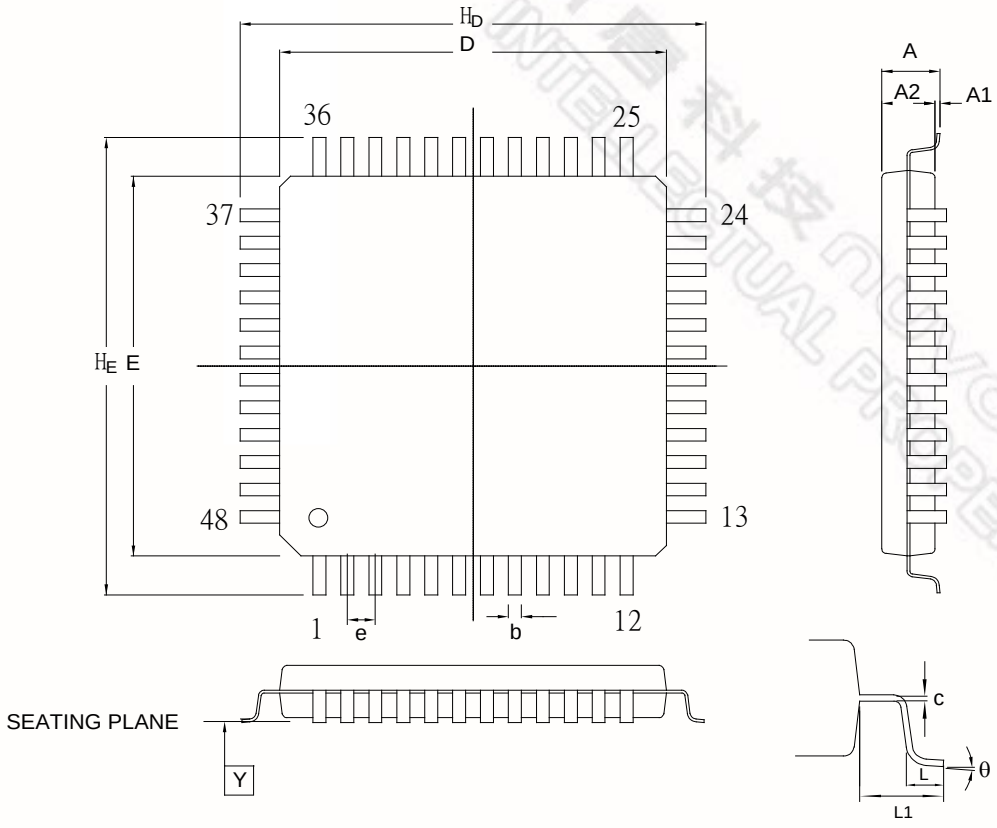
Note[1]: Internal operation voltage comes from LDO.

8.4.7 Specification of Comparator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Temperature	-	-40	25	85	℃
V_{DD}	-	2.4	3	5.5	V
V_{DD} current	-	-	40	80	uA
Input offset voltage	-		10	20	mV
Output swing	-	0.1	-	V_{DD} -0.1	V
Input common mode range	-	0.1	-	V_{DD} -0.1	V
DC gain	-	-	70	-	dB
Propagation delay	@VCM=1.2 V and VDIFF=0.1 V	-	200	-	ns
Hysteresis	@VCM=0.2 V ~ V_{DD} -0.2V	-	±10	-	mV
Stable time	@CINP=1.3 V CINN=1.2 V	-	-	2	us

9 PACKAGE DIMENSIONS

9.1 LQFP-48 (7x7x1.4mm^2 Footprint 2.0mm)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

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