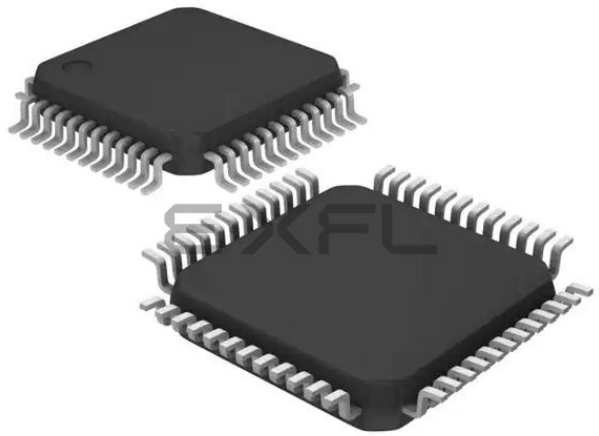

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	40
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/m058lbn

LIST OF FIGURES

1 GENERAL DESCRIPTION

The NuMicro M051™ series is a 32-bit microcontroller with embedded ARM® Cortex™-M0 core for industrial control and applications which need rich communication interfaces. The Cortex™-M0 is the newest ARM embedded processor with 32-bit performance and at a cost equivalent to traditional 8-bit microcontroller. The NuMicro M051™ series includes M052, M054, M058 and M0516 families.

The M058/M0516 can run up to 50 MHz. Thus it can afford to support a variety of industrial control and applications which need high CPU performance. The M058/M0516 has 32K/64K-byte embedded flash, 4K-byte data flash, 4K-byte flash for the ISP, and 4K-byte embedded SRAM.

Many system level peripheral functions, such as I/O Port, EBI (External Bus Interface), Timer, UART, SPI, I2C, PWM, ADC, Watchdog Timer and Brownout Detector, have been incorporated into the M058/M0516 in order to reduce component count, board space and system cost. These useful functions make the M058/M0516 powerful for a wide range of applications.

Additionally, the M058/M0516 is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product.

- Open-Drain output
- Input only with high impendence

- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports high driver and high sink IO mode

- Timer
  - Provides four channel 32-bit timers, one 8-bit pre-scale counter with 24-bit up-timer for each timer.
  - Independent clock source for each timer.
  - 24-bit timer value is readable through TDR (Timer Data Register)
  - Provides one-shot, periodic and toggle operation modes.
  - Provide event counter function.
  - Provide external capture/reset counter function equivalent to 8051 Timer2.
- Watchdog Timer
  - Multiple clock sources
  - Supports wake up from power down or sleep mode
  - Interrupt or reset selectable on watchdog time-out
- PWM
  - Built-in up to four 16-bit PWM generators; providing eight PWM outputs or four complementary paired PWM outputs
  - Individual clock source, clock divider, 8-bit pre-scalar and dead-zone generator for each PWM generator
  - PWM interrupt synchronized to PWM period
  - 16-bit digital Capture timers (shared with PWM timers) with rising/falling capture inputs
  - Supports capture interrupt
- UART

- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- Programmable clocks allow versatile rate control.
- Supports multiple address recognition (four slave address with mask option)

- ADC
  - 12-bit SAR ADC with 760k SPS
  - Up to 8-ch single-ended input or 4-ch differential input
  - Supports single mode/burst mode/single-cycle scan mode/continuous scan mode
  - Supports 2' complement/un-signed format in differential mode conversion result
  - Each channel with an individual result register
  - Supports conversion value monitoring (or comparison) for threshold voltage detection
  - Conversion can be started either by software trigger or external pin trigger
- Analog Comparator
  - Up to 2 comparator analog modules
  - External input or internal band gap voltage selectable at negative node
  - Interrupt when compare result change
  - Power down wake up
- EBI (External Bus Interface) for external memory-mapped device access
  - Accessible space: 64KB in 8-bit mode or 128KB in 16-bit mode
  - Supports 8-bit/16-bit data width
  - Supports byte-write in 16-bit data width
- In-System Programming (ISP) and In-Circuit Programming (ICP)
- One built-in temperature sensor with 1℃ resolution
- Brown-Out Detector
  - With 4 levels: 4.3V/3.7V/2.7V/2.2V

Pin number		Symbol	Alternate Function			Type[1]	Description
QFN33	LQFP48		1	2	3		
16	23	P2.4	PWM4[2]	AD12		D, I/O	The CPO1 pin is the output of Comparator1.
17	25	P2.5	PWM5[2]	AD13		D, I/O	
18	26	P2.6	PWM6[2]	AD14	CPO1	D, I/O	
NC	27	P2.7	PWM7[2]	AD15		D, I/O	
3	5	P3.0	RXD[2]		CPN1	I/O	**PORT3:** Port 3 is an 8-bit four mode output pin and two mode input. Its multifunction pins are for RXD, TXD, $\overline{INT0}$, $\overline{INT1}$, T0, T1, $\overline{WR}$, and $\overline{RD}$. The RXD/TXD pins are for UART0 function used. The SDA/SCK pins are for I^2C function used. MCLK: EBI clock output pin. CKO: HCLK clock output The STADC pin is for ADC external trigger input. The CPN1/CPP1 pins are for Comparator1 negative/positive inputs. The CPO0 pin is the output of Comparator0. The T0/T1 pins are for Timer0/1 external even counter input. The T0EX/T1EX pins are for external capture/reset trigger input of Timer0/1.
5	7	P3.1	TXD[2]		CPP1	I/O	
6	8	P3.2	$\overline{INT0}$	STADC	T0EX	I/O	
NC	9	P3.3	$\overline{INT1}$	MCLK	T1EX	I/O	
7	10	P3.4	T0	SDA		I/O	
8	11	P3.5	T1	SCL		I/O	
9	13	P3.6	$\overline{WR}$	CKO	CPO0	I/O	
NC	14	P3.7	$\overline{RD}$			I/O	
NC	24	P4.0	PWM0[2]		T2EX	I/O	**PORT4:** Port 4 is an 8-bit four mode output pin and two mode input. Its multifunction pins are for /CS, ALE, ICE_CLK and ICE_DAT. $\overline{CS}$ for EBI (External Bus Interface) used. ALE (Address Latch Enable) is used to enable the address latch that separates the address from the data on Port 0 and Port 2.
NC	36	P4.1	PWM1[2]		T3EX	I/O	
NC	48	P4.2	PWM2[2]			I/O	
NC	12	P4.3	PWM3[2]			I/O	

Pin number		Symbol	Alternate Function			Type[1]	Description
QFN33	LQFP48		1	2	3		
NC	28	P4.4	$\overline{CS}$			I/O	The ICE_CLK/ICE_DAT pins are for JTAG-ICE function used. PWM0-3 can be used from P4.0-P4.3 when EBI is active. The T2EX/T3EX pins are for external capture/reset trigger input of Timer2/3.
NC	29	P4.5	ALE			I/O	
19	30	P4.6	ICE_CLK			I/O	
20	31	P4.7	ICE_DAT			I/O	

Table 5-1 NuMicro™ M051 Series Pin Description

[1] I/O type description. I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pins, ST: Schmitt trigger.

[2] The pins features which are set by S/W. Only one-set pin can be used while S/W to set it.

6.2 System Manager

6.2.1 Overview

The following functions are included in system manager section

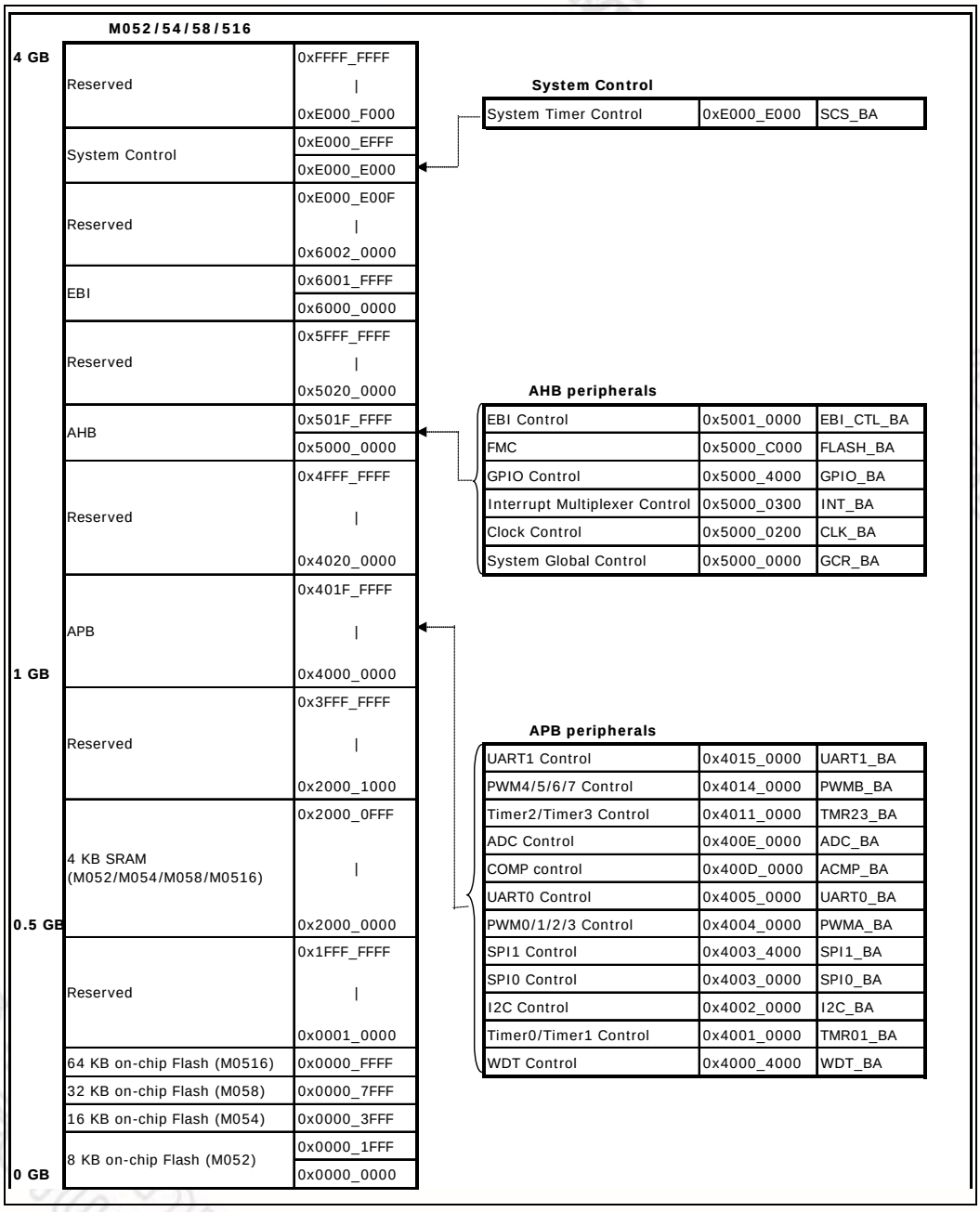
- System Resets
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip module reset , multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset includes one of the list below event occurs. For these reset event flags can be read by RSTSRC register.

- The Power-On Reset (POR)
- The low level on the /RESET pin
- Watchdog Time Out Reset (WDT)
- Low Voltage Reset (LVR)
- Brown-Out Detected Reset (BOD)
- CPU Reset
- Software one shot Reset

6.2.5 Whole System Memory Mapping Table



6.2.6 System Timer (SysTick)

The Cortex-M0 includes an integrated system timer, SysTick. SysTick provides a simple, 24-bit

clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock edge, then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the documents “ARM® Cortex™-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

6.2.7 Nested Vectored Interrupt Controller (NVIC)

Cortex-M0 provides an interrupt controller as an integral part of the exception mode, named as "Nested Vectored Interrupt Controller (NVIC)". It is closely coupled to the processor kernel and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Dynamic priority changing
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in "Handler Mode". This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one's priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When any interrupts is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers "PC, PSR, LR, R0~R3, R12" to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports "Tail Chaining" which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports "Late Arrival" which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the documents "ARM® Cortex™-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

6.3 Clock Controller

6.3.1 Overview

The clock controller generates the clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip will not enter power-down mode until CPU sets the power down enable bit (PWR_DOWN_EN) and Cortex-M0 core executes the WFI instruction. After that, chip enter power-down mode and wait for wake-up interrupt source triggered to leave power-down mode. In the power down mode, the clock controller turns off the external crystal and internal 22.1184 MHz oscillator to reduce the overall system power consumption.

6.3.2 Clock Generator Block Diagram

The clock generator consists of 4 sources which list below:

- One external 4~24 MHz crystal
- One internal 22.1184 MHz RC oscillator
- One programmable PLL FOUT(PLL source consists of external 4~24 MHz crystal and internal 22.1184M)
- One internal 10 kHz oscillator

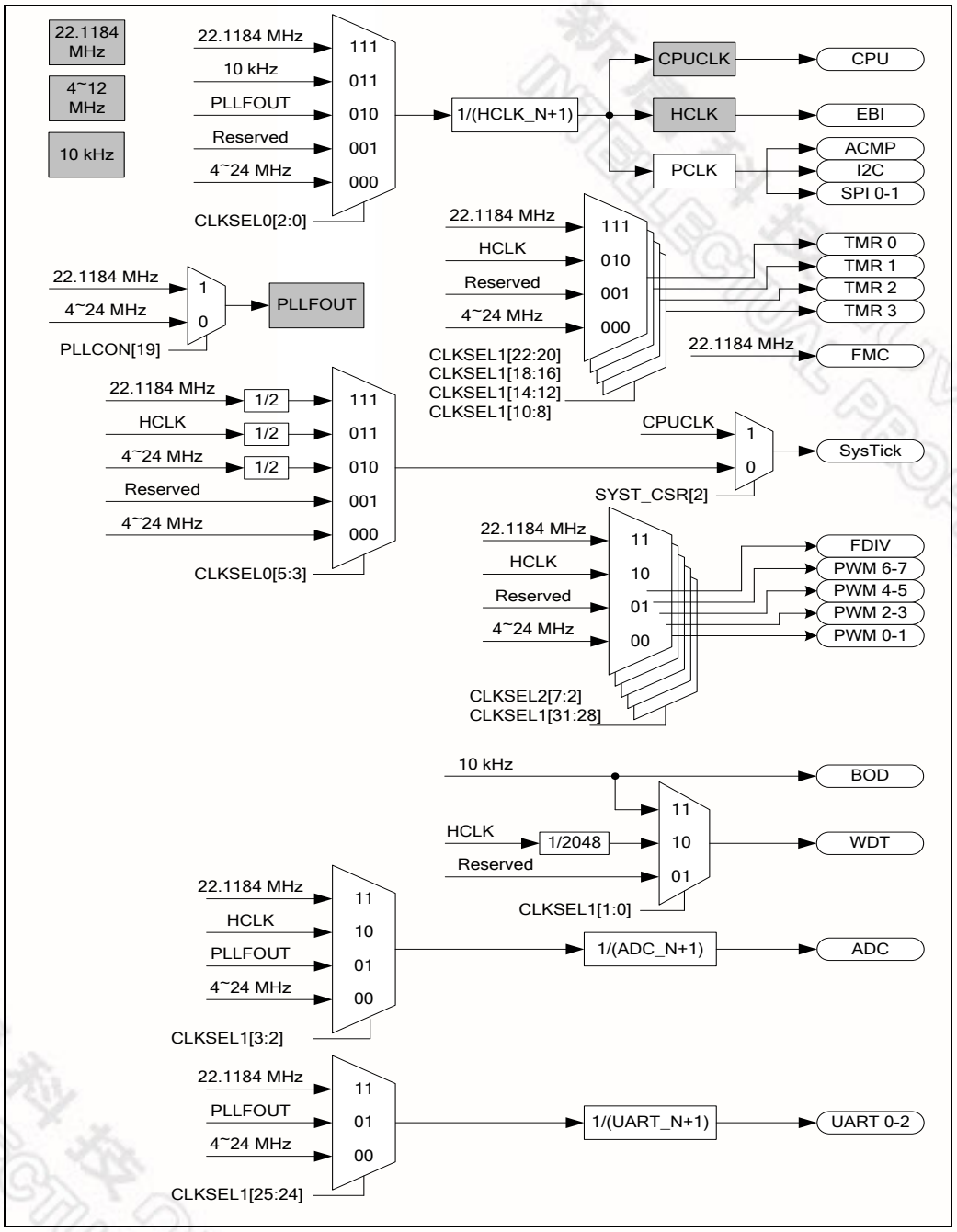


Figure 6-3 Clock generator block diagram

6.3.5 Peripherals Clock Source Select

The peripherals clock had different clock source switch setting which depends on the different peripheral..

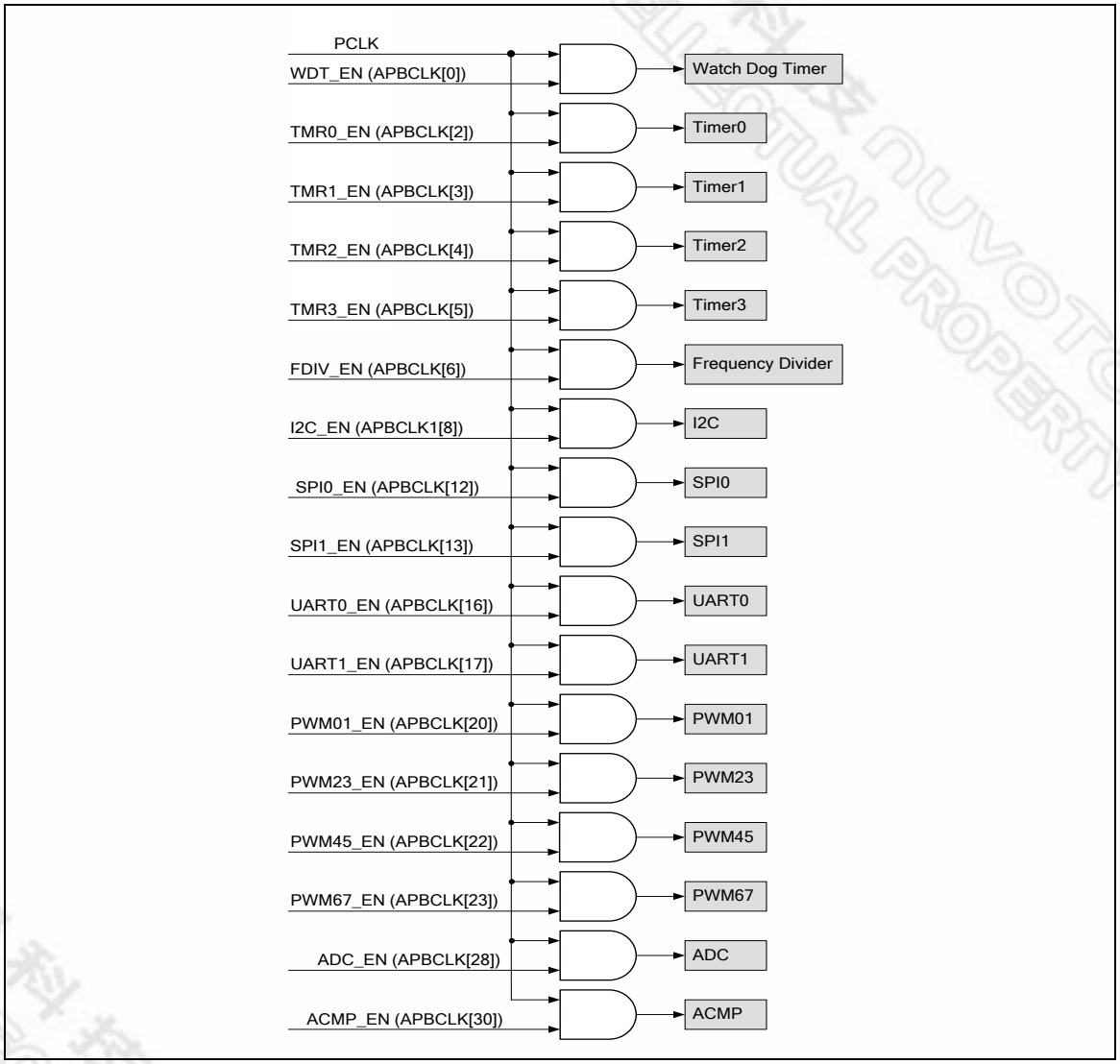


Figure 6-7 Peripherals Clock Source Select for PCLK

6.8 Timer Controller

6.8.1 Overview

NuMicro M051™ series timer controller includes four 32-bit timers, which allows user to easily implement a timer control for applications. The timer can perform functions like frequency measurement, event counting, interval measurement, clock generation, delay timing, and so on. The timer can generates an interrupt signal upon timeout, or provide the current counting value during operation.

6.8.2 Features:

- 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle and continuous counting operation modes
- Time out period = (Period of timer clock input) * (8-bit pre-scale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = (1 / T MHz) * (2^8) * (2^{24}), T is the period of timer clock
- 24-bit timer value is readable through TDR (Timer Data Register)
- Support event counting function to count the event from external pin
- Support input capture function to capture or reset counter value

110	$2^{16} * T_{WDT}$	$1024 * T_{WDT}$	6.5536 s ~ 6.656 s
111	$2^{18} * T_{WDT}$	$1024 * T_{WDT}$	26.2144 s ~ 26.3168 s

Table 6-2 Watchdog Timeout Interval Selection

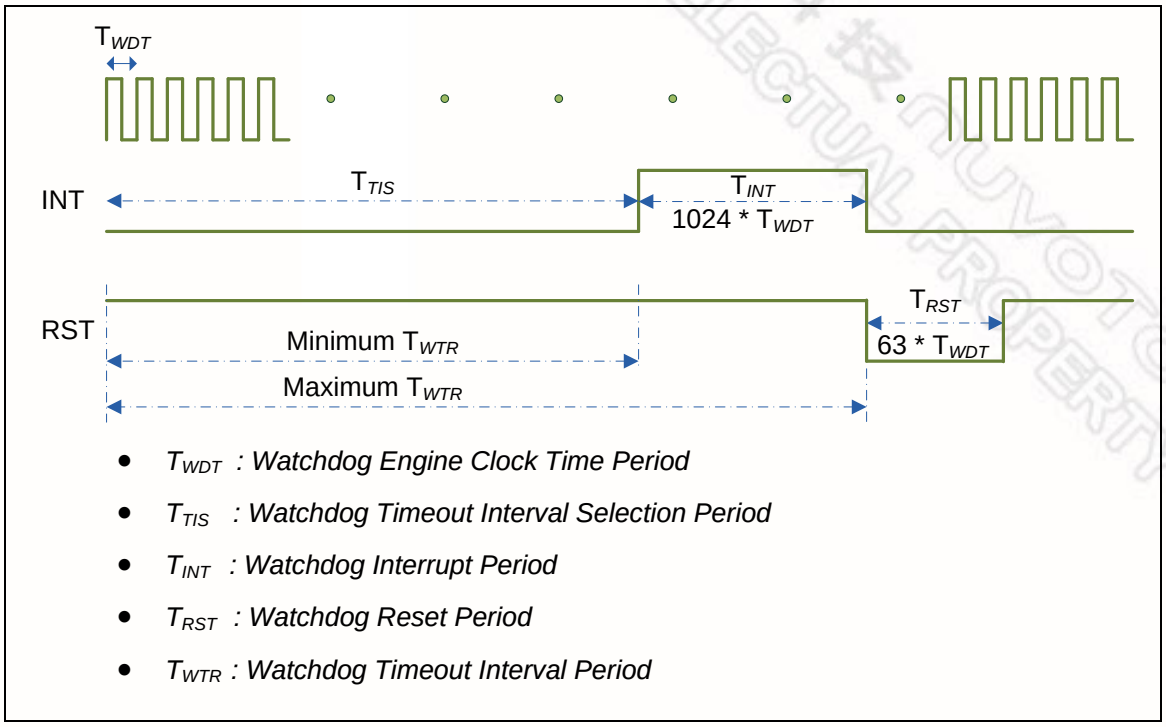


Figure 6-14 Timing of Interrupt and Reset Signal

6.9.2 Features

- 18-bit free running counter to avoid chip from Watchdog timer reset before the delay time expires.
- Selectable time-out interval (2^4 ~ 2^{18}) and the time out interval is 104 ms ~ 26.3168 s (if WDT_CLK = 10 kHz).
- Reset period = (1 / 10 kHz) * 63, if WDT_CLK = 10 kHz.

6.10 UART Interface Controller (UART)

NuMicro M051™ series provides two channels of Universal Asynchronous Receiver/Transmitters (UART). UART0~1 performs Normal Speed UART, and support flow control function.

6.10.1 Overview

The Universal Asynchronous Receiver/Transmitter (UART) performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR Function, LIN master/slave mode function and RS-485 mode functions. Each UART channel supports seven types of interrupts including transmitter FIFO empty interrupt (INT_THRE), receiver threshold level reaching interrupt (INT_RDA), line status interrupt (parity error or framing error or break interrupt) (INT_RLS), receiver buffer time out interrupt (INT_TOUT), MODEM/Wakeup status interrupt (INT_MODEM), Buffer error interrupt (INT_BUF_ERR) and LIN receiver break field detected interrupt (INT_LIN_RX_BREAK).

The UART0 and UART1 are built-in with a 16-byte transmitter FIFO (TX_FIFO) and a 16-byte receiver FIFO (RX_FIFO) that reduces the number of interrupts presented to the CPU. The CPU can read the status of the UART at any time during the operation. The reported status information includes the type and condition of the transfer operations being performed by the UART, as well as 3 error conditions (parity error, framing error, break interrupt) probably occur while receiving data. The UART includes a programmable baud rate generator that is capable of dividing clock input by divisors to produce the serial clock that transmitter and receiver need. The baud rate equation is Baud Rate = UART_CLK / M * [BRD + 2], where M and BRD are defined in Baud Rate Divider Register (UA_BAUD). Table 6-3 lists the equations in the various conditions and Table 6-4 list the UART baud rate setting table.

Mode	DIV_X_EN	DIV_X_ONE	Divider X	BRD	M	Baud rate equation
0	0	0	B	A	16	UART_CLK / [16 * (A+2)]
1	1	0	B	A	B+1	UART_CLK / [(B+1) * (A+2)] , B must >= 8
2	1	1	Don't care	A	1	UART_CLK / (A+2), A must >=3

Table 6-3 UART Baud Rate Equation

The alternate function of UART controllers is LIN (Local Interconnect Network) function. The LIN mode is selected by setting UA_FUN_SEL [1:0] = '01'. In LIN mode, one start bit and 8-bit data format with 1-bit stop bit are required in accordance with the LIN standard.

Another alternate function of UART controllers is RS-485 9 bit mode function, and direction control provided by RTS pin or can program GPIO (P0.3 for RTS0 and P0.1 for RTS1) to implement the function by software. The RS-485 mode is selected by setting the UA_FUN_SEL register to select RS-485 function. The RS-485 driver control is implemented by using the RTS control signal from an asynchronous serial port to enable the RS-485 driver. In RS-485 mode, many characteristics of the RX and TX are same as UART.

6.10.2 Features

- Full duplex, asynchronous communications
- Separate receive / transmit 16/16 bytes entry FIFO for data payloads
- Support hardware auto flow control/flow control function (CTS, RTS) and programmable RTS flow control trigger level
- Programmable receiver buffer trigger level
- Support programmable baud-rate generator for each channel individually
- Support CTS wake up function
- Support 8 bit receiver buffer time out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting UA_TOR [DLY] register
- Support break error, frame error, parity error and receive / transmit buffer overflow detect function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5, 6, 7, 8 bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Support IrDA SIR function mode
  - Support for 3/16 bit duration for normal mode
- Support LIN function mode
  - Support LIN master/slave mode
  - Support programmable break generation function for transmitter
  - Support break detect function for receiver
- Support RS-485 function mode.
  - Support RS-485 9bit mode
  - Support hardware or software enable to program RTS pin to control RS-485 transmission direction directly

10 REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
V1.0	Oct 20, 2011	-	Initial issued
V1.01	Mar. 19, 2012	8.3.4	Updated the Center Frequency of 22Mhz RC spec