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Understanding <u>Embedded - DSP (Digital</u> <u>Signal Processors)</u>

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of <u>Embedded - DSP (Digital</u> <u>Signal Processors)</u>

Details

Product Status	Obsolete
Туре	SC3850 Dual Core
Interface	Ethernet, I ² C, PCI, RGMII, Serial RapidIO, SGMII, SPI, UART/USART
Clock Rate	1GHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	576kB
Voltage - I/O	2.50V
Voltage - Core	1.00V
Operating Temperature	0°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8152svt1000b

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



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Figure 1. MSC8152 Block Diagram



Figure 2. StarCore SC3850 DSP Subsystem Block Diagram



1.2 Signal List By Ball Location

Table 1 presents the signal list sorted by ball number. When designing a board, make sure that the power rail for each signal is appropriately considered. The specified power rail must be tied to the voltage level specified in this document if any of the related signal functions are used (active)

Note: The information in Table 1 and Table 2 distinguishes among three concepts. First, the power pins are the balls of the device package used to supply specific power levels for different device subsystems (as opposed to signals). Second, the power rails are the electrical lines on the board that transfer power from the voltage regulators to the device. They are indicated here as the reference power rails for signal lines; therefore, the actual power inputs are listed as N/A with regard to the power rails. Third, symbols used in these tables are the names for the voltage levels (absolute, recommended, and so on) and not the power supplies themselves.

Ball Number	Signal Name ^{1,2}	Pin Type ¹⁰	Power Rail Name
A2	M2DQS3	I/O	GVDD2
A3	M2DQS3	I/O	GVDD2
A4	M2ECC0	I/O	GVDD2
A5	M2DQS8	I/O	GVDD2
A6	M2DQS8	I/O	GVDD2
A7	M2A5	0	GVDD2
A8	M2CK1	0	GVDD2
A9	M2CK1	0	GVDD2
A10	M2CS0	0	GVDD2
A11	M2BA0	0	GVDD2
A12	M2CAS	0	GVDD2
A13	M2DQ34	I/O	GVDD2
A14	M2DQS4	I/O	GVDD2
A15	M2DQS4	I/O	GVDD2
A16	M2DQ50	I/O	GVDD2
A17	M2DQS6	I/O	GVDD2
A18	M2DQS6	I/O	GVDD2
A19	M2DQ48	I/O	GVDD2
A20	M2DQ49	I/O	GVDD2
A21	VSS	Ground	N/A
A22	Reserved	NC	—
A23	SXPVDD1	Power	N/A
A24	SXPVSS1	Ground	N/A
A25	Reserved	NC	—
A26	Reserved	NC	—
A27	SXCVDD1	Power	N/A
A28	SXCVSS1	Ground	N/A
B1	M2DQ24	I/O	GVDD2
B2	GVDD2	Power	N/A
B3	M2DQ25	I/O	GVDD2
B4	VSS	Ground	N/A
B5	GVDD2	Power	N/A
B6	M2ECC1	I/O	GVDD2
B7	VSS	Ground	N/A
B8	GVDD2	Power	N/A

Table 1. Signal List by Ball Number



Ball Number	Signal Name ^{1,2}	Pin Type ¹⁰	Power Rail Name
Y11	GVDD1	Power	N/A
Y12	VSS	Ground	N/A
Y13	GVDD1	Power	N/A
Y14	VSS	Ground	N/A
Y15	GVDD1	Power	N/A
Y16	VSS	Ground	N/A
Y17	GVDD1	Power	N/A
Y18	VSS	Ground	N/A
Y19	GVDD1	Power	N/A
Y20	VSS	Ground	N/A
Y21	NVDD	Power	N/A
Y22	GPIO20/SPI_SL ^{5,8}	I/O	NVDD
Y23	GPIO17/SPI_SCK ^{5,8}	I/O	NVDD
Y24	GPIO14/DRQ0/IRQ14/RC14 ^{5,8}	I/O	NVDD
Y25	GPI012/IRQ12/RC12 ^{5,8}	I/O	NVDD
Y26	GPIO8/IRQ8/RC8 ^{5,8}	I/O	NVDD
Y27	NVDD	Power	N/A
Y28	VSS	Ground	N/A
AA1	GVDD1	Power	N/A
AA2	VSS	Ground	N/A
AA3	M1DQ18	I/O	GVDD1
AA4	GVDD1	Power	N/A
AA5	VSS	Ground	N/A
AA6	M1DQ20	I/O	GVDD1
AA7	GVDD1	Power	N/A
AA8	VSS	Ground	N/A
AA9	M1A15	0	GVDD1
AA10	M1CK2	0	GVDD1
AA11	M1MDIC0	I/O	GVDD1
AA12	M1VREF	I	GVDD1
AA13	M1MDIC1	I/O	GVDD1
AA14	M1DQ46	I/O	GVDD1
AA15	M1DQ47	I/O	GVDD1
AA16	M1DQ45	I/O	GVDD1
AA17	M1DQ41	I/O	GVDD1
AA18	M1DQ62	I/O	GVDD1
AA19	M1DQ63	I/O	GVDD1
AA20	M1DQ61	I/O	GVDD1
AA21	VSS	Ground	N/A
AA22	GPIO21 ^{5,8}	I/O	NVDD
AA23	GPIO18/SPI_MOSI ^{5,8}	I/O	NVDD
AA24	GPIO16/RC16 ^{5,8}	I/O	NVDD
AA25	GPIO4/DDN1/IRQ4/RC4 ^{5,8}	I/O	NVDD
AA26	GPIO9/IRQ9/RC9 ^{5,8}	I/O	NVDD
AA27	GPIO6/IRQ6/RC6 ^{5,8}	I/O	NVDD
AA28	GPIO1/IRQ1/RC1 ^{5,8}	I/O	NVDD

Table 1. Signal List by Ball Number (continued)



AB1 M1DQS2 I/O GVDD1 AB2 M1DQS2 I/O GVDD1 AB3 M1DQ19 I/O GVDD1 AB4 M1DM2 0 GVDD1 AB5 M1DQ21 I/O GVDD1 AB5 M1DQ22 I/O GVDD1 AB7 M1CKE0 0 GVDD1 AB8 M1A1 0 GVDD1 AB8 M1A1 0 GVDD1 AB8 M1A7 0 GVDD1 AB9 M1A7 0 GVDD1 AB10 M1CK2 0 GVDD1 AB11 M1APAR_OUT 0 GVDD1 AB12 M1DD11 0 GVDD1 AB13 M1APAR_IN 1 GVDD1 AB14 M1DQ43 I/O GVDD1 AB16 M1DQ40 I/O GVDD1 AB17 M1DQ40 I/O GVDD1 AB18 M1DQ69 I/O N/D	Ball Number	Signal Name ^{1,2}	Pin Type ¹⁰	Power Rail Name
AB2 MIDOS2 I/O GVDD1 AB3 MIDO19 I/O GVDD1 AB4 MIDQ12 I/O GVDD1 AB5 MIDQ21 I/O GVDD1 AB5 MIDQ21 I/O GVDD1 AB6 MIDQ2 I/O GVDD1 AB7 MICKE0 O GVDD1 AB8 MIA11 O GVDD1 AB9 MIA7 O GVDD1 AB1 MIAPAR_OUT O GVDD1 AB12 MIDD11 O GVDD1 AB13 MIAPAR_IN I GVDD1 AB14 MIDQ4 I/O GVD1 AB15 MIDM5 O GVD1 AB16 MIDA4 I/O GVD1 AB17 MIDQ40 I/O GVD1 AB19 MIDM6 I/O GVD1 AB20 MIDQ60 I/O N/A AB22 GPIO3/I/IXC_SDA ^{5/8} I/O N/A	AB1	M1DQS2	I/O	GVDD1
AB3 M1D019 UO GVD11 AB4 M1D021 UO GVD11 AB5 M1D021 UO GVD11 AB6 M1D022 UO GVD11 AB7 M1022 UO GVD11 AB7 M1CK0 O GVD11 AB8 M1A1 O GVD11 AB8 M1A7 O GVD11 AB9 M1A7 O GVD11 AB1 M1APAR_OUT O GVD11 AB13 M1APAR_IN 1 GVD11 AB14 M1D043 UO GVD11 AB15 M1D043 UO GVD11 AB16 M1D240 UO GVD11 AB18 M1D260 UO GVD11 AB18 M1D240 UO GVD11 AB14 M1D240 UO GVD11 AB12 VS Groand NA AB21 VS Groand NA	AB2	M1DQS2	I/O	GVDD1
AB4 M1M2 O GVD1 AB5 M1DQ21 I/O GVD01 AB6 M1DQ22 I/O GVD01 AB7 M1CKE0 O GVD01 AB8 M1A1 O GVD01 AB8 M1A1 O GVD01 AB9 M1A7 O GVD01 AB10 M1CK2 O GVD01 AB11 M1APAR_OUT O GVD01 AB13 M1APAR_DUT O GVD01 AB13 M1APAR_DUT I GVD01 AB13 M1DAS O GVD01 AB14 M10043 I/O GVD01 AB16 M1D044 I/O GVD01 AB17 M1D040 I/O GVD01 AB18 M1DQ59 I/O GVD01 AB22 GPI03/12C_SDA ^{5,8} I/O NVD AB23 GPI03/17C_SDA ^{5,8} I/O NVDD AB24 GPI03/17C_SDA ^{5,8} I/O	AB3	M1DQ19	I/O	GVDD1
AB5 M1021 I/O GVD11 AB6 M1022 I/O GVD11 AB7 M1CKE0 O GVD11 AB8 M1A1 O GVD11 AB9 M1A7 O GVD11 AB10 M1CK2 O GVD11 AB11 M1APAR_OUT O GVD11 AB12 M10D11 O GVD11 AB13 M1APAR_IN I GVD11 AB14 M1D43 I/O GVD11 AB15 M1DA4 I/O GVD11 AB16 M1D44 I/O GVD11 AB17 M1D40 I/O GVD11 AB18 M1D269 I/O GVD11 AB19 M1D07 O GVD11 AB20 M1D269 I/O GVD11 AB21 VSS Ground N/A AB22 GPI027/TM4/RCW_SRC2 ^{5,8} I/O NVDD AB23 GPI02/FM2/RCW_SRC2 ^{5,8} I/O	AB4	M1DM2	0	GVDD1
AB6 M1022 I/O GYDD1 AB7 M1CKE0 O GYDD1 AB8 M1A1 O GYDD1 AB8 M1A7 O GYDD1 AB9 M1A7 O GYDD1 AB10 M1CK2 O GYDD1 AB11 M1APAR_OUT O GYDD1 AB12 M1OD11 O GYDD1 AB13 M1APAR_OUT O GYDD1 AB14 M1OA3 I GYDD1 AB15 M1DM5 O GYDD1 AB16 M1DQ40 I/O GYDD1 AB17 M1DQ40 I/O GYDD1 AB19 M1DG60 I/O GYDD1 AB20 M1DG60 I/O GYDD1 AB21 VSS Ground N/A AB22 GPI031/32C_SDA ^{5,8} I/O NYDD AB23 GPI02/TMR4/RCW_SRC1 ^{5,8} I/O NYDD AB24 GPI00/mRC0/msc5. ^{5,8}	AB5	M1DQ21	I/O	GVDD1
A87 MrKE0 O GVD1 A88 M1A11 O GVD1 A89 M1A7 O GVD1 AB10 MTCK2 O GVD1 AB10 MTCK2 O GVD1 AB11 M1APAR_OUT O GVD1 AB12 M1ODT1 O GVD1 AB13 MTAPAR_IN I GVD1 AB14 M1DQ43 I/O GVD1 AB15 M1DM5 O GVD1 AB16 M1DQ44 I/O GVD1 AB16 M1DQ44 I/O GVD1 AB17 M1DQ69 I/O GVD1 AB20 M1DG69 I/O GVD1 AB21 VSS I/O NVDD AB22 GPI03/I2C_SDA ^{5,8} I/O NVDD AB23 GPI02/TMR4/RCW_SRC5 ^{5,8} I/O NVDD AB26 GPI00/IRG16/C16 ^{5,6} I/O NVDD AB26 GPI00/IRG16/C16 ^{5,6} <td< td=""><td>AB6</td><td>M1DQ22</td><td>I/O</td><td>GVDD1</td></td<>	AB6	M1DQ22	I/O	GVDD1
AB8 M1A1 O GVDD1 AB9 M1A7 O GVDD1 AB10 M1GK2 O GVDD1 AB11 M1APAR_OUT O GVDD1 AB12 M1ODT1 O GVDD1 AB13 M1APAR_IN I GVDD1 AB14 M1DQ43 I/O GVDD1 AB15 M1DM5 O GVDD1 AB16 M1DQ40 I/O GVDD1 AB17 M1DQ40 I/O GVDD1 AB18 M1DG9 I/O GVDD1 AB19 M1DM7 O GVDD1 AB20 M1DG60 I/O GVDD1 AB21 VSS Ground NA AB22 GPIO31/2C_SDA ^{6,8} I/O NVDD AB23 GPIO27/MR4/RCW_SRC5 ^{6,8} I/O NVDD AB24 GPIO247/MR1/RCW_SRC5 ^{6,8} I/O NVDD AB25 GPIO247/MR1/RCW_SRC5 ^{6,8} I/O NVDD AB26 <	AB7	M1CKE0	0	GVDD1
AB9 M1A7 O GVDD1 AB10 MTCRZ O GVDD1 AB11 MTAPAR_OUT O GVDD1 AB12 M10DT1 O GVDD1 AB13 MTAPAR_N I GVDD1 AB13 MTAPAR_N I GVDD1 AB13 MTAPAR_N I GVDD1 AB14 MIDQ3 I/O GVDD1 AB15 MTDM5 O GVDD1 AB16 MTDQ40 I/O GVDD1 AB17 MTDQ40 I/O GVDD1 AB18 MTDQ59 I/O GVDD1 AB20 MTDQ60 I/O GVDD1 AB21 VSS Ground N/A AB22 GPI02/TMR4/RCW_SRC0 ^{5,8} I/O NVDD AB23 GPI02/TMR4/RCW_SRC0 ^{5,8} I/O NVDD AB24 GPI02/TMR4/RCW_SRC2 ^{5,8} I/O NVDD AB25 GPI00/RQ7/G/RC10 ^{5,8} I/O NVDD AB26	AB8	M1A11	0	GVDD1
AB10 MTCK2 O GVDD1 AB11 M1APAR_OUT O GVDD1 AB12 M10D11 O GVDD1 AB13 MTAPAR_IN I GVDD1 AB14 M1DC43 IO GVDD1 AB15 M1DM5 O GVDD1 AB16 M1DC43 IO GVDD1 AB16 M1DC44 IO GVDD1 AB18 M1DC44 IO GVDD1 AB18 M1DC44 IO GVDD1 AB18 M1DC40 IO GVDD1 AB18 M1DC40 O GVDD1 AB20 M1DR60 IO GVDD1 AB21 VSS Ground N/A AB22 GPI03/I/C_SDA ^{5,8} IO NVDD AB23 GPI02/TMR4/RCW_SRC5 ^{5,8} IO NVDD AB24 GPI02/TMR1/RCW_SRC5 ^{5,8} IO NVDD AB25 GPI03/RG5/RC5 ^{6,8} IO NVDD AC1 VSS<	AB9	M1A7	0	GVDD1
AB11 M1APAR_OUT O GVDD1 AB12 M1ODT1 O GVDD1 AB13 M1APAR_IN I GVDD1 AB14 M1DQ43 I/O GVDD1 AB15 M1DM5 O GVDD1 AB16 M1DQ43 I/O GVDD1 AB16 M1DQ40 I/O GVDD1 AB17 M1DQ40 I/O GVDD1 AB18 M1DQ59 I/O GVDD1 AB19 M1DQ60 I/O GVD1 AB20 M1DQ60 I/O GVD1 AB21 VSS Ground N/A AB22 GPI031/12C_SDA ^{5,8} I/O NVDD AB23 GPI027/TMR4/RCW_SRC5 ^{5,8} I/O NVDD AB24 GPI027/TMR4/RCW_SRC5 ^{5,8} I/O NVDD AB25 GPI010/IRG0/RC10 ^{5,8} I/O NVDD AB26 GPI010/IRG0/RC10 ^{5,8} I/O NVDD AB27 GPI05/IRG5/RC5 ^{5,8} I/O NVDD	AB10	M1CK2	0	GVDD1
AB12 M10DT1 O GVD1 AB13 M1APAR_IN I GVD1 AB14 M1D043 I/O GVD1 AB15 M1DM5 O GVD1 AB16 M1D044 I/O GVD1 AB17 M1D040 I/O GVD1 AB18 M1D040 I/O GVD1 AB18 M1D040 O GVD1 AB18 M1D040 O GVD1 AB19 M1DM7 O GVD1 AB20 M1D060 I/O GVD1 AB21 VSS GPI031/I2C_SDA ^{5,8} I/O NVD AB22 GPI027/TMR4/RCW_SRC9 ^{5,8} I/O NVDD AB23 GPI02/TMR4/RCW_SRC9 ^{5,8} I/O NVDD AB24 GPI02/TMR4/RCW_SRC9 ^{5,8} I/O NVDD AB25 GPI02/TMR4/RCW_SRC9 ^{5,8} I/O NVDD AB26 GPI001/RO0/RC10 ^{5,8} I/O NVDD AB27 GPI06/RO0/RC0 ^{5,8} I/O <td< td=""><td>AB11</td><td>M1APAR_OUT</td><td>0</td><td>GVDD1</td></td<>	AB11	M1APAR_OUT	0	GVDD1
AB13 M1APAR_IN I GVDD1 AB14 M1DQ43 I/O GVDD1 AB15 M1DM6 O GVDD1 AB16 M1DQ44 I/O GVDD1 AB17 M1DQ40 I/O GVDD1 AB18 M1DQ40 I/O GVDD1 AB19 M1DA7 O GVDD1 AB20 M1DQ60 I/O GVDD1 AB21 VSS Ground N/A AB22 GPIO31/I2C_SDA ^{5,8} I/O NVDD AB23 GPIO27/TMR4/RCW_SRC0 ^{5,8} I/O NVDD AB24 GPIO27/TMR4/RCW_SRC2 ^{5,8} I/O NVDD AB25 GPIO24/TMR1/RCW_SRC2 ^{5,8} I/O NVDD AB26 GPIO1/RQ7/O/RC10 ^{5,8} I/O NVDD AB27 GPIO3/RQ7/O/RC10 ^{5,8} I/O NVDD AB28 GPIO1/RQ7/O/RC10 ^{5,8} I/O NVDD AB29 GPIO1/RQ7/O/RC10 ^{5,8} I/O NVDD AC1 VSS Ground	AB12	M1ODT1	0	GVDD1
AB14 M1DQ43 I/O GVDD1 AB15 M1DM5 O GVDD1 AB16 M1DQ44 I/O GVDD1 AB17 M1DQ40 I/O GVDD1 AB18 M1DQ59 I/O GVDD1 AB19 M1DM7 O GVDD1 AB20 M1DQ60 I/O GVDD1 AB21 VSS Ground N/A AB22 GPIO31/I2C_SDA ^{5,8} I/O NVDD AB23 GPIO27/TMR4/RCW_SRC9 ^{5,8} I/O NVDD AB24 GPIO27/TMR4/RCW_SRC5 ^{5,8} I/O NVDD AB25 GPIO27/TMR4/RCW_SRC5 ^{5,8} I/O NVDD AB26 GPIO0/IRQ10/RC10 ^{6,8} I/O NVDD AB27 GPIO5/IRQ5/RC5 ^{5,8} I/O NVDD AB28 GPIO0/IRQ10/RC10 ^{6,8} I/O NVDD AC1 VSS Ground N/A AC2 GVD1 Power N/A AC3 M1DQ16 I/O GVD1	AB13	M1APAR_IN	I	GVDD1
AB15 M1DM5 O GVD1 AB16 M1D044 I/O GVD1 AB17 M1D040 I/O GVD1 AB17 M1D059 I/O GVD1 AB18 M1D059 I/O GVD1 AB19 M1DM7 O GVD1 AB20 M1D060 I/O GVD1 AB21 VSS Ground N/A AB22 GPI021/I2C_SDA ^{5,8} I/O NVDD AB23 GPI027/TIMR4/RCW_SRC0 ^{5,8} I/O NVDD AB24 GPI025/TIME2/RCW_SRC1 ^{5,8} I/O NVDD AB25 GPI024/TIMR1/RCW_SRC2 ^{5,8} I/O NVDD AB26 GPI00/IRQ10/RC10 ^{6,3} I/O NVDD AB27 GPI05/IRQ5/RC5 ^{5,8} I/O NVDD AC1 VSS Ground N/A AC2 GVD1 Power N/A AC2 GVD1 Power N/A AC3 M1D016 I/O GVD1	AB14	M1DQ43	I/O	GVDD1
AB16 M1DQ44 I/O GVD1 AB17 M1DQ40 I/O GVD1 AB18 M1DQ59 I/O GVD1 AB18 M1DQ59 I/O GVD1 AB19 M1DQ60 I/O GVD1 AB20 M1DQ60 I/O GVD1 AB21 VSS Ground N/A AB22 GPI031/I2C_SDA ^{5,8} I/O NVDD AB23 GPI027/TMR4/RCW_SRC0 ^{5,8} I/O NVDD AB24 GPI027/TMR4/RCW_SRC2 ^{5,8} I/O NVDD AB25 GPI02/TMR1/RCW_SRC2 ^{5,8} I/O NVDD AB26 GPI01/IRQ10/RC10 ^{5,8} I/O NVDD AB27 GPI06/IRQ5/RC5/R ^{5,8} I/O NVDD AB26 GPI00/IRQ10/RC0 ^{5,8} I/O NVDD AC2 GVD1 Power N/A AC3 M1DQ16 I/O GVD1 AC4 VSS Ground N/A AC5 GVD1 Power N/A <	AB15	M1DM5	0	GVDD1
AB17 M1DQ40 I/O GVD1 AB18 M1DQ59 I/O GVD1 AB19 M1DM7 O GVD1 AB19 M1DM7 O GVD1 AB20 M1DQ60 I/O GVD1 AB21 VSS Ground N/A AB22 GPI031/I2C_SDA ^{5,8} I/O NVDD AB23 GPI027/TMR4/RCW_SRC5 ^{5,8} I/O NVDD AB24 GPI024/TMR1/RCW_SRC2 ^{5,8} I/O NVDD AB25 GPI024/TMR1/RCW_SRC2 ^{5,8} I/O NVDD AB26 GPI010/IRQ10/RC10 ^{5,8} I/O NVDD AB27 GPI06/IRQ5/RC5 ^{5,8} I/O NVDD AB28 GPI00/IRQ1/RC10 ^{5,8} I/O NVDD AC1 VS Ground N/A AC2 GVD1 Power N/A AC3 M1DQ16 I/O GVD1 AC4 VSS Ground N/A AC5 GVD1 Power N/A	AB16	M1DQ44	I/O	GVDD1
AB18 M1DQ59 I/O GVDD1 AB19 M1DM7 O GVDD1 AB20 M1DQ60 I/O GVDD1 AB20 M1DQ60 I/O GVDD1 AB21 VSS Ground N/A AB22 GPI031/12C_SDA ^{5,8} I/O NVDD AB23 GPI027/TIMR4/RCW_SRC0 ^{5,8} I/O NVDD AB24 GPI025/TMR2/RCW_SRC1 ^{5,8} I/O NVDD AB25 GPI024/TIMR1/RCW_SRC2 ^{5,8} I/O NVDD AB26 GPI010/IRQ0/RC16 ^{5,8} I/O NVDD AB27 GPI05/IRQ6/RC6 ^{5,8} I/O NVDD AB28 GPI00/IRQ0/RC0 ^{5,8} I/O NVDD AC1 VSS Ground N/A AC2 GVDD1 Power N/A AC3 M1DQ16 I/O GVD1 AC4 VSS Ground N/A AC6 M1DQ17 I/O GVD1 AC6 M1DQ17 O GVD1 <td>AB17</td> <td>M1DQ40</td> <td>I/O</td> <td>GVDD1</td>	AB17	M1DQ40	I/O	GVDD1
AB19 M1DM7 O GVDD1 AB20 M1DQ60 I/O GVDD1 AB21 VSS Ground N/A AB22 GPI031/2C_SDA ^{5,8} I/O NVDD AB23 GPI027/TMR4/RCW_SRC0 ^{5,8} I/O NVDD AB24 GPI027/TMR2/RCW_SRC1 ^{5,8} I/O NVDD AB25 GPI024/TMR1/RCW_SRC2 ^{5,8} I/O NVDD AB26 GPI010/IRQ10/RC10 ^{5,8} I/O NVDD AB27 GPI05/IRG6/RC5 ^{5,8} I/O NVDD AB28 GPI00/IRQ0/RC0 ^{5,8} I/O NVDD AB28 GPI00/IRQ0/RC0 ^{5,8} I/O NVDD AC1 VSS Ground N/A AC2 GVD1 Power N/A AC3 M1DQ16 I/O GVD1 AC4 VSS Ground N/A AC6 M1DQ16 I/O GVD1 AC6 M1DQ17 I/O GVD1 AC7 VSS Ground N/A	AB18	M1DQ59	I/O	GVDD1
AB20 M1DQ60 I/O GVDD1 AB21 VSS Ground N/A AB22 GPI031/I2C_SDA ^{5.8} I/O NVDD AB23 GPI027/TMR4/RCW_SRC0 ^{5.8} I/O NVDD AB24 GPI025/TMR2/RCW_SRC1 ^{5.8} I/O NVDD AB25 GPI024/TMR1/RCW_SRC2 ^{5.8} I/O NVDD AB26 GPI010/IRQ10/RC10 ^{5.8} I/O NVDD AB27 GPI05//RQ5/RC5 ^{5.8} I/O NVDD AB28 GPI00/IRQ0/RC0 ^{5.8} I/O NVDD AC1 VSS Ground N/A AC2 GVD1 Power N/A AC2 GVD1 Power N/A AC3 M1DQ16 I/O GVD1 AC4 VSS Ground N/A AC5 GVD1 Power N/A AC6 M1DQ17 I/O GVD1 AC7 VSS Ground N/A AC6 GVD1 Power N/A	AB19	M1DM7	0	GVDD1
AB21 VSS Ground N/A AB22 GPI031/J2C_SDA ^{5,8} I/O NVDD AB23 GPI027/TMR4/RCW_SRC0 ^{5,8} I/O NVDD AB24 GPI028/TMR2/RCW_SRC1 ^{5,8} I/O NVDD AB25 GPI024/TMR1/RCW_SRC2 ^{5,8} I/O NVDD AB26 GPI010/IRO10/RC10 ^{5,8} I/O NVDD AB27 GPI05/IRO5/RC5 ^{5,8} I/O NVDD AB28 GPI00/IRO0/RC0 ^{5,8} I/O NVDD AC1 VSS Ground N/A AC2 GVDD1 Power N/A AC3 M1DQ16 I/O GVDD1 AC4 VSS Ground N/A AC5 GVD1 Power N/A AC5 GVD1 Power N/A AC6 M1DQ17 I/O GVD1 AC4 VSS Ground N/A AC5 GVD1 Power N/A AC6 M1DQ17 I/O GVD1	AB20	M1DQ60	I/O	GVDD1
AB22 GPI031/J2C_SDA ^{5.8} I/O NVDD AB23 GPI027/TMR4/RCW_SRC0 ^{5.8} I/O NVDD AB24 GPI025/TMR2/RCW_SRC1 ^{5.8} I/O NVDD AB25 GPI024/TMR1/RCW_SRC2 ^{5.8} I/O NVDD AB26 GPI010/RQ10/RC10 ^{5.8} I/O NVDD AB27 GPI05/RQ5/RC5 ^{5.8} I/O NVDD AB28 GPI001/RQ0/RC0 ^{5.8} I/O NVDD AC1 VSS Ground N/A AC2 GVD1 Power N/A AC3 M1DQ16 I/O GVD1 AC4 VSS Ground N/A AC5 GVD1 Power N/A AC6 M1DQ17 I/O GVD1 AC7 VSS Ground N/A AC8 GVD1 Power N/A AC6 M1DQ17 I/O GVD1 AC7 VSS Ground N/A AC8 GVD1 O GVD1	AB21	VSS	Ground	N/A
AB23 GPI027/TMR4/RCW_SRC0 ^{5,8} I/O NVDD AB24 GPI025/TMR2/RCW_SRC1 ^{5,8} I/O NVDD AB25 GPI024/TMR1/RCW_SRC2 ^{5,8} I/O NVDD AB26 GPI010/IRQ10/RC10 ^{5,8} I/O NVDD AB27 GPI05/IRQ3/RC5 ^{5,8} I/O NVDD AB28 GPI00/IRQ0/RC0 ^{5,8} I/O NVDD AC1 VSS Ground N/A AC2 GVDD1 Power N/A AC3 M1DQ16 I/O GVD1 AC4 VSS Ground N/A AC5 GVDD1 Power N/A AC6 M1DQ16 I/O GVD1 AC6 M1DQ17 I/O GVD1 AC6 M1DQ17 I/O GVD1 AC6 M1DQ17 I/O GVD1 AC7 VSS Ground N/A AC8 GVDD1 Power N/A AC9 M1BA2 O GVD1 <t< td=""><td>AB22</td><td>GPIO31/I2C_SDA^{5,8}</td><td>I/O</td><td>NVDD</td></t<>	AB22	GPIO31/I2C_SDA ^{5,8}	I/O	NVDD
AB24 GPI025/TMR2/RCW_SRC1 ^{5,8} I/O NVDD AB25 GPI024/TMR1/RCW_SRC2 ^{5,8} I/O NVDD AB26 GPI010/IRQ10/RC10 ^{5,8} I/O NVDD AB27 GPI05/IRQ5/RC5 ^{5,8} I/O NVDD AB28 GPI00/IRQ0/RC0 ^{5,8} I/O NVDD AC1 VSS Ground N/A AC2 GVDD1 Power N/A AC3 M1DQ16 I/O GVDD1 AC4 VSS Ground N/A AC5 GVDD1 Ground N/A AC6 M1DQ17 I/O GVD11 AC6 M1DQ17 I/O GVD1 AC6 M1DQ17 I/O GVD1 AC6 M1DQ17 I/O GVD1 AC6 M1DQ17 I/O GVD1 AC7 VSS Ground N/A AC8 GVD1 Power N/A AC10 VSS Ground N/A AC11	AB23	GPIO27/TMR4/RCW_SRC0 ^{5,8}	I/O	NVDD
AB25 GPI024/TMR1/RCW_SRC2 ^{5,8} I/O NVDD AB26 GPI010/IRQ10/RC10 ^{5,8} I/O NVDD AB27 GPI05/IRQ5/RC5 ^{5,8} I/O NVDD AB28 GPI00/IRQ0/RC0 ^{5,8} I/O NVDD AC1 VSS Ground N/A AC2 GVDD1 Power N/A AC3 M1DQ16 I/O GVD1 AC4 VSS Ground N/A AC5 GVD1 GVD1 GVD1 AC6 M1DQ17 I/O GVD1 AC6 M1DQ17 I/O GVD1 AC7 VSS Ground N/A AC8 GVD1 Power N/A AC9 M1BA2 O GVD1 AC10 VSS Ground N/A AC11 GVD1 Power N/A AC8 GVD1 Power N/A AC8 GVD1 Q GVD1 AC10 VS Gro	AB24	GPIO25/TMR2/RCW_SRC1 ^{5,8}	I/O	NVDD
AB26GPI010/ĪRQ10/RC10 ^{5,8} I/ONVDDAB27GPI05/ĪRQ5/RC5 ^{5,8} I/ONVDDAB28GPI00/ĪRQ0/RC0 ^{5,8} I/ONVDDAC1VSSGroundN/AAC2GVDD1PowerN/AAC3M1DQ16I/OGVDD1AC4VSSGroundN/AAC5GVDD1PowerN/AAC6M1DQ17I/OGVDD1AC7VSSGroundN/AAC8GVDD1PowerN/AAC9M1BA2OGVDD1AC10VSSGroundN/AAC11GVDD1PowerN/AAC12M1A4OGVDD1AC14GVD1PowerN/AAC15M1DQ42I/OGVDD1AC14M1DQ42I/OGVDD1AC18M1DQ48I/OGVDD1	AB25	GPIO24/TMR1/RCW_SRC2 ^{5,8}	I/O	NVDD
AB27GPIO5/IRQ5/RC5 ^{5.8} I/ONVDDAB28GPIO0/IRQ0/RC0 ^{5.8} I/ONVDDAC1VSSGroundN/AAC2GVD1PowerN/AAC3M1DQ16I/OGVDD1AC4VSSGroundN/AAC5GVD1PowerN/AAC6M1DQ17I/OGVDD1AC7VSSGroundN/AAC8GVD1PowerN/AAC9M1BA2OGVD1AC11GVD1PowerN/AAC12M1A4OGVD1AC13VSSGroundN/AAC14GVD1PowerN/AAC15M1DQ42I/OGVD1AC16VSSGroundN/AAC17GVD1PowerN/AAC18M1DQ42I/OGVD1AC18M1DQ58I/OGVD1	AB26	GPIO10/IRQ10/RC10 ^{5,8}	I/O	NVDD
AB28 GPIOUIRQO/RC0 ^{5.8} I/O NVDD AC1 VSS Ground N/A AC2 GVDD1 Power N/A AC3 M1DQ16 I/O GVDD1 AC4 VSS Ground N/A AC3 M1DQ16 I/O GVDD1 AC4 VSS Ground N/A AC5 GVDD1 Power N/A AC6 M1DQ17 I/O GVDD1 AC7 VSS Ground N/A AC8 GVDD1 O GVD1 AC7 VSS Ground N/A AC8 GVD1 O GVD1 AC10 VSS Ground N/A AC11 GVD1 O GVD1 AC12 M1A4 O GVD1 O AC13 VSS Ground N/A AC14 GVD1 Power N/A AC15 M1DQ42 I/O GVD1	AB27	GPI05/IRQ5/RC5 ^{5,8}	I/O	NVDD
AC1 VSS Ground N/A AC2 GVDD1 Power N/A AC3 M1DQ16 I/O GVDD1 AC4 VSS Ground N/A AC5 GVDD1 Power N/A AC6 M1DQ17 Power N/A AC6 M1DQ17 I/O GVDD1 AC7 VSS Ground N/A AC8 GVDD1 Power N/A AC9 M1BA2 O GVDD1 AC10 VSS Ground N/A AC11 GVDD1 Power N/A AC12 M1A4 O GVDD1 AC13 VSS Ground N/A AC14 GVDD1 Power N/A AC15 M1Dq42 I/O GVDD1 AC16 VSS Ground N/A AC16 VSS Ground N/A AC16 VSS Ground N/A	AB28	GPIO0/IRQ0/RC0 ^{5,8}	I/O	NVDD
AC2GVDD1PowerN/AAC3M1DQ16I/OGVDD1AC4VSSGroundN/AAC5GVDD1PowerN/AAC6M1DQ17I/OGVDD1AC7VSSGroundN/AAC8GVDD1GroundN/AAC9M1BA2OGVDD1AC10VSSGroundN/AAC11GVDD1OGVDD1AC12M1A4OGVDD1AC13VSSGroundN/AAC14GVD1PowerN/AAC15M1DQ42I/OGVDD1AC16VSSGroundN/AAC17GVD1I/OGVDD1AC18M1DQ58I/OGVDD1	AC1	VSS	Ground	N/A
AC3M1DQ16I/OGVDD1AC4VSSGroundN/AAC5GVDD1PowerN/AAC6M1DQ17I/OGVDD1AC7VSSGroundN/AAC8GVDD1PowerN/AAC9M1BA2OGVDD1AC10VSSGroundN/AAC11GVDD1OGVDD1AC12M1A4OGVDD1AC13VSSGroundN/AAC14GVDD1OGVDD1AC15M1DQ42I/OGVDD1AC16VSSGroundN/AAC17GVDD1M/AOAC18M1DQ58I/OGVDD1	AC2	GVDD1	Power	N/A
AC4VSSGroundN/AAC5GVDD1PowerN/AAC6M1DQ17GVDD1I/OGVDD1AC7VSSGroundN/AAC8GVDD1PowerN/AAC9M1BA2OGVDD1AC10VSSGroundN/AAC11GVDD1PowerN/AAC12M1A4OGVDD1AC13VSSGroundN/AAC14GVDD1PowerN/AAC15M1DQ42I/OGVDD1AC16VSSGroundN/AAC17GVDD1PowerN/AAC18M1DQ58I/OGVDD1	AC3	M1DQ16	I/O	GVDD1
AC5GVDD1PowerN/AAC6M1DQ17I/OGVDD1AC7VSSGroundN/AAC8GVDD1PowerN/AAC9M1BA2OGVDD1AC10VSSGroundN/AAC11GVDD1PowerN/AAC12M1A4OGVDD1AC13VSSGroundN/AAC14GVDD1PowerN/AAC15M1DQ42I/OGVDD1AC16VSSGroundN/AAC17GVDD1PowerN/A	AC4	VSS	Ground	N/A
AC6M1DQ17I/OGVDD1AC7VSSGroundN/AAC8GVDD1PowerN/AAC9M1BA2OGVDD1AC10VSSGroundN/AAC11GVDD1PowerN/AAC12M1A4OGVDD1AC13VSSGroundN/AAC14GVDD1PowerN/AAC15M1DQ42I/OGVDD1AC16VSSGroundN/AAC17GVDD1PowerN/A	AC5	GVDD1	Power	N/A
AC7VSSGroundN/AAC8GVDD1PowerN/AAC9M1BA2OGVDD1AC10VSSGroundN/AAC11GVDD1PowerN/AAC12M1A4OGVDD1AC13VSSGroundN/AAC14GVDD1PowerN/AAC15M1DQ42I/OGVDD1AC16VSSGroundN/AAC17GVDD1PowerN/A	AC6	M1DQ17	I/O	GVDD1
AC8GVDD1PowerN/AAC9M1BA2OGVDD1AC10VSSGroundN/AAC11GVDD1PowerN/AAC12M1A4OGVDD1AC13VSSGroundN/AAC14GVDD1PowerN/AAC15M1DQ42I/OGVDD1AC16VSSGroundN/AAC17GVDD1PowerN/AAC18M1DQ58I/OGVDD1	AC7	VSS	Ground	N/A
AC9M1BA2OGVDD1AC10VSSGroundN/AAC11GVDD1PowerN/AAC12M1A4OGVDD1AC13VSSGroundN/AAC14GVDD1PowerN/AAC15M1DQ42I/OGVDD1AC16VSSGroundN/AAC17GVDD1PowerN/AAC18M1DQ58I/OGVDD1	AC8	GVDD1	Power	N/A
AC10VSSGroundN/AAC11GVDD1PowerN/AAC12M1A4OGVDD1AC13VSSGroundN/AAC14GVDD1PowerN/AAC15M1DQ42I/OGVDD1AC16VSSGroundN/AAC17GVDD1PowerN/AAC18M1DQ58I/OGVDD1	AC9	M1BA2	0	GVDD1
AC11GVDD1PowerN/AAC12M1A4OGVDD1AC13VSSGroundN/AAC14GVDD1PowerN/AAC15M1DQ42I/OGVDD1AC16VSSGroundN/AAC17GVDD1PowerN/AAC18M1DQ58I/OGVDD1	AC10	VSS	Ground	N/A
AC12M1A4OGVDD1AC13VSSGroundN/AAC14GVDD1PowerN/AAC15M1DQ42I/OGVDD1AC16VSSGroundN/AAC17GVDD1PowerN/AAC18M1DQ58I/OGVDD1	AC11	GVDD1	Power	N/A
AC13VSSGroundN/AAC14GVDD1PowerN/AAC15M1DQ42I/OGVDD1AC16VSSGroundN/AAC17GVDD1PowerN/AAC18M1DQ58I/OGVDD1	AC12	M1A4	0	GVDD1
AC14 GVDD1 Power N/A AC15 M1DQ42 I/O GVDD1 AC16 VSS Ground N/A AC17 GVDD1 Power N/A AC18 M1DQ58 I/O GVDD1	AC13	VSS	Ground	N/A
AC15 M1DQ42 I/O GVDD1 AC16 VSS Ground N/A AC17 GVDD1 Power N/A AC18 M1DQ58 I/O GVDD1	AC14	GVDD1	Power	N/A
AC16 VSS Ground N/A AC17 GVDD1 Power N/A AC18 M1DQ58 I/O GVDD1	AC15	M1DQ42	I/O	GVDD1
AC17 GVDD1 Power N/A AC18 M1DQ58 I/O GVDD1	AC16	VSS	Ground	N/A
AC18 M1DQ58 I/O GVDD1	AC17	GVDD1	Power	N/A
	AC18	M1DQ58	I/O	GVDD1

Table 1. Signal List by Ball Number (continued)



Ball Number	Signal Name ^{1,2}	Pin Type ¹⁰	Power Rail Name
AE9	M1A8	0	GVDD1
AE10	GVDD1	Power	N/A
AE11	VSS	Ground	N/A
AE12	M1A0	0	GVDD1
AE13	GVDD1	Power	N/A
AE14	VSS	Ground	N/A
AE15	M1DQ39	I/O	GVDD1
AE16	GVDD1	Power	N/A
AE17	VSS	Ground	N/A
AE18	M1DQ54	I/O	GVDD1
AE19	GVDD1	Power	N/A
AE20	VSS	Ground	N/A
AE21	GPIO29/UART_TXD ^{5,8}	I/O	NVDD
AE22	TDM1TCK/GE2_RX_CLK ³	I	NVDD
AE23	TDM1RSN/GE2_RX_CTL ³	I/O	NVDD
AE24	VSS	Ground	N/A
AE25	TDM3RCK/GE1_GTX_CLK ³	I/O	NVDD
AE26	TDM3TSN/GE1_RX_CLK ³	I/O	NVDD
AE27	TDM2RSN/GE1_TD2 ³	I/O	NVDD
AE28	TDM2RDT/GE1_TD1 ³	I/O	NVDD
AF1	M1DQ28	I/O	GVDD1
AF2	M1DM3	0	GVDD1
AF3	M1DQ26	I/O	GVDD1
AF4	M1ECC4	I/O	GVDD1
AF5	M1DM8	0	GVDD1
AF6	M1ECC2	I/O	GVDD1
AF7	M1CKE1	0	GVDD1
AF8	M1CK0	0	GVDD1
AF9	M1CK0	0	GVDD1
AF10	M1BA1	0	GVDD1
AF11	M1A1	0	GVDD1
AF12	MIWE	0	GVDD1
AF13	M1DQ37	I/O	GVDD1
AF14	M1DM4	0	GVDD1
AF15	M1DQ36	I/O	GVDD1
AF16	M1DQ32	I/O	GVDD1
AF17	M1DQ55	I/O	GVDD1
AF18	M1DM6	0	GVDD1
AF19	M1DQ53	I/O	GVDD1
AF20	M1DQ52	I/O	GVDD1
AF21	GPIO28/UART_RXD ^{5,8}	I/O	NVDD
AF22	TDM0RSN/GE2_TD2 ³	I/O	NVDD
AF23	TDM0TDT/GE2_TD3 ³	I/O	NVDD
AF24	NVDD	Power	N/A
AF25	TDM2TSN/GE1_TX_CTL ³	I/O	NVDD
AF26	GE1_RX_CTL	<u> </u>	NVDD

Table 1. Signal List by Ball Number (continued)

2 Electrical Characteristics

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC8152 Reference Manual*.

2.1 Maximum Ratings

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification never occurs in the same device with a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2 describes the maximum electrical ratings for the MSC8152.

Rating	Power Rail Name	Symbol	Value	Unit
Core supply voltage • Cores 0–1	VDD	V _{DD}	-0.3 to 1.1	V
PLL supply voltage ³		V _{DDPLL0} V _{DDPLL1} V _{DDPLL2}	-0.3 to 1.1 -0.3 to 1.1 -0.3 to 1.1	V V V
M3 memory supply voltage	M3VDD	V _{DDM3}	-0.3 to 1.1	V
MAPLE-B supply voltage	MVDD	V _{DDM}	-0.3 to 1.1	V
DDR memory supply voltage DDR2 mode DDR3 mode DDR reference voltage	GVDD1, GVDD2	V _{DDDDR}	-0.3 to 1.98 -0.3 to 1.65	V V V
Input DDR voltage	WVICEI	V _{INDDR}	-0.3 to V _{DDDDR} + 0.3	V
I/O voltage excluding DDR and RapidIO lines	NVDD, QVDD	V _{DDIO}	-0.3 to 2.625	V
Input I/O voltage		V _{INIO}	–0.3 to V _{DDIO} + 0.3	V
RapidIO pad voltage	SXPVDD1, SXPVDD2	V _{DDSXP}	-0.3 to 1.26	V
Rapid I/O core voltage	SXCVDD1, SXCVDD2	V _{DDSXC}	-0.3 to 1.21	V
Rapid I/O PLL voltage ³		V _{DDRIOPLL}	-0.3 to 1.21	V
Input RapidIO I/O voltage		V _{INRIO}	–0.3 to V _{DDSXC} + 0.3	V
Operating temperature		Тј	-40 to 105	°C
Storage temperature range		T _{STG}	-55 to +150	°C

Table 2. Absolute Maximum Matings	Table 2	. Absolute	Maximum	Ratings
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Notes: 1. Functional operating conditions are given in Table 3.

2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.

3. PLL supply voltage is specified at input of the filter and not at pin of the MSC8152 (see Figure 37 and Figure 38)



2.5 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8152.

2.5.1 DDR SDRAM DC Electrical Characteristics

This section describes the DC electrical specifications for the DDR SDRAM interface of the MSC8152.

Note: DDR2 SDRAM uses $V_{DDDDR}(typ) = 1.8 V$ and DDR3 SDRAM uses $V_{DDDDR}(typ) = 1.5 V$.

2.5.1.1 DDR2 (1.8 V) SDRAM DC Electrical Characteristics

Table 6 provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR2 SDRAM.

Note: At recommended operating conditions (see Table 3) with $V_{DDDDR} = 1.8$ V.

Table 6. DDR2 SDRAM Interface DC Electrical	Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Notes	
I/O reference voltage	MV _{REF}	$0.49 \times V_{DDDDR}$	$0.51 \times V_{DDDDR}$	V	2, 3, 4	
Input high voltage	V _{IH}	MV _{REF} + 0.125	V _{DDDDR} + 0.3	V	5	
Input low voltage	V _{IL}	-0.3	MV _{REF} - 0.125	V	5	
I/O leakage current	I _{OZ}	-50	50	μΑ	6	
Output high current (V_{OUT} (VOH) = 1.37 V)	I _{ОН}	-13.4	—	mA	7	
Output low current (V _{OUT} (VOL) = 0.33 V) I_{OL} 13.4mA					7	
 Notes: 1. V_{DDDDR} is expected to be within 50 mV of the DRAM V_{DD} supply voltage at all times. The DRAM and memory controller can use the same or different sources. 2. MV_{DDD} is expected to be equal to 0.5 × V_{DDDDD} and to track V_{DDDDDD} DC variations as measured at the receiver. Peak-to-peak 						

MV_{REF} is expected to be equal to 0.5 × V_{DDDDR} and to track V_{DDDDR} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.

 V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF} with a minimum value of MV_{REF} – 0.4 and a maximum value of MV_{REF} + 0.04 V. V_{TT} should track variations in the DC-level of MV_{REF}.

4. The voltage regulator for MV_{REF} must be able to supply up to 300 μ A.

5. Input capacitance load for DQ, DQS, and DQS signals are available in the IBIS models.

6. Output leakage is measured with all outputs are disabled, $0 V \le V_{OUT} \le V_{DDDDR}$.

7. Refer to the IBIS model for the complete output IV curve characteristics.

For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC-level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to GND_{SXC}. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage GND_{SXC}. Figure 8 shows the SerDes reference clock input requirement for AC-coupled connection scheme.



Figure 8. Differential Reference Clock Input DC Requirements (External AC-Coupled)

- Single-Ended Mode
 - The reference clock can also be single-ended. The SR[1–2]_REF_CLK input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from V_{MIN} to V_{MAX}) with SR[1–2]_REF_CLK either left unconnected or tied to ground.
 - The SR[1–2]_REF_CLK input average voltage must be between 200 and 400 mV. Figure 9 shows the SerDes
 reference clock input requirement for single-ended signalling mode.
 - To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase (SR[1-2]_REF_CLK) through the same source impedance as the clock input (SR[1-2]_REF_CLK) in use.



Figure 9. Single-Ended Reference Clock Input DC Requirements

2.5.3.2 DC-Level Requirements for PCI Express Configurations

The DC-level requirements for PCI Express implementations have separate requirements for the Tx and Rx lines. The MSC8152 supports a 2.5 Gbps PCI Express interface defined by the *PCI Express Base Specification, Revision 1.0a*. The transmitter specifications are defined in Table 11 and the receiver specifications are defined in Table 12.



Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Table TT. FULLADIESS (2.3 UDDS) DITIETETILIAI TIATSTITUET (TA) UUDUL DU SDEUTIUAUUT

Parameter	Symbol	Min	Typical	Мах	Units	Notes		
Differential peak-to-peak output voltage	V _{TX-DIFFp-p}	800	1000	1200	mV	1		
De-emphasized differential output voltage (ratio)	V _{TX-DE-RATIO}	3.0	3.5	4.0	dB	2		
DC differential Tx impedance	Z _{TX-DIFF-DC}	80	100	120	Ω	3		
Transmitter DC impedance	Z _{TX-DC}	40	50	60	Ω	4		
Notes: 1 V 2 × V V Measured at the package pips with a test load of 50 O to CND on each pip								

V_{TX-DIFFp-p} = 2 × |V_{TX-D+} - V_{TX-D-}| Measured at the package pins with a test load of 50 Ω to GND on each pin.
 Ratio of the V_{TX-DIFFp-p} of the second and following bits after a transition divided by the V_{TX-DIFFp-p} of the first bit after a

2. Ratio of the $v_{TX-DIFF_{P}P}$ of the second and following bits after a transition divided by the v_{TX-DI} transition. Measured at the package pins with a test load of 50 Ω to GND on each pin.

3. Tx DC differential mode low impedance

4. Required Tx D+ as well as D– DC Impedance during all states

Table 12. PCI Express (2.5 Gbps) Differential Receiver (Rx) Input DC Specifications

Parameter	Symbol	Min	Typical	Мах	Units	Notes
Differential input peak-to-peak voltage	V _{RX-DIFFp-p}	120	1000	1200	mV	1
DC differential Input Impedance	Z _{RX-DIFF-DC}	80	100	120	Ω	2
DC input impedance	Z _{RX-DC}	40	50	60	Ω	3
Powered down DC input impedance	Z _{RX-HIGH-IMP-DC}	50	—	—	KΩ	4
Electrical idle detect threshold	V _{RX-IDLE-DET-DIFFp-p}	65	—	175	mV	5

V_{RX-DIFFp-p} = 2 × |V_{RX-D+} - V_{RX-D-}| Measured at the package pins with a test load of 50 Ω to GND on each pin.
 Rx DC differential mode impedance. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.

3. Required Rx D+ as well as D– DC Impedance (50 ±20% tolerance). Measured at the package pins with a test load of 50 Ω to GND on each pin. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.

4. Required Rx D+ as well as D– DC Impedance when the receiver terminations do not have power. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.

5. $V_{RX-IDLE-DET-DIFFp-p} = 2 \times |V_{RX-D+} - V_{RX-D-}|$. Measured at the package pins of the receiver

2.5.3.3 DC-Level Requirements for Serial RapidIO Configurations

This sections provided various DC-level requirements for Serial RapidIO Configurations.

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Table 13. Serial RapidIO Transmitter DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Notes		
Output voltage	V _O	-0.40	—	2.30	V	1		
Long run differential output voltage	V _{DIFFPP}	800	—	1600	mVp-p	—		
Short run differential output voltage V _{DIFFPP} 500 — 1000 mVp-p —								
Note: Voltage relative to COMMON of either signal comprising a differential pair.								



Parameter	Symbol	Min	Typical	Мах	Units	Notes
Differential input voltage	V _{IN}	200	—	1600	mVp-p	1
Notes: 1. Measured at receiver.						

Table 14. Serial RapidIO Receiver DC Specifications

DC-Level Requirements for SGMII Configurations 2.5.3.4

Note: Specifications are valid at the recommended operating conditions listed in Table 3

Table 15 describes the SGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SR[1–2]_TX[n] and $\overline{SR[1-2]_TX}[n]$) as shown in Figure 10.

Parameter	Symbol	Min	Тур	Max	Unit	Notes	
Output high voltage	V _{OH}	-	_	XV _{DD_SRDS-Typ} /2 + V _{OD} _{-max} /2	mV	1	
Output low voltage	V _{OL}	$XV_{DD_SRDS-Typ}/2 - V_{OD} _{max}/2$	—	—	mV	1	
Output differential	V _{OD}	323	500	725	mV	2,3,4	
voltage (XV _{DD-Typ} at		296	459	665		2,3,5	
1.0 V)		269	417	604		2,3,6	
		243	376	545		2,3,7	
		215	333	483		2,3,8	
		189	292	424		2,3,9	
		162	250	362		2,3,10	
Output impedance R_0 40 50 60 Ω - (single-ended)							
 Notes: 1. This does not align to DC-coupled SGMII. XV_{DD_SRDS2-Typ} = 1.1 V. 2. The V_{OD} value shown in the table assumes full multitude by setting srd_smit_lvl as 000 and the following transmit equalization setting in the XMITEQAB (for lanes A and B) or XMITEQEF (for lanes E and F) bit field of Control Register: 							

Table 15. SGMII DC Transmitter Electrical Characteristics

The MSB (bit 0) of the above bit field is set to zero (selecting the full V_{DD-DIFF-p-p} amplitude which is power up default);

• The LSB (bit [1-3]) of the above bit field is set based on the equalization settings listed in notes 4 through 10. The $|V_{OD}|$ value shown in the Typ column is based on the condition of $XV_{DD_SRDS2-Typ} = 1.0 V$, no common mode offset 3. variation (V_{OS} =500mV), SerDes transmitter is terminated with 100- Ω differential load between

- Equalization setting: 1.0x: 0000. 4.
- Equalization setting: 1.09x: 1000. 5.
- Equalization setting: 1.2x: 0100. 6.
- 7. Equalization setting: 1.33x: 1100.
- Equalization setting: 1.5x: 0010. 8.
- Equalization setting: 1.71x: 1010. 9.
- 10. Equalization setting: 2.0x: 0110.
- 11. $|V_{OD}| = |V_{SR[1-2]_TXn} V_{\overline{SR[1-2]_TXn}}|$. $|V_{OD}|$ is also referred to as output differential peak voltage. $V_{TX-DIFF_{P-P}} = 2^*|V_{OD}|$



Table 21. DDR SDRAM Output AC Timing Specifications (continued)

		Parameter	Symbol ¹	Min	Max	Unit	Notes	
Notes:	1.	The symbols used for timing specifications follow the pattern of t _{(first two letters of functional block)(signal)(state)} (reference)(state) for inputs and t _(first two letters of functional block) (reference)(state)(signal)(state) for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t _{DDKHAS} symbolizes DDR timing (DD) for the time t _{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t _{DDKLDX} symbolizes DDR timing (DD) for the time t _{MCK} memory clock reference (K) are setup (S) or output valid time. Also, t _{DDKLDX} symbolizes DDR timing (DD) for the time t _{MCK} memory clock reference (K) are setup (S) or output valid time.						
	2. 3.	All MCK/MCK referenced measurements are made from the crossing of the two signals. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ/MECC/MDM/MDQS.						
	4.	Note that t _{DDKHMH} follows the symbol converting edge of the MCK(n) clock (KH the DQSS override bits in the TIMING_CFG_CLK_CNTL register. The timing parameters adjustment value. See the <i>MSC8152 Refere</i> enabled by use of these bits.	ntions described) until the MDQS _2 register. This listed in the table nce Manual for a	in note 1. For example signal is valid (MH). t will typically be set to a assume that these tw a description and unde	e, t _{DDKHMH} describes t _{DDKHMH} can be modified the same delay as the vo parameters have be erstanding of the timing	he DDR tim ed through o clock adjus een set to th modificatio	ning (DD) control of st in the ne same ons	
	5. C	Determined by maximum possible skew betw (MECC), or data mask (MDM). The data stro	veen a data strol be should be ce	be (MDQS) and any contered inside of the date	orresponding bit of dat ata eye at the pins of th	a (MDQ), E ne MSC815	2.	
	ю.	At recommended operating conditions with V	/ _{DDDDR} (1.5 V or	1,8 V) ± 5%.				

Note: For the ADDR/CMD setup and hold specifications in Table 21, it is assumed that the clock control register is set to adjust the memory clocks by ¹/₂ applied cycle.

Figure 12 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).



Figure 12. MCK to MDQS Timing



Table 24. SR[1–2]_REF_CLK and SR[1–2]_REF_CLK Input Clock Requirements (continued)

		Parameter	Symbol	Min	Typical	Max	Units	Notes	
Notes:	1.	Caution: Only 100 and 125 have b	een tested. Other va	lues will not wo	rk correctly with	n the rest of the	system.		
	2.	Limits from PCI Express CEM Rev	1.0a						
	3.	Measured from -200 mV to +200 mV on the differential waveform (derived from SR[1-2]_REF_CLK minus							
		SR[1-2]_REF_CLK). The signal m	ust be monotonic th	rough the meas	urement region	for rise and fal	l time. The 400	mV	
		measurement window is centered	on the differential ze	ro crossing. Se	e Figure 16.				
	4.	Measurement taken from differenti	al waveform						
	5.	Measurement taken from single-er	nded waveform						
	6.	Matching applies to rising edge for	SR[1-2]_REF_CLK	and falling edg	e rate for SR[1-	-2]_REF_CLK.	It is measured	using a	
		200 mV window centered on the m	edian cross point wl	here SR[1-2]_R	REF_CLK rising	meets SR[1-2]	_REF_CLK fall	ing. The	
		median cross point is used to calc	ulate the voltage thre	sholds that the	oscilloscope us	ses for the edge	e rate calculation	ns. The	
		rise edge rate of SR[1-2]_REF_CI	K should be compa	red to the fall ed	dge rate of SR[1–2]_REF_CLK	; the maximum	allowed	
		difference should not exceed 20%	of the slowest edge	rate. See Figure	e 17.				



Figure 16. Differential Measurement Points for Rise and Fall Time



Figure 17. Single-Ended Measurement Points for Rise and Fall Time Matching



Serial RapidIO AC Timing Specifications 2.6.2.3

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Table 27 defines the transmitter AC specifications for the Serial RapidIO interface. The AC timing specifications do not include REF_CLK jitter.

Table 27. Serial RapidIO T	Transmitter AC	Timing	Specifications
----------------------------	----------------	--------	----------------

Characteristic	Symbol	Min	Typical	Max	Unit
Deterministic Jitter	J _D	—	—	0.17	UI p-p
Total Jitter	J _T	—	_	0.35	UI p-p
Unit Interval: 1.25 GBaud	UI	800 – 100ppm	800	800 + 100ppm	ps
Unit Interval: 2.5 GBaud	UI	400 – 100ppm	400	400 + 100ppm	ps
Unit Interval: 3.125 GBaud	UI	320 – 100ppm	320	320 + 100ppm	ps

Table 28 defines the Receiver AC specifications for the Serial RapidIO interface. The AC timing specifications do not include REF_CLK jitter.

Table 28. Serial RapidIO Receiver AC Timing Specifications

Characteristic	Symbol	Min	Typical	Max	Unit	Notes
Deterministic Jitter Tolerance	J _D	0.37	_	—	UI p-p	1
Combined Deterministic and Random Jitter Tolerance	J _{DR}	0.55	_	—	UI p-p	1
Total Jitter Tolerance	J _T	0.65		—	UI p-p	1, 2
Bit Error Rate	BER	—	_	10 ⁻¹²	_	—
Unit Interval: 1.25 GBaud	UI	800 – 100ppm	800	800 + 100ppm	ps	—
Unit Interval: 2.5 GBaud	UI	400 – 100ppm	400	400 + 100ppm	ps	—
Unit Interval: 3.125 GBaud	UI	320 – 100ppm	320	320 + 100ppm	ps	_
Notes: 1 Measured at receiver						

Total jitter is composed of three components, deterministic jitter, random jitter, and single frequency sinusoidal jitter. The 2. sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 18. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.



Figure 18. Single Frequency Sinusoidal Jitter Limits





2.6.7 Asynchronous Signal Timing

Table 35 lists the asynchronous signal timing specifications.

Table 37. Signal Timing

Characteristics	Symbol	Туре	Min				
Input	t _{IN}	Asynchronous	One CLKIN cycle				
Output	t _{OUT}	Asynchronous	Application dependent				
Note: Input value relevant for EE0, IRQ[15–0], and NMI only.							

The following interfaces use the specified asynchronous signals:

• *GPIO*. Signals GPIO[31–0], when used as GPIO signals, that is, when the alternate multiplexed special functions are not selected.

Note: When used as a general purpose input (GPI), the input signal should be driven until it is acknowledged by the MSC8152 device, that is, when the expected input value is read from the GPIO data register.

- *EE port*. Signals EE0, EE1.
- *Boot function*. Signal STOP_BS.
- I^2C interface. Signals I2C_SCL and I2C_SDA.
- Interrupt inputs. Signals IRQ[15–0] and NMI.
- Interrupt outputs. Signals INT_OUT and NMI_OUT (minimum pulse width is 32 ns).

2.6.8 JTAG Signals

Table 38 lists the JTAG timing specifications shown in Figure 29 through Figure 32.

Table 38. JTAG Timing

Characteristics		All frequencies		l lmit
Characteristics	Symbol	Min	Max	Unit
TCK cycle time	t _{тскх}	36.0	—	ns
TCK clock high phase measured at $V_{M} = V_{DDIO}/2$	t _{тскн}	15.0	—	ns
Boundary scan input data setup time	t _{BSVKH}	0.0	—	ns
Boundary scan input data hold time	t _{BSXKH}	15.0	—	ns
TCK fall to output data valid	t _{TCKHOV}	—	20.0	ns
TCK fall to output high impedance	t _{TCKHOZ}	—	24.0	ns
TMS, TDI data setup time	t _{TDIVKH}	0.0	—	ns
TMS, TDI data hold time	t _{TDIXKH}	5.0	—	ns
TCK fall to TDO data valid	t _{TDOHOV}	—	10.0	ns
TCK fall to TDO high impedance	t _{TDOHOZ}	—	12.0	ns
TRST assert time	t _{TRST}	100.0	—	ns
Note: All timings apply to OnCE module data transfers as well as any other transfers via the JTAG port.				

Figure 29 shows the test clock input timing diagram



Figure 29. Test Clock Input Timing



NP

ware Design Considerations

3 Hardware Design Considerations

The following sections discuss areas to consider when the MSC8152 device is designed into a system.

3.1 Power Supply Ramp-Up Sequence

The following subsections describe the required device initialization sequence.

3.1.1 Clock, Reset, and Supply Coordination

Starting the device requires coordination between several inputs including: clock, reset, and power supplies. Follow this guidelines when starting up an MSC8152 device:

- <u>PORESET</u> and <u>TRST</u> must be asserted externally for the duration of the supply ramp-up, using the V_{DDIO} supply. <u>TRST</u> deassertion does not have to be synchronized with <u>PORESET</u> deassertion. However, <u>TRST</u> must be deasserted before normal operation begins to ensure correct functionality of the device.
- CLKIN should toggle at least 32 cycles before PORESET deassertion to guarantee correct device operation. The 32 cycles should only be counted from the time after V_{DDIO} reaches its nominal value (see timing 1 in Figure 33).
- CLKIN should either be stable low during ramp-up of V_{DDIO} supply (and start its swings after ramp-up) or should swing within V_{DDIO} range during V_{DDIO} ramp-up, so its amplitude grows as V_{DDIO} grows during ramp-up.

Figure 33 shows a sequence in which V_{DDIO} ramps-up after V_{DD} and CLKIN begins to toggle with the raise of V_{DDIO} supply.



Figure 33. Supply Ramp-Up Sequence with V_{DD} Ramping Before V_{DDIO} and CLKIN Starting With V_{DDIO}

Note: For details on power-on reset flow and duration, see the Reset chapter in the MSC8152 Reference Manual.

3.2 PLL Power Supply Design Considerations

Each global PLL power supply must have an external RC filter for the PLLn_AVDD input (see Figure 37) in which the following components are defined as listed:

- $R = 5 \ \Omega \pm 5\%$
- $C1 = 10 \ \mu\text{F} \pm 10\%$, 0603, X5R, with ESL $\leq 0.5 \ \text{nH}$, low ESL Surface Mount Capacitor.
- $C2 = 1.0 \ \mu\text{F} \pm 10\%$, 0402, X5R, with ESL $\leq 0.5 \ \text{nH}$, low ESL Surface Mount Capacitor.

Note: A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change.

All three PLLs can connect to a single supply voltage source (such as a voltage regulator) as long as the external RC filter is applied to each PLL separately. For optimal noise filtering, place the circuit as close as possible to its PLLn_AVDD inputs.



Figure 37. PLL Supplies

Each SerDes PLL power supply must be filtered using a circuit similar to the one shown in Figure 38, to ensure stability of the internal clock. For maximum effectiveness, the filter circuit should be placed as closely as possible to the SRn_PLL_AVDD ball to ensure it filters out as much noise as possible. The ground connection should be near the SRn_PLL_AVDD ball. The 0.003 μ F capacitor is closest to the ball, followed by the two 2.2 μ F capacitors, and finally the 1 Ω resistor to the board supply plane. The capacitors are connected from SRn_PLL_AVDD to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All trances should be kept short, wide, and direct.



Figure 38. SerDes PLL Supplies





3.5 Connectivity Guidelines

Note: Although the package actually uses a ball grid array, the more conventional term pin is used to denote signal connections in this discussion.

First, select the pin multiplexing mode to allocate the required I/O signals. Then use the guidelines presented in the following subsections for board design and connections. The following conventions are used in describing the connectivity requirements:

- GND indicates using a 10 kΩ pull-down resistor (recommended) or a direct connection to the ground plane. Direct connections to the ground plane may yield DC current up to 50 mA through the I/O supply that adds to overall power consumption.
- 2. V_{DD} indicates using a 10 k Ω pull-up resistor (recommended) or a direct connection to the appropriate power supply. Direct connections to the supply may yield DC current up to 50 mA through the I/O supply that adds to overall power consumption.
- 3. Mandatory use of a pull-up or pull-down resistor is clearly indicated as "pull-up/pull-down." For buses, each pin on the bus should have its own resistor.
- 4. NC indicates "not connected" and means do not connect anything to the pin.
- 5. The phrase "in use" indicates a typical pin connection for the required function.
- **Note:** Please see recommendations #1 and #2 as mandatory pull-down or pull-up connection for unused pins in case of subset interface connection.



ware Design Considerations

Table 48. Connectivity of TDM Related Pins When TDM Interface Is Not Used

Signal Name		Signal Name	Pin Connection		
TDM n TCL	K		GND		
TDMT n DA	١T		GND		
TDM n TSY	'N		GND		
V _{DDIO}			2.5 V		
Notes:	1. 2.	 n = {0, 1, 2,3} In case of subset of TDM interface usage please make sure to disable unused TDM modules. See <i>TDM</i> chapter in the <i>MSC8152 Reference Manual</i> for details. 			

3.5.5 Miscellaneous Pins

Table 49 lists the board connections for the pins not required by the system design. Table 49 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 49. Connectivity of Individual Pins When They Are Not Required

Signal Name	Pin Connection		
CLKOUT	NC		
EE0	GND		
EE1	NC		
GPIO[31–0]	NC		
SCL	See the GPIO connectivity guidelines in this table.		
SDA	See the GPIO connectivity guidelines in this table.		
INT_OUT	NC		
IRQ[15–0]	See the GPIO connectivity guidelines in this table.		
NMI	V _{DDIO}		
NMI_OUT	NC		
RC[21–0]	GND		
STOP_BS	GND		
тск	GND		
TDI	GND		
TDO	NC		
TMR[4–0]	See the GPIO connectivity guidelines in this table.		
TMS	GND		
TRST	See Section 3.1 for guidelines.		
URXD	See the GPIO connectivity guidelines in this table.		
UTXD	See the GPIO connectivity guidelines in this table.		
DDN[1-0]	See the GPIO connectivity guidelines in this table.		
DRQ[1-0]	See the GPIO connectivity guidelines in this table.		
RCW_LSEL_0	GND		
RCW_LSEL_1	GND		
RCW_LSEL_2	GND		
RCW_LSEL_3	GND		
V _{DDIO}	2.5 V		

Note: For details on configuration, see the *MSC8152 Reference Manual*. For additional information, refer to the *MSC815x* and *MSC825x DSP Family Design Checklist*.

MSC8152 Dual-Core Digital Signal Processor Data Sheet, Rev. 6



3.6 Guide to Selecting Connections for Remote Power Supply Sensing

To assure consistency of input power levels, some applications use a practice of connecting the remote sense signal input of an on-board power supply to one of power supply pins of the IC device. The advantage of using this connection is the ability to compensate for the slow components of the IR drop caused by resistive supply current path from on-board power supply to the pins layer on the package. However, because of specific device requirements, not every ball connection can be selected as the remote sense pin. Some of these pins must be connected to the appropriate power supply or ground to ensure correct device functionality. Some connections supply critical power to a specific high usage area of the IC die; using such a connection as a non-supply pin could impact necessary supply current during high current events. The following balls can be used as the board supply remote sense output without degrading the power and ground supply quality:

- *VDD:* W10, T19
- VSS: J18, Y10
- M3VDD: None

Do not use any other connections for remote sensing. Use of any other connections for this purpose can result in application and device failure.

4 Ordering Information

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

Qual Status	Cores	Encryption	Temeprature Range	Package Type	Core Frequency	Die Revision
PC = Prototype MSC = Production	8152 = 2 Core	[blank] = Non-encrypted	S = 0° to 105°C T = -40°C to 105°C	VT = FC-PBGA Lead Free AG = FC-PBGA C4/C5 Lead Free	1000 = 1Ghz	B = Rev 2.1