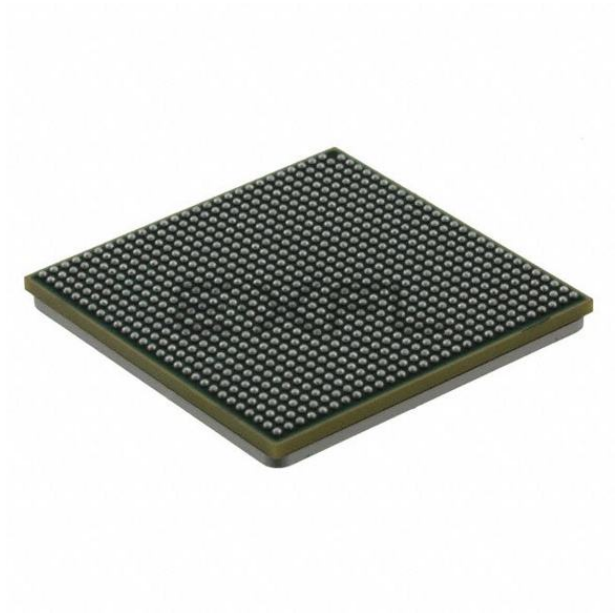

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3850 Dual Core
Interface	Ethernet, I²C, PCI, RGMII, Serial RapidIO, SGMII, SPI, UART/USART
Clock Rate	1GHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	576kB
Voltage - I/O	2.50V
Voltage - Core	1.00V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8152tag1000b

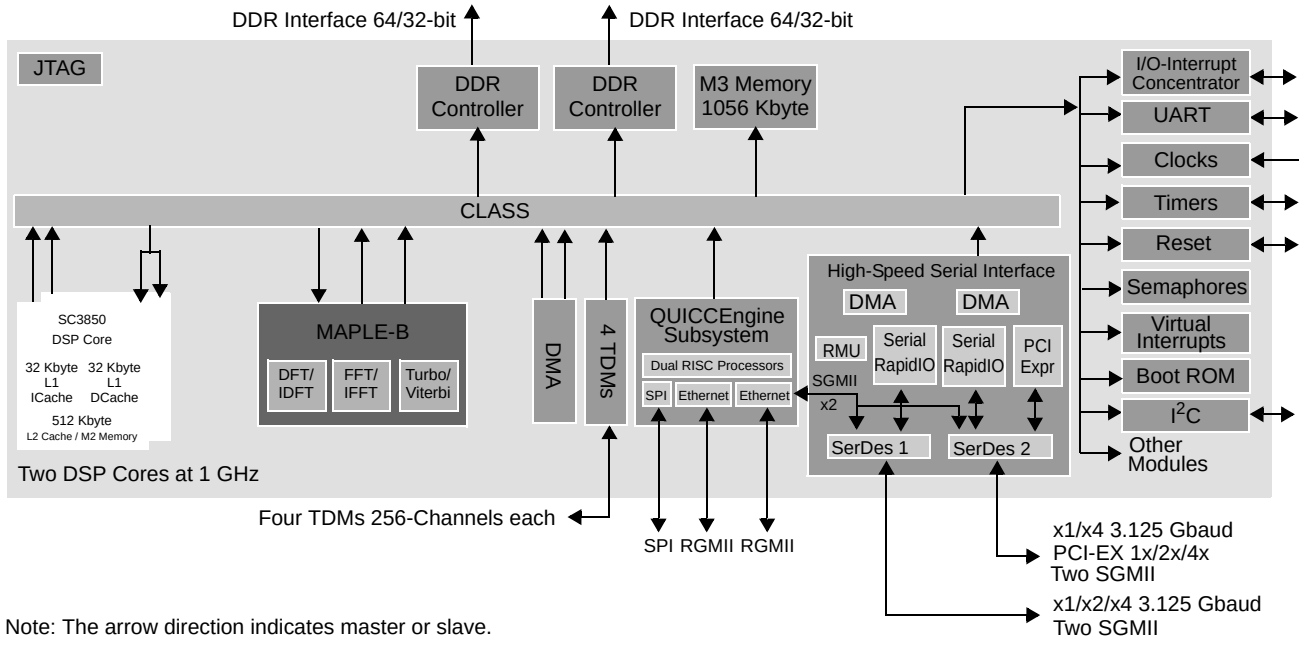

Figure 1. MSC8152 Block Diagram

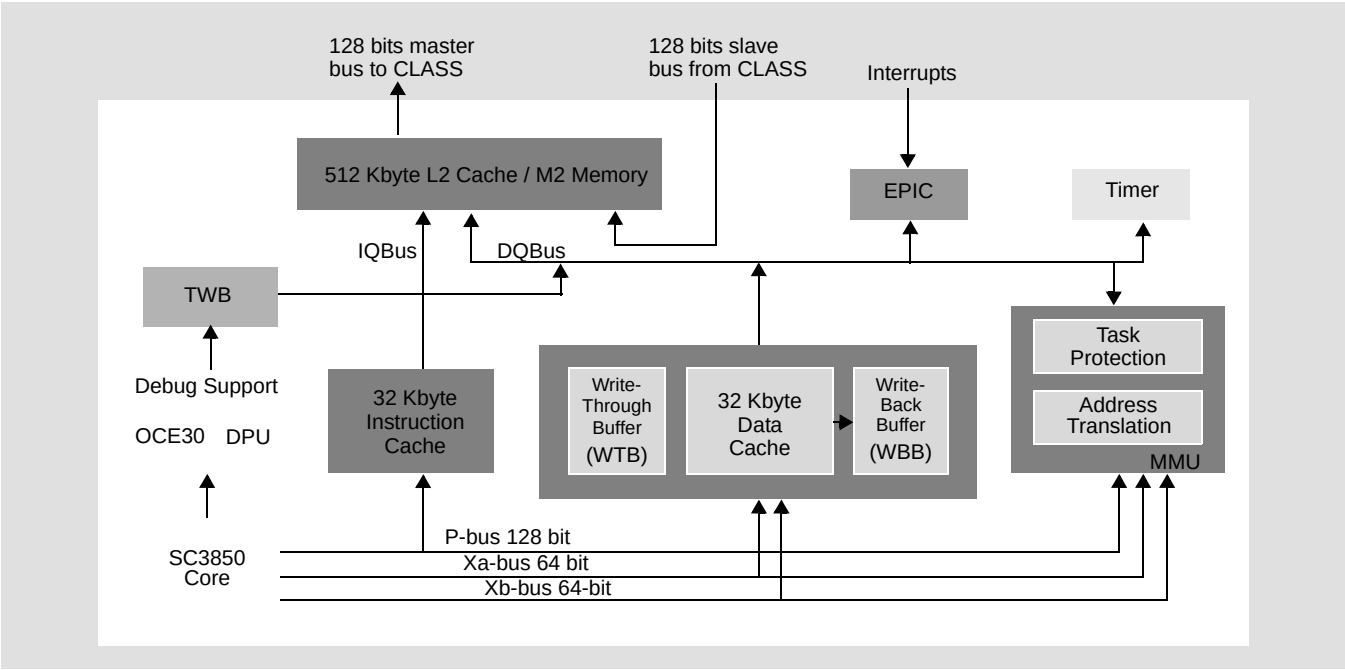

Figure 2. StarCore SC3850 DSP Subsystem Block Diagram

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
K15	VDD	Power	N/A
K16	VSS	Ground	N/A
K17	VSS	Ground	N/A
K18	VSS	Ground	N/A
K19	VDD	Power	N/A
K20	Reserved	NC	—
K21	Reserved	NC	—
K22	Reserved	NC	—
K23	SXPVDD2	Power	N/A
K24	SXPVSS2	Ground	N/A
K25	SXCVDD2	Power	N/A
K26	SXCVSS2	Ground	N/A
K27	SXCVDD2	Power	N/A
K28	SXCVSS2	Ground	N/A
L1	M2DQ9	I/O	GVDD2
L2	M2DQ12	I/O	GVDD2
L3	M2DQ13	I/O	GVDD2
L4	$\overline{\text{M2DQS0}}$	I/O	GVDD2
L5	M2DQS0	I/O	GVDD2
L6	M2DM0	O	GVDD2
L7	M2DQ3	I/O	GVDD2
L8	M2DQ2	I/O	GVDD2
L9	M2DQ4	I/O	GVDD2
L10	VDD	Power	N/A
L11	VSS	Ground	N/A
L12	M3VDD	Power	N/A
L13	VSS	Ground	N/A
L14	VSS	Ground	N/A
L15	VSS	Ground	N/A
L16	VSS	Ground	N/A
L17	VSS	Ground	N/A
L18	VDD	Power	N/A
L19	VSS	Ground	N/A
L20	Reserved	NC	—
L21	Reserved	NC	—
L22	Reserved	NC	—
L23	SR2_TXD3/PE_TXD3/SG2_TX[4]	O	SXPVDD2
L24	$\overline{\text{SR2\_TXD3}}$/$\overline{\text{PE\_TXD3}}$/$\overline{\text{SG2\_TX}}$[4]	O	SXPVDD2
L25	SXCVSS2	Ground	N/A
L26	SXCVDD2	Power	N/A
L27	$\overline{\text{SR2\_RXD3}}$/$\overline{\text{PE\_RXD3}}$/$\overline{\text{SG2\_RX}}$[4]	I	SXCVDD2
L28	SR2_RXD3/PE_RXD3/SG2_RX[4]	I	SXCVDD2
M1	M2DQ8	I/O	GVDD2
M2	VSS	Ground	N/A
M3	GVDD2	Power	N/A
M4	M2DQ15	I/O	GVDD2

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
N23	SR2_TXD2/PE_TXD2/SG1_TX[4]	O	SXPVDD2
N24	$\overline{\text{SR2\_TXD2}}$/$\overline{\text{PE\_TXD2}}$/$\overline{\text{SG1\_TX}}$[4]	O	SXPVDD2
N25	SXCVDD2	Power	N/A
N26	SXCVSS2	Ground	N/A
N27	$\overline{\text{SR2\_RXD2}}$/$\overline{\text{PE\_RXD2}}$/$\overline{\text{SG1\_RX}}$[4]	I	SXCVDD2
N28	SR2_RXD2/PE_RXD2/SG1_RX[4]	I	SXCVDD2
P1	CLKIN	I	QVDD
P2	EE0	I	QVDD
P3	QVDD	Power	N/A
P4	VSS	Ground	N/A
P5	STOP_BS	I	QVDD
P6	QVDD	Power	N/A
P7	VSS	Ground	N/A
P8	PLL0_AVDD[9]	Power	VDD
P9	PLL2_AVDD[9]	Power	VDD
P10	VSS	Ground	N/A
P11	VDD	Power	N/A
P12	VSS	Ground	N/A
P13	VDD	Power	N/A
P14	VSS	Ground	N/A
P15	MVDD	Power	N/A
P16	VSS	Ground	N/A
P17	MVDD	Power	N/A
P18	VSS	Ground	N/A
P19	VDD	Power	N/A
P20	Reserved	NC	—
P21	Reserved	NC	—
P22	Reserved	NC	—
P23	SXPVDD2	Power	N/A
P24	SXPVSS2	Ground	N/A
P25	SR2_PLL_AGND[9]	Ground	SXCVSS2
P26	SR2_PLL_AVDD[9]	Power	SXCVDD2
P27	SXCVSS2	Ground	N/A
P28	SXCVDD2	Power	N/A
R1	VSS	Ground	N/A
R2	$\overline{\text{NMI}}$	I	QVDD
R3	$\overline{\text{NMI\_OUT}}$[6]	O	QVDD
R4	$\overline{\text{HRESET}}$[6,7]	I/O	QVDD
R5	$\overline{\text{INT\_OUT}}$[6]	O	QVDD
R6	EE1	O	QVDD
R7	VSS	Ground	N/A
R8	PLL1_AVDD[9]	Power	VDD
R9	VSS	Ground	N/A
R10	VDD	Power	N/A
R11	VSS	Non-user	N/A
R12	VDD	Power	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
R13	VSS	Ground	N/A
R14	VDD	Power	N/A
R15	VSS	Ground	N/A
R16	MVDD	Power	N/A
R17	VSS	Ground	N/A
R18	VDD	Power	N/A
R19	VSS	Ground	N/A
R20	VSS	Non-user	N/A
R21	SXPVSS2	Ground	N/A
R22	SXPVDD2	Power	N/A
R23	SR2_TXD1/PE_TXD1[4]	O	SXPVDD2
R24	$\overline{\text{SR2\_TXD1}}$/$\overline{\text{PE\_TXD1}}$[4]	O	SXPVDD2
R25	SXCVSS2	Ground	N/A
R26	SXCVDD2	Power	N/A
R27	$\overline{\text{SR2\_RXD1}}$/$\overline{\text{PE\_RXD1}}$[4]	I	SXCVDD2
R28	SR2_RXD1/PE_RXD1[4]	I	SXCVDD2
T1	VSS	Ground	N/A
T2	TCK	I	QVDD
T3	$\overline{\text{SRESET}}$[6,7]	I/O	QVDD
T4	TDI	I	QVDD
T5	VSS	Ground	N/A
T6	TDO	O	QVDD
T7	VSS	Ground	N/A
T8	VSS	Ground	N/A
T9	QVDD	Power	N/A
T10	VSS	Ground	N/A
T11	VDD	Power	N/A
T12	VSS	Ground	N/A
T13	M3VDD	Power	N/A
T14	VSS	Ground	N/A
T15	VDD	Power	N/A
T16	VSS	Ground	N/A
T17	MVDD	Power	N/A
T18	VSS	Ground	N/A
T19	VDD	Power	N/A
T20	VSS	Ground	N/A
T21	VSS	Non-user	N/A
T22	SR2_IMP_CAL_RX	I	SXCVDD2
T23	SXPVSS2	Ground	N/A
T24	SXPVDD2	Power	N/A
T25	SR2_REF_CLK	I	SXCVDD2
T26	$\overline{\text{SR2\_REF\_CLK}}$	I	SXCVDD2
T27	Reserved	NC	—
T28	Reserved	NC	—
U1	M1DQ8	I/O	GVDD1
U2	VSS	Ground	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
U3	GVDD1	Power	N/A
U4	M1DQ15	I/O	GVDD1
U5	M1DQ1	I/O	GVDD1
U6	VSS	Ground	N/A
U7	GVDD1	Power	N/A
U8	M1DQ7	I/O	GVDD1
U9	M1DQ6	I/O	GVDD1
U10	VDD	Power	N/A
U11	VSS	Ground	N/A
U12	M3VDD	Power	N/A
U13	VSS	Ground	N/A
U14	VDD	Power	N/A
U15	VSS	Ground	N/A
U16	VDD	Power	N/A
U17	VSS	Ground	N/A
U18	VDD	Power	N/A
U19	VSS	Ground	N/A
U20	VSS	Ground	N/A
U21	VSS	Ground	N/A
U22	VSS	Non-user	N/A
U23	SR2_TXD0/PE_TXD0[4]	O	SXPVDD2
U24	$\overline{\text{SR2\_TXD0}}/\overline{\text{PE\_TXD0}}$[4]	O	SXPVDD2
U25	SXCVDD2	Power	N/A
U26	SXCVSS2	Ground	N/A
U27	$\overline{\text{SR2\_RXD0}}/\overline{\text{PE\_RXD0}}$[4]	I	SXCVDD2
U28	SR2_RXD0/PE_RXD0[4]	I	SXCVDD2
V1	M1DQ9	I/O	GVDD1
V2	M1DQ12	I/O	GVDD1
V3	M1DQ13	I/O	GVDD1
V4	$\overline{\text{M1DQS0}}$	I/O	GVDD1
V5	M1DQS0	I/O	GVDD1
V6	M1DM0	O	GVDD1
V7	M1DQ3	I/O	GVDD1
V8	M1DQ2	I/O	GVDD1
V9	M1DQ4	I/O	GVDD1
V10	VSS	Ground	N/A
V11	VDD	Power	N/A
V12	VSS	Ground	N/A
V13	VDD	Power	N/A
V14	VSS	Ground	N/A
V15	VDD	Power	N/A
V16	VSS	Ground	N/A
V17	VDD	Power	N/A
V18	VSS	Ground	N/A
V19	VDD	Power	N/A
V20	NVDD	Power	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
V21	RCW_LSEL_3/RC20	I/O	NVDD
V22	RCW_LSEL_2/RC19	I/O	NVDD
V23	SXPVDD2	Power	N/A
V24	SXPVSS2	Ground	N/A
V25	RCW_LSEL_1/RC18	I/O	NVDD
V26	RC21	I	NVDD
V27	SXCVDD2	Power	N/A
V28	SXCVSS2	Ground	N/A
W1	VSS	Ground	N/A
W2	GVDD1	Power	N/A
W3	M1DM1	O	GVDD1
W4	VSS	Ground	N/A
W5	GVDD1	Power	N/A
W6	M1DQ0	I/O	GVDD1
W7	VSS	Ground	N/A
W8	GVDD1	Power	N/A
W9	M1DQ5	I/O	GVDD1
W10	VDD	Power	N/A
W11	VSS	Ground	N/A
W12	VDD	Power	N/A
W13	VSS	Ground	N/A
W14	VDD	Power	N/A
W15	VSS	Ground	N/A
W16	VDD	Power	N/A
W17	VSS	Ground	N/A
W18	VDD	Power	N/A
W19	VSS	Ground	N/A
W20	VSS	Ground	N/A
W21	RCW_LSEL0/RC17	I/O	NVDD
W22	GPIO19/SPI_MISO[5,8]	I/O	NVDD
W23	VSS	Ground	N/A
W24	NVDD	Power	N/A
W25	GPIO11/IRQ11/RC11[5,8]	I/O	NVDD
W26	GPIO3/DRQ1/IRQ3/RC3[5,8]	I/O	NVDD
W27	GPIO7/IRQ7/RC7[5,8]	I/O	NVDD
W28	GPIO2/IRQ2/RC2[5,8]	I/O	NVDD
Y1	M1DQS1	I/O	GVDD1
Y2	M1DQS1	I/O	GVDD1
Y3	M1DQ10	I/O	GVDD1
Y4	M1DQ11	I/O	GVDD1
Y5	M1DQ14	I/O	GVDD1
Y6	M1DQ23	I/O	GVDD1
Y7	M1ODT0	O	GVDD1
Y8	M1A12	O	GVDD1
Y9	M1A14	O	GVDD1
Y10	VSS	Ground	N/A

2.2 Recommended Operating Conditions

Table 3 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Rating	Symbol	Min	Nominal	Max	Unit
Core supply voltage	V_{DD}	0.97	1.0	1.05	V
M3 memory supply voltage	V_{DDM3}	0.97	1.0	1.05	V
MAPLE-B supply voltage	V_{DDM}	0.97	1.0	1.05	V
DDR memory supply voltage • DDR2 mode • DDR3 mode DDR reference voltage	V_{DDDDR} MV_{REF}	 1.7 1.425 $0.49 \times V_{DDDDR}$	 1.8 1.5 $0.5 \times V_{DDDDR}$	 1.9 1.575 $0.51 \times V_{DDDDR}$	 V V V
I/O voltage excluding DDR and RapidIO lines	V_{DDIO}	2.375	2.5	2.625	V
Rapid I/O pad voltage	V_{DDSXP}	0.97	1.0	1.05	V
Rapid I/O core voltage	V_{DDSXC}	0.97	1.0	1.05	V
Operating temperature range: • Standard • Higher • Extended	 T_J T_J T_A T_J	 0 0 –40 —		 90 105 — 105	 °C °C °C

2.5.1.4 DDR Reference Current Draw

Table 9 lists the current draw characteristics for MV_{REF}.

Note: Values when used at recommended operating conditions (see Table 3).

Table 9. Current Draw Characteristics for MV_{REF}

Parameter / Condition	Symbol	Min	Max	Unit
Current draw for MV_{REFn} • DDR2 SDRAM • DDR3 SDRAM	I_{MVREFn}	—	 300 250	 µA µA

2.5.2 High-Speed Serial Interface (HSSI) DC Electrical Characteristics

The MSC8152 features an HSSI that includes two 4-channel SerDes ports used for high-speed serial interface applications (PCI Express, Serial RapidIO interfaces, and SGMII). This section and its subsections describe the common portion of the SerDes DC, including the DC requirements for the SerDes reference clocks and the SerDes data lane transmitter (Tx) and receiver (Rx) reference circuits. The data lane circuit specifications are specific for each supported interface, and they have individual subsections by protocol. The selection of individual data channel functionality is done via the Reset Configuration Word High Register (RCWHR) SerDes Protocol selection fields (S1P and S2P). Specific AC electrical characteristics are defined in Section 2.6.2, “HSSI AC Timing Specifications.”

2.5.2.1 Signal Term Definitions

The SerDes interface uses differential signalling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals. Figure 4 shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. Figure 4 shows the waveform for either a transmitter output (SR[1–2]_TX and $\overline{\text{SR[1–2]\_TX}}$) or a receiver input (SR[1–2]_RX and $\overline{\text{SR[1–2]\_RX}}$). Each signal swings between A volts and B volts where A > B.

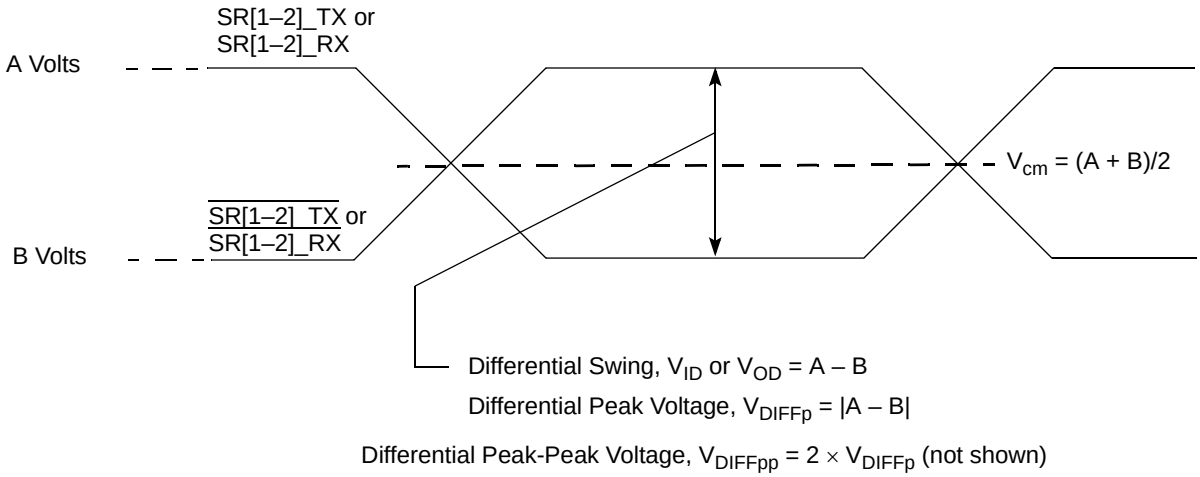

Figure 4. Differential Voltage Definitions for Transmitter or Receiver

2.5.2.2 SerDes Reference Clock Receiver Characteristics

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clock inputs are SR1_REF_CLK/$\overline{\text{SR1\_REF\_CLK}}$ or SR2_REF_CLK/$\overline{\text{SR2\_REF\_CLK}}$. Figure 5 shows a receiver reference diagram of the SerDes reference clocks.

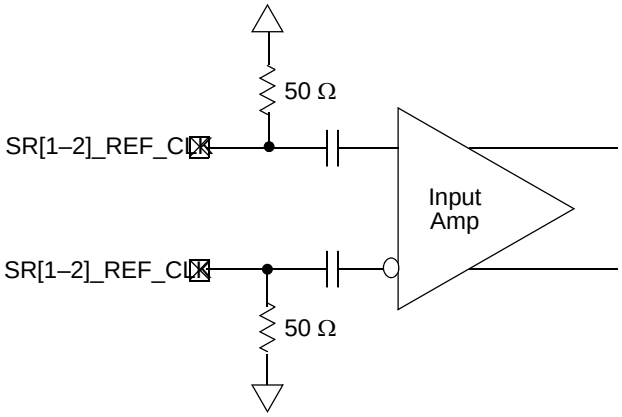

Figure 5. Receiver of SerDes Reference Clocks

The characteristics of the clock signals are as follows:

- The supply voltage requirements for V_{DDSXC} are as specified in **Table 3.**
- The SerDes reference clock receiver reference circuit structure is as follows:
  - The SR[1–2]_REF_CLK and $\overline{\text{SR[1–2]\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 5. Each differential clock input (SR[1–2]_REF_CLK or $\overline{\text{SR[1–2]\_REF\_CLK}}$) has on-chip 50-Ω termination to GND_{SXC} followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the differential mode and single-ended mode descriptions below for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V / 50 = 8 mA) while the minimum common mode input level is 0.1 V above GND_{SXC}. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SR[1–2]_REF_CLK and $\overline{\text{SR[1–2]\_REF\_CLK}}$ inputs cannot drive 50 Ω to GND_{SXC} DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled externally.
- The input amplitude requirement is described in detail in the following sections.

2.5.4 RGMII and Other Interface DC Electrical Characteristics

Table 17 describes the DC electrical characteristics for the following interfaces:

- RGMII Ethernet
- SPI
- TDM
- GPIO
- UART
- TIMER
- EE
- I^2C
- Interrupts ($\overline{\text{IRQn}}$, $\overline{\text{NMI\_OUT}}$, $\overline{\text{INT\_OUT}}$)
- Clock and resets (CLKIN, $\overline{\text{PORESET}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$)
- DMA External Request
- JTAG signals

Table 17. 2.5 V I/O DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input high current ($V_{IN} = V_{DDIO}$)	I_{IN}	—	30	μA	2
Output high voltage (V_{DDIO} = min, I_{OH} = –1.0 mA)	V_{OH}	2.0	VDDIO + 0.3	V	1
Output low voltage (V_{DDIO} = min, I_{OL}= 1.0 mA)	V_{OL}	GND – 0.3	0.40	V	1

Notes: **1.** The min V_{IL} and max V_{IH} values are based on the respective min and max V_{IN} values listed in Table 3.
2. The symbol V_{IN} represents the input voltage of the supply. It is referenced in Table 3.

Table 21. DDR SDRAM Output AC Timing Specifications (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *MSC8152 Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MSC8152.
6. At recommended operating conditions with V_{DDDDR} (1.5 V or 1,8 V) ± 5%.

Note: For the ADDR/CMD setup and hold specifications in Table 21, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

Figure 12 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

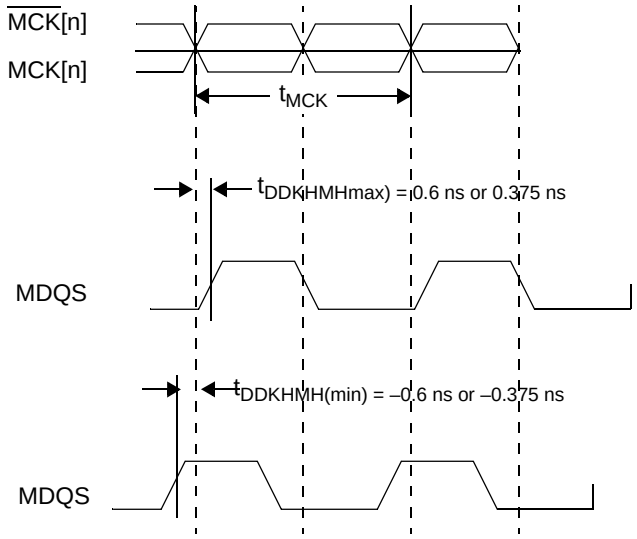

Figure 12. MCK to MDQS Timing

2.6.2.4 SGMII AC Timing Specifications

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SR[1–2]_TX[n] and $\overline{\text{SR[1–2]\_TX}}$[n]) or at the receiver inputs (SR[1–2]_RX[n] and $\overline{\text{SR[1–2]\_RX}}$[n]) as depicted in Figure 19, respectively.

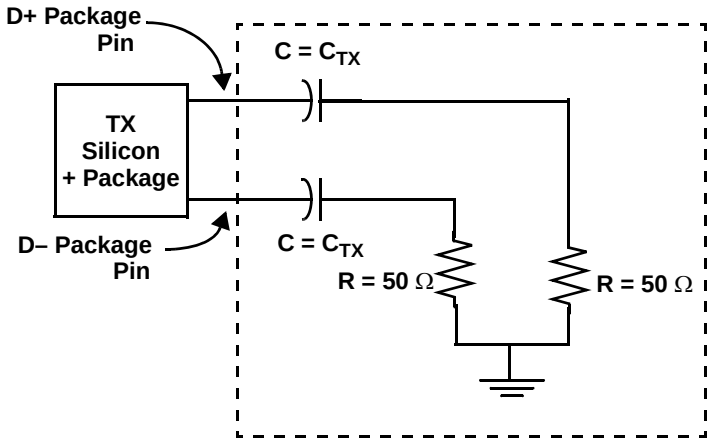

Figure 19. SGMII AC Test/Measurement Load

Table 29 provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include REF_CLK jitter.

Table 29. SGMII Transmit AC Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter	JD	—	—	0.17	UI p-p	—
Total Jitter	JT	—	—	0.35	UI p-p	2
Unit Interval	UI	799.92	800	800.08	ps	1

Notes: 1. See Figure 18 for single frequency sinusoidal jitter limits
2. Each UI is 800 ps ± 100 ppm.

Table 30 provides the SGMII receiver AC timing specifications. The AC timing specifications do not include REF_CLK jitter.

Table 30. SGMII Receive AC Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter Tolerance	JD	0.37	—	—	UI p-p	1, 2
Combined Deterministic and Random Jitter Tolerance	JDR	0.55	—	—	UI p-p	1, 2
Total Jitter Tolerance	JT	0.65	—	—	UI p-p	1,2
Bit Error Ratio	BER	—	—	10^{-12}	—	—
Unit Interval	UI	799.92	800.00	800.08	ps	3

Notes: 1. Measured at receiver.
2. Refer to RapidIO™ 1x/4x LP Serial Physical Layer Specification for interpretation of jitter specifications. Also see Figure 18.
3. Each UI is 800 ps ± 100 ppm.

2.6.5 Ethernet Timing

This section describes the AC electrical characteristics for the Ethernet interface.

There are programmable delay units (PDU) that should be programmed differently for each interface to meet timing. There is a general configuration register 4 (GCR4) used to configure the timing. For additional information, see the *MSC8152 Reference Manual*.

2.6.5.1 Management Interface Timing

Table 33 lists the timer input Ethernet controller management interface timing specifications shown in Figure 24.

Table 33. Ethernet Controller Management Interface Timing

Characteristics	Symbol	Min	Max	Unit
GE_MDC frequency	f_{MDC}	—	2.5	MHz
GE_MDC period	t_{MDC}	400	—	ns
GE_MDC clock pulse width high	t_{MDC_H}	160	—	ns
GE_MDC clock pulse width low	t_{MDC_L}	160	—	ns
GE_MDC to GE_MDIO delay[2]	t_{MDKHDX}	10	70	ns
GE_MDIO to GE_MDC rising edge setup time	t_{MDDVKH}	20	—	ns
GE_MDC rising edge to GE_MDIO hold time	t_{MDDXKH}	0	—	ns

Notes:
1. Program the GE_MDC frequency (f_{MDC}) to a maximum value of 2.5 MHz (400 ns period for t_{MDC}). The value depends on the source clock and configuration of MIIMCFG[MCS] and UPSMR[MDCP]. For example, for a source clock of 400 MHz to achieve f_{MDC} = 2.5 MHz, program MIIMCFG[MCS] = 0x4 and UPSMR[MDCP] = 0. See the *MSC8152 Reference Manual* for configuration details.
2. The value depends on the source clock. For example, for a source clock of 267 MHz, the delay is 70 ns. For a source clock of 333 MHz, the delay is 58 ns.

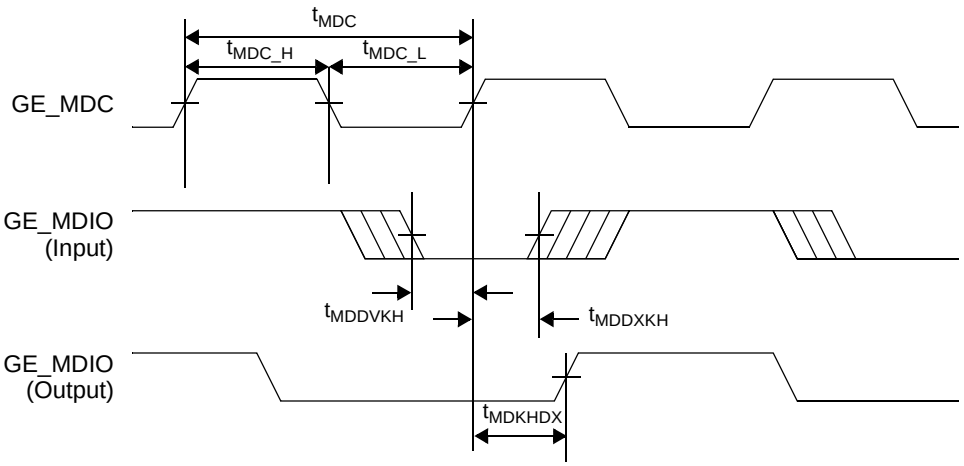

Figure 24. MII Management Interface Timing

3.1.2 Power-On Ramp Time

This section describes the AC electrical specification for the power-on ramp rate requirements for all voltage supplies (including GVDD/SXPVDD/SXCVDD/QVDD/GVDD/NVDD, all VDD supplies, MVREF, and all AVDD supplies). Controlling the power-on ramp time is required to avoid falsely triggering the ESD circuitry. Table 39 defines the power supply ramp time specification.

Table 39. Power Supply Ramp Rate

Parameter	Min	Max	Unit
Required ramp rate.	—	36000	V/s

Notes:
1. Ramp time is specified as a linear ramp from 10% to 90% of nominal voltage of the specific voltage supply. If the ramp is non-linear (for example, exponential), the maximum rate of change from 200 to 500 mV is the most critical because this range might falsely trigger the ESD circuitry.
2. Required over the full recommended operating temperature range (see Table 3).
3. All supplies must be at their stable values within 50 ms.
4. The GVDD pins can be held low on the application board at powerup. If GVDD is not held low, then GVDD will rise to a voltage level that depends on the board-level impedance-to-ground. If the impedance is high (that is, infinite), then theoretically, GVDD can rise up close to the VDD levels.

3.1.3 Power Supply Guidelines

Use the following guidelines for power-up sequencing:

- Couple M3VDD with the VDD power rail using an extremely low impedance path.
- Couple inputs PLL1_AVDD, PLL2_AVDD and PLL3_AVDD with the VDD power rail using an RC filter (see Figure 37).
- There is no dependency in power-on/power-off sequence between the GVDD1, GVDD2, NVDD, and QVDD power rails.
- Couple inputs M1VREF and M2VREF with the GVDD1 and GVDD2 power rails, respectively. They should rise at the same time as or after their respective power rail.
- There is no dependency between RapidIO supplies: SXCVDD1, SXCVDD2, SXPVDD1 and SXPVDD2 and other MSC8152 supplies in the power-on/power-off sequence
- Couple inputs SR1_PLL_AVDD and SR2_PLL_AVDD with SXCVDD1 and SXCVDD2 power rails, respectively, using an RC filter (see Figure 38).

External voltage applied to any input line must not exceed the I/O supply voltage related to this line by more than 0.6 V at any time, including during power-up. Some designs require pull-up voltages applied to selected input lines during power-up for configuration purposes. This is an acceptable exception to the rule during start-up. However, each such input can draw up to 80 mA per input pin per MSC8152 device in the system during power-up. An assertion of the inputs to the high voltage level before power-up should be with slew rate less than 4 V/ns.

The device power rails should rise in the following sequence:

1. VDD (and all coupled supplies)

3.2 PLL Power Supply Design Considerations

Each global PLL power supply must have an external RC filter for the PLLn_AVDD input (see Figure 37) in which the following components are defined as listed:

- R = 5 Ω ± 5%
- C1 = 10 µF ± 10%, 0603, X5R, with ESL ≤ 0.5 nH, low ESL Surface Mount Capacitor.
- C2 = 1.0 µF ± 10%, 0402, X5R, with ESL ≤ 0.5 nH, low ESL Surface Mount Capacitor.

Note: A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change.

All three PLLs can connect to a single supply voltage source (such as a voltage regulator) as long as the external RC filter is applied to each PLL separately. For optimal noise filtering, place the circuit as close as possible to its PLLn_AVDD inputs.

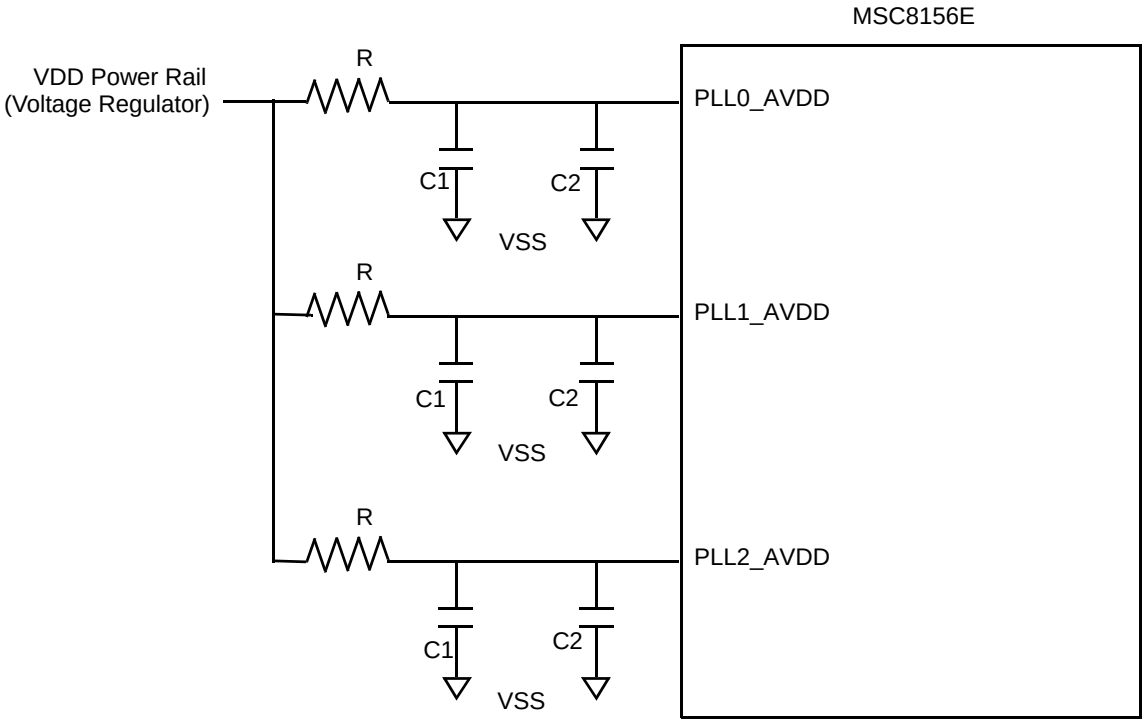

Figure 37. PLL Supplies

Each SerDes PLL power supply must be filtered using a circuit similar to the one shown in Figure 38, to ensure stability of the internal clock. For maximum effectiveness, the filter circuit should be placed as closely as possible to the SRn_PLL_AVDD ball to ensure it filters out as much noise as possible. The ground connection should be near the SRn_PLL_AVDD ball. The 0.003 µF capacitor is closest to the ball, followed by the two 2.2 µF capacitors, and finally the 1 Ω resistor to the board supply plane. The capacitors are connected from SRn_PLL_AVDD to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All trances should be kept short, wide, and direct.

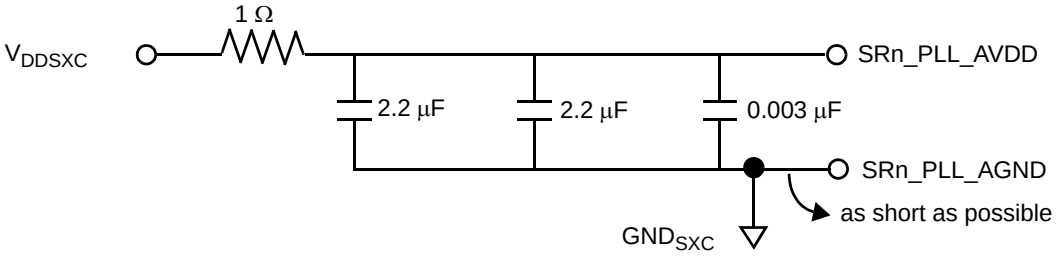

Figure 38. SerDes PLL Supplies

3.5.1 DDR Memory Related Pins

This section discusses the various scenarios that can be used with either of the MSC8152 DDR ports.

Note: The signal names in Table 40, Table 41 and Table 42 are generic names for a DDR SDRAM interface. For actual pin names refer to Table 1.

3.5.1.1 DDR Interface Is Not Used

Table 40. Connectivity of DDR Related Pins When the DDR Interface Is Not Used

Signal Name	Pin Connection
MDQ[0–63]	NC
MDQS[7–0]	NC
$\overline{\text{MDQS[7–0]}}$	NC
MA[15–0]	NC
MCK[0–2]	NC
$\overline{\text{MCK[0–2]}}$	NC
$\overline{\text{MCS[1–0]}}$	NC
MDM[7–0]	NC
MBA[2–0]	NC
$\overline{\text{MCAS}}$	NC
MCKE[1–0]	NC
MODT[1–0]	NC
MMDIC[1–0]	NC
$\overline{\text{MRAS}}$	NC
$\overline{\text{MWE}}$	NC
MECC[7–0]	NC
MDM8	NC
MDQS8	NC
$\overline{\text{MDQS8}}$	NC
MAPAR_OUT	NC
$\overline{\text{MAPAR\_IN}}$	NC
MVREF[3]	NC
GVDD1/GVDD2[3]	NC

Notes:
1. For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is not used.
2. If the DDR controller is not used, disable the internal DDR clock by setting the appropriate bit in the System Clock Control Register (SCCR) and put all DDR I/O in sleep mode by setting DRx_GCR[DDRx_DOZE] (for DDR controller x). See the *Clocks* and *General Configuration Registers* chapters in the ***MSC8152 Reference Manual*** for details.
3. For MSC8152 Revision 1 silicon, these pins were connected to GND. For newer revisions of the MSC8152, connecting these pins to GND increases device power consumption.

3.5.1.2 DDR Interface Is Used With 32-Bit DDR Memory Only

Table 41 lists unused pin connection when using 32-bit DDR memory. The 32 most significant data lines are not used.

Table 41. Connectivity of DDR Related Pins When Using 32-bit DDR Memory Only

Signal Name	Pin Connection
MDQ[31–0]	in use
MDQ[63–32]	NC
MDQS[3–0]	in use
MDQS[7–4]	NC
$\overline{\text{MDQS}}$[3–0]	in use
$\overline{\text{MDQS}}$[7–4]	NC
MA[15–0]	in use
MCK[2–0]	in use
$\overline{\text{MCK}}$[2–0]	in use
$\overline{\text{MCS}}$[1–0]	in use
MDM[3–0]	in use
MDM[7–4]	NC
MBA[2–0]	in use
$\overline{\text{MCAS}}$	in use
MCKE[1–0]	in use
MODT[1–0]	in use
MMDIC[1–0]	in use
$\overline{\text{MRAS}}$	in use
$\overline{\text{MWE}}$	in use
MVREF	in use
GVDD1/GVDD2	in use

Notes:
1. For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is not used.
2. For MSC8152 Revision 1 silicon, these pins were connected to GND (or VDD). For newer revisions of the MSC8152, connecting these pins to GND increases device power consumption.

3.5.1.3 ECC Unused Pin Connections

When the error code correction mechanism is not used in any 32- or 64-bit DDR configuration, refer to Table 42 to determine the correct pin connections.

Table 42. Connectivity of Unused ECC Mechanism Pins

Signal Name	Pin connection
MECC[7–0]	NC
MDM8	NC
MDQS8	NC
$\overline{\text{MDQS8}}$	NC

Notes:
1. For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is not used.
2. For MSC8152 Revision 1 silicon, these pins were connected to GND (or VDD). For newer revisions of the MSC8152, connecting these pins to GND increases device power consumption.

Table 45. Connectivity of HSSI Related Pins When Specific Lane Is Not Used (continued)

Signal Name	Pin Connection
SR[1–2]_RXD***n***	SXCVSS
$\overline{\text{SR[1–2]\_RXD}\textit{n}}$	SXCVSS
$\overline{\text{SR[1–2]\_TXD}\textit{n}}$	NC
SR[1–2]_TXD***n***	NC
SR[1–2]_PLL_AVDD	in use
SR[1–2]_PLL_AGND	in use
SXPVSS	in use
SXCVSS	in use
SXPVDD	in use
SXCVDD	in use
Note: The ***n*** indicates the lane number {0,1,2,3} for all unused lanes.	

3.5.3 RGMII Ethernet Related Pins

Note: Table 46 and Table 47 assume that the alternate function of the specified pin is not used. If the alternate function is used, connect the pin as required to support that function.

Table 46. Connectivity of RGMII Related Pins When the RGMII Interface Is Not Used

Signal Name	Pin Connection
GE1_RX_CTL	GND
GE2_TX_CTL	NC
Note: Assuming GE1 and GE2 are disabled in the reset configuration word.	

GE_MDC and GE_MDIO pins should be connected as required by the specified protocol. If neither GE1 nor GE2 is used, Table 47 lists the recommended management pin connections.

Table 47. Connectivity of GE Management Pins When GE1 and GE2 Are Not Used

Signal Name	Pin Connection
GE_MDC	NC
GE_MDIO	NC

3.5.4 TDM Interface Related Pins

Table 48 lists the board connections of the TDM pins when an entire specific TDM is not used. For multiplexing options that select a subset of a TDM interface, use the connections described in Table 48 for those signals that are not selected. Table 48 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 48. Connectivity of TDM Related Pins When TDM Interface Is Not Used

Signal Name	Pin Connection
TDM***n***RCLK	GND
TDM***n***RDAT	GND
TDM***n***RSYN	GND

Table 48. Connectivity of TDM Related Pins When TDM Interface Is Not Used

Signal Name	Pin Connection
TDM***n***TCLK	GND
TDMT***n***DAT	GND
TDM***n***TSYN	GND
V_{DDIO}	2.5 V

Notes: 1. ***n*** = {0, 1, 2,3}
2. In case of subset of TDM interface usage please make sure to disable unused TDM modules. See *TDM* chapter in the ***MSC8152 Reference Manual*** for details.

3.5.5 Miscellaneous Pins

Table 49 lists the board connections for the pins not required by the system design. Table 49 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 49. Connectivity of Individual Pins When They Are Not Required

Signal Name	Pin Connection
CLKOUT	NC
EE0	GND
EE1	NC
GPIO[31–0]	NC
SCL	See the GPIO connectivity guidelines in this table.
SDA	See the GPIO connectivity guidelines in this table.
$\overline{\text{INT\_OUT}}$	NC
$\overline{\text{IRQ}}$[15–0]	See the GPIO connectivity guidelines in this table.
$\overline{\text{NMI}}$	V_{DDIO}
$\overline{\text{NMI\_OUT}}$	NC
RC[21–0]	GND
STOP_BS	GND
TCK	GND
TDI	GND
TDO	NC
TMR[4–0]	See the GPIO connectivity guidelines in this table.
TMS	GND
$\overline{\text{TRST}}$	See **Section 3.1** for guidelines.
URXD	See the GPIO connectivity guidelines in this table.
UTXD	See the GPIO connectivity guidelines in this table.
DDN[1–0]	See the GPIO connectivity guidelines in this table.
DRQ[1–0]	See the GPIO connectivity guidelines in this table.
$\overline{\text{RCW\_LSEL\_0}}$	GND
$\overline{\text{RCW\_LSEL\_1}}$	GND
$\overline{\text{RCW\_LSEL\_2}}$	GND
$\overline{\text{RCW\_LSEL\_3}}$	GND
V_{DDIO}	2.5 V

Note: For details on configuration, see the *MSC8152 Reference Manual*. For additional information, refer to the *MSC815x and MSC825x DSP Family Design Checklist*.

6 Product Documentation

Following is a general list of supporting documentation:

- *MSC8152 Technical Data Sheet* (MSC8152). Details the signals, AC/DC characteristics, clock signal characteristics, package and pinout, and electrical design considerations of the MSC8152 device.
- *MSC8152 Reference Manual* (MSC8152RM). Includes functional descriptions of the extended cores and all the internal subsystems including configuration and programming information.
- *Application Notes*. Cover various programming topics related to the StarCore DSP core and the MSC8152 device.
- *QUICC Engine Block Reference Manual with Protocol Interworking* (QEIWRM). Provides detailed information regarding the QUICC Engine technology including functional description, registers, and programming information.
- *SC3850 DSP Core Reference Manual*. Covers the SC3850 core architecture, control registers, clock registers, program control, and instruction set.
- *MSC8156SC3850 DSP Core Subsystem Reference Manual*. Covers core subsystem architecture, functionality, and registers.

7 Revision History

Table 50 provides a revision history for this data sheet.

Table 50. Document Revision History

Rev.	Date	Description
0	Jun. 2010	• Initial public release.
1	Dec 2010	• Updated Table 16. • Updated **Section 3.1.2**, *Power-On Ramp Time*.
2	Mar 2011	• Updated Table 8. • Updated Table 15. • Updated Table 17. • Updated Table 33. • Updated Table 35. • Updated Table 39.
3	May 2011	• Updated Table 1. Changed the pin types for the following: – F25 from ground to power. – F26 from power to ground. – T6 from power to O.
4	Oct 2011	• Updated Table 34 and Table 35 to reflect 1 Gbps and 100 Mbps data rate instead of 1 GHz and 100 MHz.
5	Dec 2011	• Added note 4 to Table 39.
6	Aug 2013	• Updated Section 4, “Ordering Information”.