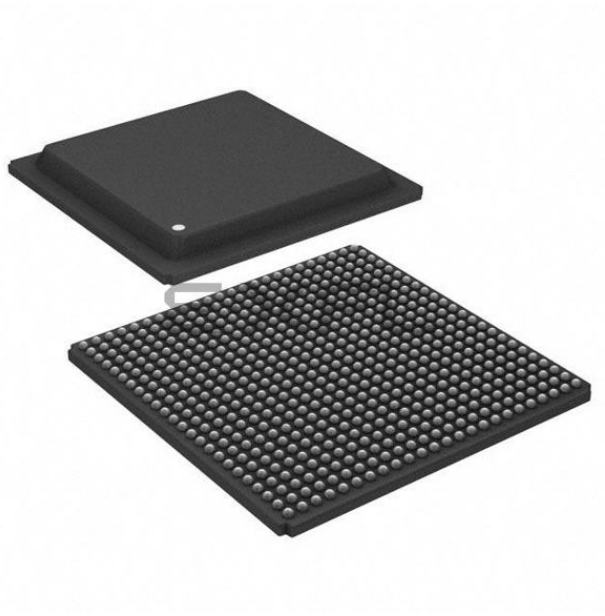

Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed/Floating Point
Interface	Host Interface, Link Port, Multi-Processor
Clock Rate	500MHz
Non-Volatile Memory	External
On-Chip RAM	3MB
Voltage - I/O	2.50V
Voltage - Core	1.05V
Operating Temperature	-40°C ~ 85°C (TC)
Mounting Type	Surface Mount
Package / Case	576-BBGA
Supplier Device Package	576-BGA-ED (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-ts201sabpz050

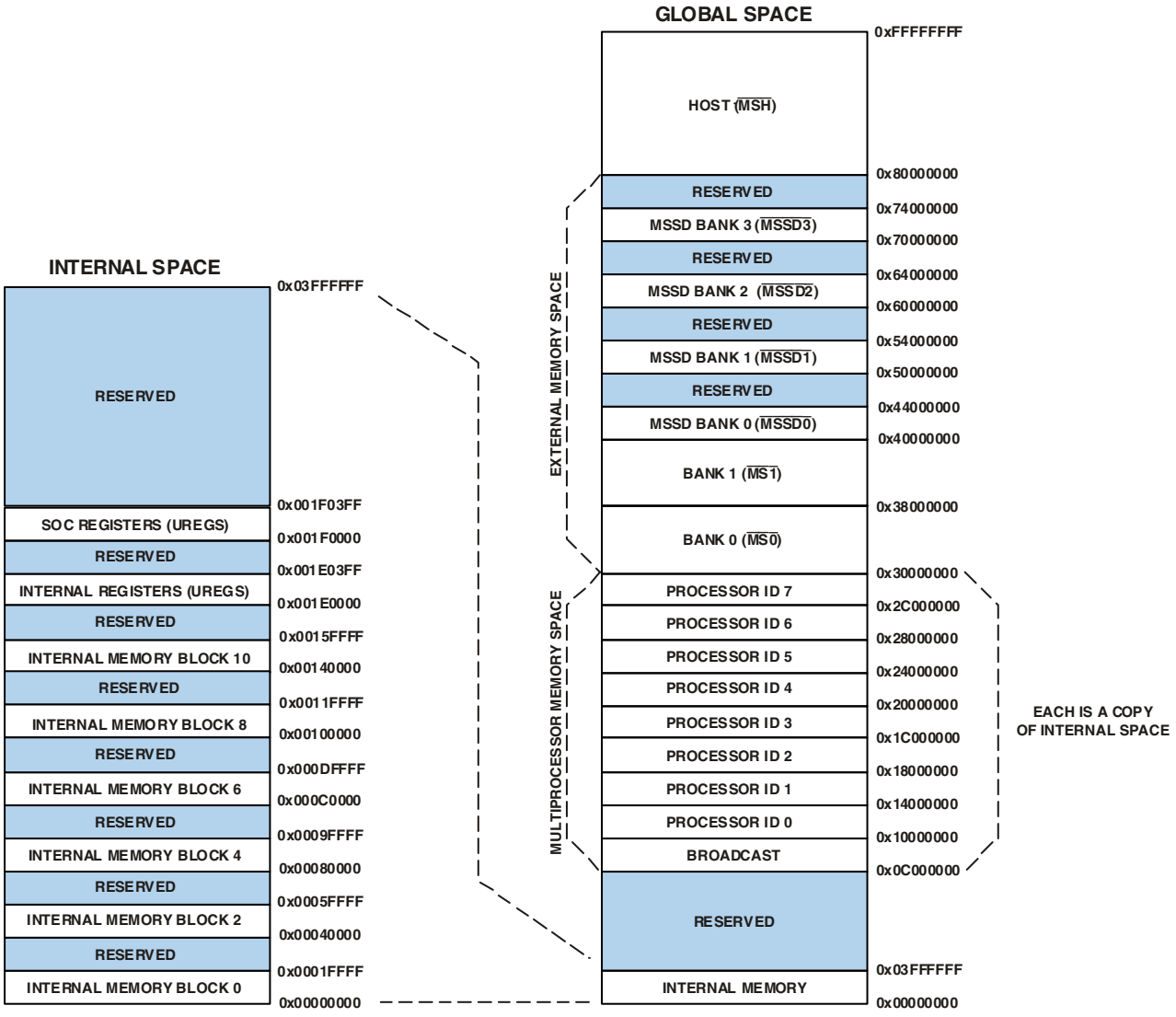

Figure 3. ADSP-TS201S Memory Map

33.6G bytes per second, enabling the core and I/O to access eight 32-bit data-words and four 32-bit instructions each cycle. The DSP's flexible memory structure enables:

- DSP core and I/O accesses to different memory blocks in the same cycle
- DSP core access to three memory blocks in parallel—one instruction and two data accesses
- Programmable partitioning of program and data memory
- Program access of all memory as 32-, 64-, or 128-bit words—16-bit words with the DAB

EXTERNAL PORT (OFF-CHIP MEMORY/PERIPHERALS INTERFACE)

The ADSP-TS201S processor's external port provides the DSP's interface to off-chip memory and peripherals. The 4G word address space is included in the DSP's unified address space.

The separate on-chip buses—four 128-bit data buses and four 32-bit address buses—are multiplexed at the SOC interface and transferred to the external port over the SOC bus to create an external system bus transaction. The external system bus provides a single 64-bit data bus and a single 32-bit address bus. The external port supports data transfer rates of 1G byte per second over the external bus.

The external bus can be configured for 32-bit or 64-bit, little-endian operations. When the system bus is configured for 64-bit operations, the lower 32 bits of the external data bus connect to even addresses, and the upper 32 bits connect to odd addresses.

The external port supports pipelined, slow, and SDRAM protocols. Addressing of external memory devices and memory-mapped peripherals is facilitated by on-chip decoding of high order address lines to generate memory bank select signals.

The ADSP-TS201S processor provides programmable memory, pipeline depth, and idle cycle for synchronous accesses; and external acknowledge controls to support interfacing to pipelined or slow devices, host processors, and other memory-mapped peripherals with variable access, hold, and disable time requirements.

Host Interface

The ADSP-TS201S processor provides an easy and configurable interface between its external bus and host processors through the external port (see Figure 4). To accommodate a variety of host processors, the host interface supports pipelined or slow protocols for ADSP-TS201S processor access of the host as slave or pipelined for host access of the ADSP-TS201S processor as slave. Each protocol has programmable transmission parameters, such as idle cycles, pipe depth, and internal wait cycles.

The host interface supports burst transactions initiated by a host processor. After the host issues the starting address of the burst and asserts the $\overline{\text{BRST}}$ signal, the DSP increments the address internally while the host continues to assert $\overline{\text{BRST}}$.

The host interface provides a deadlock recovery mechanism that enables a host to recover from deadlock situations involving the DSP. The $\overline{\text{BOFF}}$ signal provides the deadlock recovery mechanism. When the host asserts $\overline{\text{BOFF}}$, the DSP backs off the current transaction and asserts $\overline{\text{HBG}}$ and relinquishes the external bus.

The host can directly read or write the internal memory of the ADSP-TS201S processor, and it can access most of the DSP registers, including DMA control (TCB) registers. Vector interrupts support efficient execution of host commands.

Multiprocessor Interface

The ADSP-TS201S processor offers powerful features tailored to multiprocessing DSP systems through the external port and link ports (see Figure 4). This multiprocessing capability provides the highest bandwidth for interprocessor communication, including:

- Up to eight DSPs on a common bus
- On-chip arbitration for glueless multiprocessing
- Link ports for point-to-point communication

The external port and link ports provide integrated, glueless multiprocessing support.

The external port supports a unified address space (see Figure 3) that enables direct interprocessor accesses of each ADSP-TS201S processor's internal memory and registers. The DSP's on-chip distributed bus arbitration logic provides simple, glueless connection for systems containing up to eight ADSP-TS201S processors and a host processor. Bus arbitration has a rotating priority. Bus lock supports indivisible read-modify-write sequences for semaphores. A bus fairness feature prevents one DSP from holding the external bus too long.

The DSP's four link ports provide a second path for interprocessor communications with throughput of 4G bytes per second. The cluster bus provides 1G byte per second throughput—with a total of 4.8G bytes per second interprocessor bandwidth (limited by SOC bandwidth).

SDRAM Controller

The SDRAM controller controls the ADSP-TS201S processor's transfers of data to and from external synchronous DRAM (SDRAM) at a throughput of 32 bits or 64 bits per SCLK cycle using the external port and SDRAM control pins.

The SDRAM interface provides a glueless interface with standard SDRAMs—16M bit, 64M bit, 128M bit, 256M bit, and 512M bit. The DSP supports directly a maximum of four banks of 64M words × 32 bits of SDRAM. The SDRAM interface is mapped in external memory in each DSP's unified memory map.

EPROM Interface

The ADSP-TS201S processor can be configured to boot from an external 8-bit EPROM at reset through the external port. An automatic process (which follows reset) loads a program from the EPROM into internal memory. This process uses 16 wait cycles for each read access. During booting, the $\overline{\text{BMS}}$ pin functions as the EPROM chip select signal. The EPROM boot procedure uses DMA Channel 0, which packs the bytes into 32-bit instructions. Applications can also access the EPROM (write flash memories) during normal operation through DMA.

The EPROM or flash memory interface is not mapped in the DSP's unified memory map. It is a byte address space limited to a maximum of 16M bytes (24 address bits). The EPROM or flash memory interface can be used after boot via a DMA.

DMA CONTROLLER

The ADSP-TS201S processor's on-chip DMA controller, with 14 DMA channels, provides zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to the DSP's core, enabling DMA operations to occur while the DSP's core continues to execute program instructions.

The DMA controller performs DMA transfers between internal memory, external memory, and memory-mapped peripherals; the internal memory of other DSPs on a common bus, a host processor, or link port I/O; between external memory and external peripherals or link port I/O; and between an external bus master and internal memory or link port I/O. The DMA controller performs the following DMA operations:

- External port block transfers. Four dedicated bidirectional DMA channels transfer blocks of data between the DSP's internal memory and any external memory or memory-mapped peripheral on the external bus. These transfers support master mode and handshake mode protocols.
- Link port transfers. Eight dedicated DMA channels (four transmit and four receive) transfer quad-word data only between link ports and between a link port and internal or

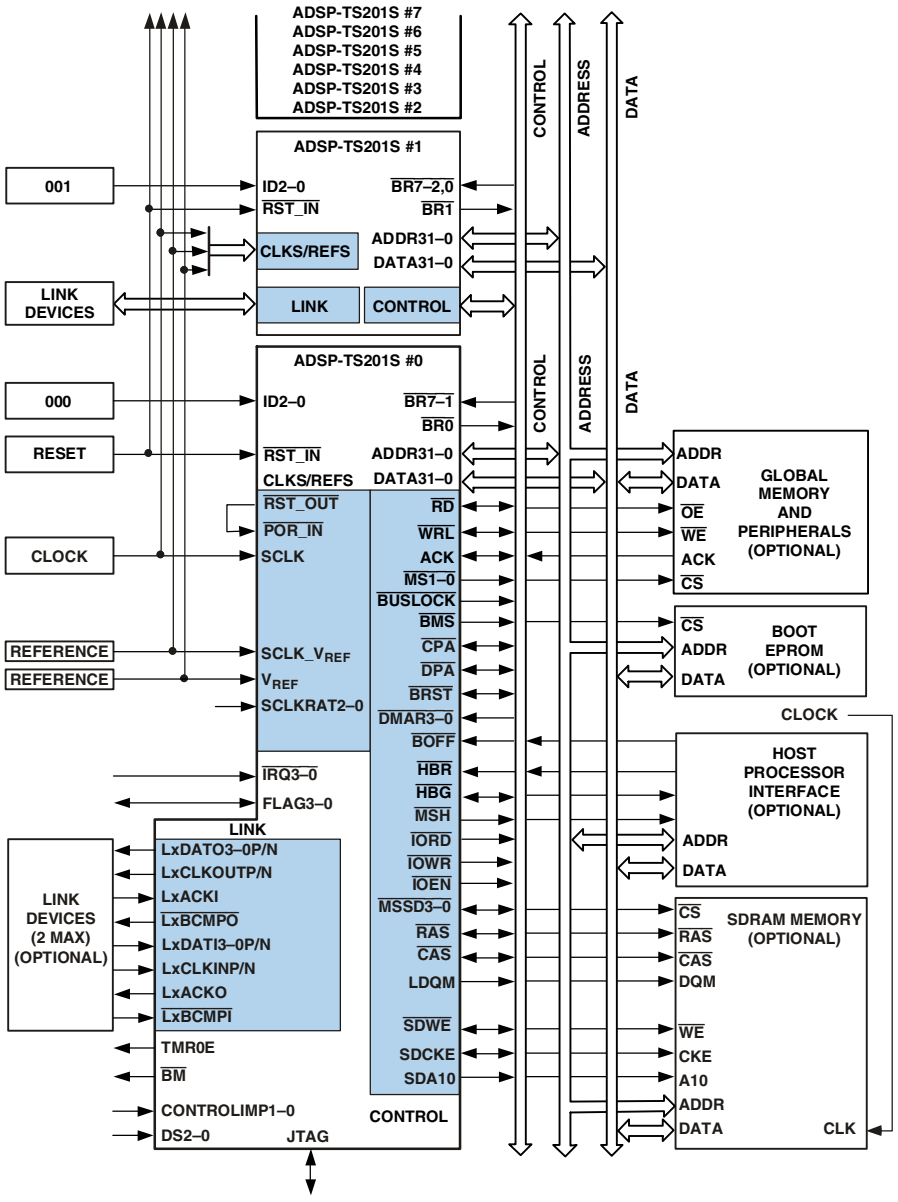

Figure 4. ADSP-TS201S Shared Memory Multiprocessing System

external memory. These transfers only use handshake mode protocol. DMA priority rotates between the four receive channels.

- AutoDMA transfers. Two dedicated unidirectional DMA channels transfer data received from an external bus master to internal memory or to link port I/O. These transfers only use slave mode protocol, and an external bus master must initiate the transfer.

The DMA controller provides these additional features:

- Flyby transfers. Flyby operations only occur through the external port (DMA Channel 0) and do not involve the DSP's core. The DMA controller acts as a conduit to transfer data from an I/O device to external SDRAM memory. During a transaction, the DSP relinquishes the external data bus; outputs addresses and memory selects ($\overline{\text{MSSD3–0}}$); outputs the $\overline{\text{IORD}}$, $\overline{\text{IOWR}}$, $\overline{\text{IOEN}}$, and $\overline{\text{RD}}/\overline{\text{WR}}$ strobes; and responds to ACK.
- DMA chaining. DMA chaining operations enable applications to automatically link one DMA transfer sequence to another for continuous transmission. The sequences can occur over different DMA channels and have different transmission attributes.
- Two-dimensional transfers. The DMA controller can access and transfer two-dimensional memory arrays on any DMA transmit or receive channel. These transfers are implemented with index, count, and modify registers for both the X and Y dimensions.

LINK PORTS (LVDS)

The DSP's four full-duplex link ports each provide additional four-bit receive and four-bit transmit I/O capability, using low voltage, differential-signal (LVDS) technology. With the ability to operate at a double data rate—latching data on both the rising and falling edges of the clock—running at up to 500 MHz, each link port can support up to 500M bytes per second per direction, for a combined maximum throughput of 4G bytes per second.

The link ports provide an optional communications channel that is useful in multiprocessor systems for implementing point-to-point interprocessor communications. Applications can also use the link ports for booting.

Each link port has its own triple-buffered quad-word input and double-buffered quad-word output registers. The DSP's core can write directly to a link port's transmit register and read from a receive register, or the DMA controller can perform DMA transfers through eight (four transmit and four receive) dedicated link port DMA channels.

Each link port direction has three signals that control its operation. For the transmitter, LxCLKOUT is the output transmit clock, LxACKI is the handshake input to control the data flow, and the $\overline{\text{LxBCMPO}}$ output indicates that the block transfer is complete. For the receiver, LxCLKIN is the input receive clock, LxACKO is the handshake output to control the data flow, and the $\overline{\text{LxBCMPI}}$ input indicates that the block transfer is complete. The LxDATO3–0 pins are the data output bus for the transmitter and the LxDATI3–0 pins are the input data bus for the receiver.

Applications can program separate error detection mechanisms for transmit and receive operations (applications can use the checksum mechanism to implement consecutive link port transfers), the size of data packets, and the speed at which bytes are transmitted.

TIMER AND GENERAL-PURPOSE I/O

The ADSP-TS201S processor has a timer pin (TMR0E) that generates output when a programmed timer counter has expired, and four programmable general-purpose I/O pins (FLAG3–0) that can function as either single-bit input or output. As outputs, these pins can signal peripheral devices; as inputs, they can provide the test for conditional branching.

RESET AND BOOTING

The ADSP-TS201S processor has three levels of reset:

- Power-up reset – after power-up of the system (SCLK, all static inputs, and strap pins are stable), the $\overline{\text{RST\_IN}}$ pin must be asserted (low).
- Normal reset – for any chip reset following the power-up reset, the $\overline{\text{RST\_IN}}$ pin must be asserted (low).
- DSP-core reset – when setting the SWRST bit in EMUCTL, the DSP core is reset, but not the external port or I/O.

For normal operations, tie the $\overline{\text{RST\_OUT}}$ pin to the $\overline{\text{POR\_IN}}$ pin.

After reset, the ADSP-TS201S processor has four boot options for beginning operation:

- Boot from EPROM.
- Boot by an external master (host or another ADSP-TS201S processor).
- Boot by link port.
- No boot—start running from memory address selected with one of the $\overline{\text{IRQ3–0}}$ interrupt signals. See Table 2.

Using the "no boot" option, the ADSP-TS201S processor must start running from memory when one of the interrupts is asserted.

Table 2. No Boot, Run from Memory Addresses

Interrupt	Address
$\overline{\text{IRQ0}}$	0x3000 0000 (External Memory)
$\overline{\text{IRQ1}}$	0x3800 0000 (External Memory)
$\overline{\text{IRQ2}}$	0x8000 0000 (External Memory)
$\overline{\text{IRQ3}}$	0x0000 0000 (Internal Memory)

The ADSP-TS201S processor core always exits from reset in the idle state and waits for an interrupt. Some of the interrupts in the interrupt vector table are initialized and enabled after reset.

For more information on boot options, see the *EE-200: ADSP-TS20x TigerSHARC Processor Boot Loader Kernels Operation* on the Analog Devices website (www.analog.com).

CLOCK DOMAINS

The DSP uses calculated ratios of the SCLK clock to operate, as shown in Figure 5. The instruction execution rate is equal to CCLK. A PLL from SCLK generates CCLK which is phase-locked. The SCLKRATx pins define the clock multiplication of SCLK to CCLK (see Table 4 on Page 12). The link port clock is generated from CCLK via a software programmable divisor, and the SOC bus operates at 1/2 CCLK. Memory transfers to external and link port buffers operate at the SOCCLK rate. SCLK also provides clock input for the external bus interface and defines the ac specification reference for the external bus signals. The external bus interface runs at the SCLK frequency. The maximum SCLK frequency is one quarter the internal DSP clock (CCLK) frequency.

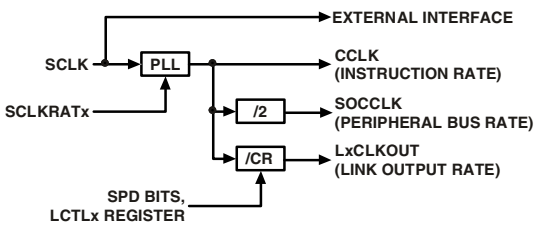

Figure 5. Clock Domains

PIN FUNCTION DESCRIPTIONS

While most of the ADSP-TS201S processor's input pins are normally synchronous—tied to a specific clock—a few are asynchronous. For these asynchronous signals, an on-chip synchronization circuit prevents metastability problems. Use the ac specification for asynchronous signals when the system design requires predictable, cycle-by-cycle behavior for these signals.

The output pins can be three-stated during normal operation. The DSP three-states all output pins during reset, allowing these pins to get to their internal pull-up or pull-down state. Some pins have an internal pull-up or pull-down resistor (±30% tolerance) that maintains a known value during transitions between different drivers.

Table 3. Pin Definitions—Clocks and Reset

Signal	Type	Term	Description
SCLKRAT2–0	I (pd)	na	Core Clock Ratio. The DSP's core clock (CCLK) rate = n × SCLK, where n is user-programmable using the SCLKRATx pins to the values shown in Table 4. These pins may change only during reset; connect these pins to V_{DD_IO} or V_{SS}. All reset specifications in Table 25, Table 26, and Table 27 must be satisfied. The core clock rate (CCLK) is the instruction cycle rate.
SCLK	I	na	System Clock Input. The DSP's system input clock for cluster bus. The core clock rate is user-programmable using the SCLKRATx pins. For more information, see Clock Domains on Page 9.
$\overline{\text{RST\_IN}}$	I/A	na	Reset. Sets the DSP to a known state and causes program to be in idle state. $\overline{\text{RST\_IN}}$ must be asserted a specified time according to the type of reset operation. For details, see Reset and Booting on Page 9, Table 25 on Page 26, and Figure 13 on Page 26.
$\overline{\text{RST\_OUT}}$	O	na	Reset Output. Indicates that the DSP reset is complete. Connect to $\overline{\text{POR\_IN}}$.
$\overline{\text{POR\_IN}}$	I/A	na	Power-On Reset for internal DRAM. Connect to $\overline{\text{RST\_OUT}}$.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on DSP ID = 0; **pu_0** = internal pull-up 5 kΩ on DSP ID = 0; **pu_od_0** = internal pull-up 500 Ω on DSP ID = 0; **pd_m** = internal pull-down 5 kΩ on DSP bus master; **pu_m** = internal pull-up 5 kΩ on DSP bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 22.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

Table 4. SCLK Ratio

SCLKRAT2–0	Ratio
000 (default)	4
001	5
010	6
011	7
100	8
101	10
110	12
111	Reserved

Table 7. Pin Definitions—External Port DMA/Flyby

Signal	Type	Term	Description
$\overline{\text{DMAR3–0}}$	I/A	epu	DMA Request Pins. Enable external I/O devices to request DMA services from the DSP. In response to $\overline{\text{DMARx}}$, the DSP performs DMA transfers according to the DMA channel's initialization. The DSP ignores DMA requests from uninitialized channels.
$\overline{\text{IOWR}}$	O/T (pu_0)	nc	I/O Write. When a DSP DMA channel initiates a flyby mode read transaction, the DSP asserts the $\overline{\text{IOWR}}$ signal during the data cycles. This assertion makes the I/O device sample the data instead of the TigerSHARC.
$\overline{\text{IORD}}$	O/T (pu_0)	nc	I/O Read. When a DSP DMA channel initiates a flyby mode write transaction, the DSP asserts the $\overline{\text{IORD}}$ signal during the data cycle. This assertion with the $\overline{\text{IOEN}}$ makes the I/O device drive the data instead of the TigerSHARC.
$\overline{\text{IOEN}}$	O/T (pu_0)	nc	I/O Device Output Enable. Enables the output buffers of an external I/O device for flyby transactions between the device and external memory. Active on flyby transactions.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on DSP ID = 0; **pu_0** = internal pull-up 5 kΩ on DSP ID = 0; **pu_od_0** = internal pull-up 500 Ω on DSP ID = 0; **pd_m** = internal pull-down 5 kΩ on DSP bus master; **pu_m** = internal pull-up 5 kΩ on DSP bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 22.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

Table 8. Pin Definitions—External Port SDRAM Controller

Signal	Type	Term	Description
$\overline{\text{MSSD3–0}}$	I/O/T (pu_0)	nc	Memory Select SDRAM. $\overline{\text{MSSD0}}$, $\overline{\text{MSSD1}}$, $\overline{\text{MSSD2}}$, or $\overline{\text{MSSD3}}$ is asserted whenever the DSP accesses SDRAM memory space. $\overline{\text{MSSD3–0}}$ are decoded memory address pins that are asserted whenever the DSP issues an SDRAM command cycle (access to ADDR31:30 = 0b01—except reserved spaces shown in Figure 3 on Page 6). In a multiprocessor system, the master DSP drives $\overline{\text{MSSD3–0}}$.
$\overline{\text{RAS}}$	I/O/T (pu_0)	nc	Row Address Select. When sampled low, $\overline{\text{RAS}}$ indicates that a row address is valid in a read or write of SDRAM. In other SDRAM accesses, it defines the type of operation to execute according to SDRAM specification.
$\overline{\text{CAS}}$	I/O/T (pu_0)	nc	Column Address Select. When sampled low, $\overline{\text{CAS}}$ indicates that a column address is valid in a read or write of SDRAM. In other SDRAM accesses, it defines the type of operation to execute according to the SDRAM specification.
LDQM	O/T (pu_0)	nc	Low Word SDRAM Data Mask. When sampled high, three-states the SDRAM DQ buffers. LDQM is valid on SDRAM transactions when $\overline{\text{CAS}}$ is asserted, and inactive on read transactions. On write transactions, LDQM is active when accessing an odd address word on a 64-bit memory bus to disable the write of the low word.
HDQM	O/T (pu_0)	nc	High Word SDRAM Data Mask. When sampled high, three-states the SDRAM DQ buffers. HDQM is valid on SDRAM transactions when $\overline{\text{CAS}}$ is asserted, and inactive on read transactions. On write transactions, HDQM is active when accessing an even address in word accesses or when memory is configured for a 32-bit bus to disable the write of the high word.
SDA10	O/T (pu_0)	nc	SDRAM Address Bit 10. Separate A10 signals enable SDRAM refresh operation while the DSP executes non-SDRAM transactions.
SDCKE	I/O/T (pu_m/ pd_m)	nc	SDRAM Clock Enable. Activates the SDRAM clock for SDRAM self-refresh or suspend modes. A slave DSP in a multiprocessor system does not have the pull-up or pull-down. A master DSP (or ID = 0 in a single processor system) has a pull-up before granting the bus to the host, except when the SDRAM is put in self refresh mode. In self refresh mode, the master has a pull-down before granting the bus to the host.
$\overline{\text{SDWE}}$	I/O/T (pu_0)	nc	SDRAM Write Enable. When sampled low while $\overline{\text{CAS}}$ is active, $\overline{\text{SDWE}}$ indicates an SDRAM write access. When sampled high while $\overline{\text{CAS}}$ is active, $\overline{\text{SDWE}}$ indicates an SDRAM read access. In other SDRAM accesses, $\overline{\text{SDWE}}$ defines the type of operation to execute according to SDRAM specification.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on DSP ID = 0; **pu_0** = internal pull-up 5 kΩ on DSP ID = 0; **pu_od_0** = internal pull-up 500 Ω on DSP ID = 0; **pd_m** = internal pull-down 5 kΩ on DSP bus master; **pu_m** = internal pull-up 5 kΩ on DSP bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 22.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

Table 9. Pin Definitions—JTAG Port

Signal	Type	Term	Description
$\overline{\text{EMU}}$	O/OD	nc[1]	Emulation. Connected to the DSP's JTAG emulator target board connector only.
TCK	I	epd or epu[1]	Test Clock (JTAG). Provides an asynchronous clock for JTAG scan.
TDI	I (pu_ad)	nc[1]	Test Data Input (JTAG). A serial data input of the scan path.
TDO	O/T	nc[1]	Test Data Output (JTAG). A serial data output of the scan path.
TMS	I (pu_ad)	nc[1]	Test Mode Select (JTAG). Used to control the test state machine.
$\overline{\text{TRST}}$	I/A (pu_ad)	na	Test Reset (JTAG). Resets the test state machine. $\overline{\text{TRST}}$ must be asserted or pulsed low after power up for proper device operation. For more information, see Reset and Booting on Page 9.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on DSP ID = 0; **pu_0** = internal pull-up 5 kΩ on DSP ID = 0; **pu_od_0** = internal pull-up 500 Ω on DSP ID = 0; **pd_m** = internal pull-down 5 kΩ on DSP bus master; **pu_m** = internal pull-up 5 kΩ on DSP bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 22.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

[1] See the reference on Page 11 to the JTAG emulation technical reference EE-68.

Table 10. Pin Definitions—Flags, Interrupts, and Timer

Signal	Type	Term	Description
FLAG3–0	I/O/A (pu)	nc	FLAG pins. Bidirectional input/output pins can be used as program conditions. Each pin can be configured individually for input or for output. FLAG3–0 are inputs after power-up and reset.
$\overline{\text{IRQ3–0}}$	I/A (pu)	nc	Interrupt Request. When asserted, the DSP generates an interrupt. Each of the $\overline{\text{IRQ3–0}}$ pins can be independently set for edge-triggered or level-sensitive operation. After reset, these pins are disabled unless the $\overline{\text{IRQ3–0}}$ strap option and interrupt vectors are initialized for booting.
TMR0E	O	na	Timer 0 expires. This output pulses whenever timer 0 expires. At reset, this is a strap pin. For more information, see Table 16 on Page 20.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on DSP ID = 0; **pu_0** = internal pull-up 5 kΩ on DSP ID = 0; **pu_od_0** = internal pull-up 500 Ω on DSP ID = 0; **pd_m** = internal pull-down 5 kΩ on DSP bus master; **pu_m** = internal pull-up 5 kΩ on DSP bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 22.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

STRAP PIN FUNCTION DESCRIPTIONS

Some pins have alternate functions at reset. Strap options set DSP operating modes. During reset, the DSP samples the strap option pins. Strap pins have an internal pull-up or pull-down for the default value. If a strap pin is not connected to an overdriving external pull-up, pull-down, or logic load, the DSP samples the default value during reset. If strap pins are connected to logic inputs, a stronger external pull-up or pull-down may be required to ensure default value depending on leakage and/or low level input current of the logic load. To set a mode other than the default mode, connect the strap pin to a sufficiently stronger external pull-up or pull-down. Table 16 lists and describes each of the DSP's strap pins.

Table 16. Pin Definitions—I/O Strap Pins

Signal	Type (at Reset)	On Pin …	Description
EBOOT	I (pd_0)	$\overline{\text{BMS}}$	EPROM Boot. 0 = boot from EPROM immediately after reset (default) 1 = idle after reset and wait for an external device to boot DSP through the external port or a link port
IRQEN	I (pd)	$\overline{\text{BM}}$	Interrupt Enable. 0 = disable and set $\overline{\text{IRQ3–0}}$ interrupts to edge-sensitive after reset (default) 1 = enable and set $\overline{\text{IRQ3–0}}$ interrupts to level-sensitive immediately after reset
LINK_DWIDTH	I (pd)	TMR0E	Link Port Input Default Data Width. 0 = 1-bit (default) 1 = 4-bit
SYS_REG_WE	I (pd_0)	$\overline{\text{BUSLOCK}}$	SYSCON and SDRCON Write Enable. 0 = one-time writable after reset (default) 1 = always writable
TM1	I (pu)	$\overline{\text{L1BCMPO}}$	Test Mode 1. Do not overdrive default value during reset.
TM2	I (pu)	$\overline{\text{L2BCMPO}}$	Test Mode 2. Do not overdrive default value during reset.
TM3	I (pu)	$\overline{\text{L3BCMPO}}$	Test Mode 3. Do not overdrive default value during reset.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on DSP ID = 0; **pu_0** = internal pull-up 5 kΩ on DSP ID = 0; **pu_od_0** = internal pull-up 500 Ω on DSP ID = 0; **pd_m** = internal pull-down 5 kΩ on DSP bus master; **pu_m** = internal pull-up 5 kΩ on DSP bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 22.

When default configuration is used, no external resistor is needed on the strap pins. To apply other configurations, a 500 Ω resistor connected to V_{DD_IO} is required. If providing external pull-downs, do not strap these pins directly to V_{SS}; the strap pins require 500 Ω resistor straps.

All strap pins are sampled on the rising edge of $\overline{\text{RST\_IN}}$ (deassertion edge). Each pin latches the strapped pin state (state of the strap pin at the rising edge of $\overline{\text{RST\_IN}}$). Shortly after deassertion of $\overline{\text{RST\_IN}}$, these pins are reconfigured to their normal functionality.

These strap pins have an internal pull-down resistor, pull-up resistor, or no-resistor (three-state) on each pin. The resistor type, which is connected to the I/O pad, depends on whether $\overline{\text{RST\_IN}}$ is active (low) or if $\overline{\text{RST\_IN}}$ is deasserted (high). Table 17 shows the resistors that are enabled during active reset and during normal operation.

Table 17. Strap Pin Internal Resistors—Active Reset ($\overline{\text{RST\_IN}}$ = 0) vs. Normal Operation ($\overline{\text{RST\_IN}}$ = 1)

Pin	$\overline{\text{RST\_IN}}$ = 0	$\overline{\text{RST\_IN}}$ = 1
$\overline{\text{BMS}}$	(pd_0)	(pu_0)
$\overline{\text{BM}}$	(pd)	Driven
TMR0E	(pd)	Driven
$\overline{\text{BUSLOCK}}$	(pd_0)	(pu_0)
$\overline{\text{L1BCMPO}}$	(pu)	Driven
$\overline{\text{L2BCMPO}}$	(pu)	Driven
$\overline{\text{L3BCMPO}}$	(pu)	Driven

pd = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ;
pd_0 = internal pull-down 5 kΩ on DSP ID = 0;
pu_0 = internal pull-up 5 kΩ on DSP ID = 0

Table 18. Maximum Duty Cycle for Input Transient Voltage

V_{IN} Max (V)[1]	V_{IN} Min (V)[1]	Maximum Duty Cycle[2]
+3.63	–0.33	100%
+3.64	–0.34	90%
+3.70	–0.40	50%
+3.78	–0.48	30%
+3.86	–0.56	17%
+3.93	–0.63	10%

[1] The individual values cannot be combined for analysis of a single instance of overshoot or undershoot. The worst case observed value must fall within one of the voltages specified and the total duration of the overshoot or undershoot (exceeding the 100% case) must be less than or equal to the corresponding duty cycle.

[2] Duty cycle refers to the percentage of time the signal exceeds the value for the 100% case. This is equivalent to the measured duration of a single instance of overshoot or undershoot as a percentage of the period of occurrence. The practical worst case for period of occurrence for either overshoot or undershoot is $2 \times t_{SCLK}$.

ELECTRICAL CHARACTERISTICS

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH}	High Level Output Voltage[1]	@V_{DD_IO} = Min, I_{OH} = –2 mA	2.18		V
V_{OL}	Low Level Output Voltage[1]	@V_{DD_IO} = Min, I_{OL} = 4 mA		0.4	V
I_{IH}	High Level Input Current	@V_{DD_IO} = Max, V_{IN} = V_{IH} Max		20	µA
I_{IH_PU}	High Level Input Current	@V_{DD_IO} = Max, V_{IN} = V_{IH} Max		20	µA
I_{IH_PD}	High Level Input Current	@V_{DD_IO} = Max, V_{IN} = V_{DD_IO} Max	0.3	0.76	mA
$I_{IH\_PD\_L}$	High Level Input Current	@V_{DD_IO} = Max, V_{IN} = V_{IH} Max	30	76	µA
I_{IL}	Low Level Input Current	@V_{DD_IO} = Max, V_{IN} = 0 V		20	µA
I_{IL_PU}	Low Level Input Current	@V_{DD_IO} = Max, V_{IN} = 0 V	0.3	0.76	mA
$I_{IL\_PU\_AD}$	Low Level Input Current	@V_{DD_IO} = Max, V_{IN} = 0 V	30	100	µA
I_{OZH}	Three-State Leakage Current High	@V_{DD_IO} = Max, V_{IN} = V_{IH} Max		50	µA
I_{OZH_PD}	Three-State Leakage Current High	@V_{DD_IO} = Max, V_{IN} = V_{DD_IO} Max	0.3	0.76	mA
I_{OZL}	Three-State Leakage Current Low	@V_{DD_IO} = Max, V_{IN} = 0 V		20	µA
I_{OZL_PU}	Three-State Leakage Current Low	@V_{DD_IO} = Max, V_{IN} = 0 V	0.3	0.76	mA
$I_{OZL\_PU\_AD}$	Three-State Leakage Current Low	@V_{DD_IO} = Max, V_{IN} = 0 V	30	100	µA
I_{OZL_OD}	Three-State Leakage Current Low	@V_{DD_IO} = Max, V_{IN} = 0 V	4	7.6	mA
C_{IN}	Input Capacitance[2, 3]	@f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		3	pF

Parameter name suffix conventions: no suffix = applies to pins without pull-up or pull-down resistors, **_PD** = applies to pin types (pd) or (pd_0), **_PU** = applies to pin types (pu) or (pu_0), **_PU_AD** = applies to pin types (pu_ad), **_OD** = applies to pin types OD, **_PD_L** = applies to pin types (pd_l)

[1] Applies to output and bidirectional pins.

[2] Applies to all signals.

[3] Guaranteed but not tested.

Table 23. Reference Clocks—System Clock (SCLK) Cycle Time

Parameter	Description	SCLKRAT = 4×, 6×, 8×, 10×, 12×		SCLKRAT = 5×, 7×		Unit
		Min	Max	Min	Max	
t_{SCLK}[1, 2, 3]	System Clock Cycle Time	8	50	8	50	ns
t_{SCLKH}	System Clock Cycle High Time	0.40 × t_{SCLK}	0.60 × t_{SCLK}	0.45 × t_{SCLK}	0.55 × t_{SCLK}	ns
t_{SCLKL}	System Clock Cycle Low Time	0.40 × t_{SCLK}	0.60 × t_{SCLK}	0.45 × t_{SCLK}	0.55 × t_{SCLK}	ns
t_{SCLKF}	System Clock Transition Time—Falling Edge[4]	—	1.5	—	1.5	ns
t_{SCLKR}	System Clock Transition Time—Rising Edge	—	1.5	—	1.5	ns
t_{SCLKJ}[5, 6]	System Clock Jitter Tolerance	—	500	—	500	ps

[1] For more information, see Table 3 on Page 12.
[2] For more information, see Clock Domains on Page 9.
[3] The value of (t_{SCLK} / SCLKRAT2-0) must not violate the specification for t_{CCLK}.
[4] System clock transition times apply to minimum SCLK cycle time (t_{SCLK}) only.
[5] Actual input jitter should be combined with ac specifications for accurate timing analysis.
[6] Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

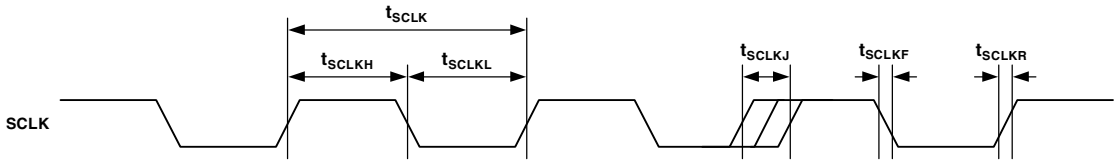

Figure 10. Reference Clocks—System Clock (SCLK) Cycle Time

Table 24. Reference Clocks—JTAG Test Clock (TCK) Cycle Time

Parameter	Description	Min	Max	Unit
t_{TCK}	Test Clock (JTAG) Cycle Time	Greater of 30 or t_{CCLK} × 4	—	ns
t_{TCKH}	Test Clock (JTAG) Cycle High Time	12	—	ns
t_{TCKL}	Test Clock (JTAG) Cycle Low Time	12	—	ns

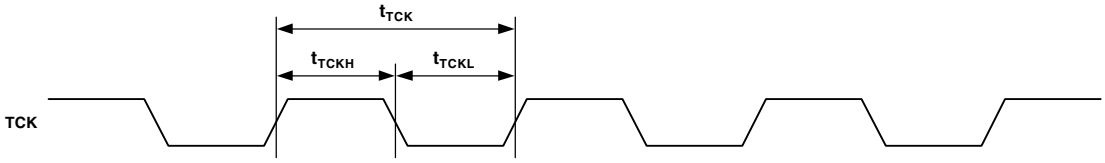

Figure 11. Reference Clocks—JTAG Test Clock (TCK) Cycle Time

Table 27. Normal Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{RST_IN}	$\overline{RST\_IN}$ Asserted	2		ms
t_{STRAP}	$\overline{RST\_IN}$ Deasserted After Strap Pins Stable	1.5		ms
Switching Characteristic				
t_{RST_OUT}	$\overline{RST\_OUT}$ Deasserted After $\overline{RST\_IN}$ Deasserted	1.5		ms

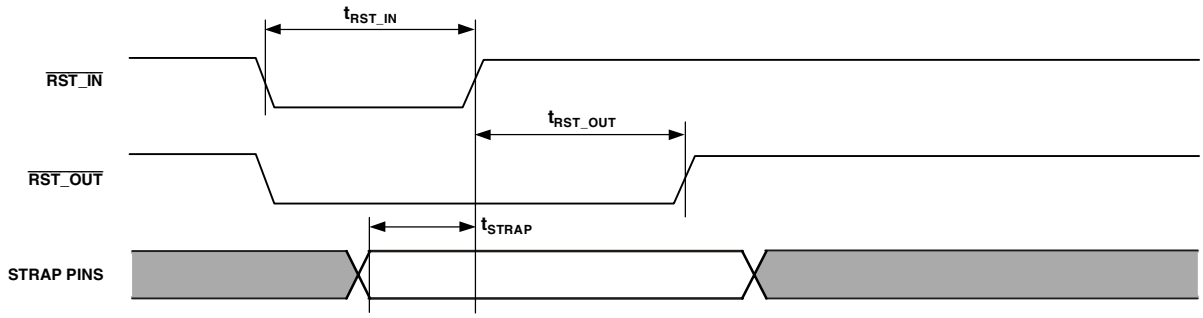

Figure 14. Normal Reset Timing

Table 28. On-Chip DRAM Refresh[1]

Parameter		Min	Max	Unit
Timing Requirement				
t_{REF}	On-chip DRAM Refresh Period		1.56	µs

[1] For more information on setting the refresh rate for the on-chip DRAM, refer to the *ADSP-TS201 TigerSHARC Processor Programming Reference.*

Table 29. AC Signal Specifications

(All values in this table are in nanoseconds.)

Name	Description	Input Setup (Min)	Input Hold (Min)	Output Valid (Max)	Output Hold (Min)	Output Enable (Min)[1]	Output Disable (Max)[1]	Reference Clock
ADDR31–0	External Address Bus	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
DATA63–0	External Data Bus	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{MSH}}$	Memory Select HOST Line	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{MSSD3–0}}$	Memory Select SDRAM Lines	1.5	0.5	4.0	1.0	1.0	2.0	SCLK
$\overline{\text{MS1–0}}$	Memory Select for Static Blocks	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{RD}}$	Memory Read	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{WRL}}$	Write Low Word	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{WRH}}$	Write High Word	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
ACK	Acknowledge for Data High to Low	1.5	0.5	3.6	1.0	1.15	2.0	SCLK
	Acknowledge for Data Low to High	1.5	0.5	4.2	0.9	1.15	2.0	SCLK
SDCKE	SDRAM Clock Enable	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{RAS}}$	Row Address Select	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{CAS}}$	Column Address Select	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{SDWE}}$	SDRAM Write Enable	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
LDQM	Low Word SDRAM Data Mask	—	—	4.0	1.0	1.15	2.0	SCLK
HDQM	High Word SDRAM Data Mask	—	—	4.0	1.0	1.15	2.0	SCLK
SDA10	SDRAM ADDR10	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{HBR}}$	Host Bus Request	1.5	0.5	—	—	—	—	SCLK
$\overline{\text{HBG}}$	Host Bus Grant	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{BOFF}}$	Back Off Request	1.5	0.5	—	—	—	—	SCLK
$\overline{\text{BUSLOCK}}$	Bus Lock	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{BRST}}$	Burst Pin	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{BR7–0}}$	Multiprocessing Bus Request Pins	1.5	0.5	4.0	1.0	—	—	SCLK
$\overline{\text{BM}}$	Bus Master Debug Aid Only	—	—	4.0	1.0	—	—	SCLK
$\overline{\text{IORD}}$	I/O Read Pin	—	—	4.0	1.0	1.0	2.0	SCLK
$\overline{\text{IOWR}}$	I/O Write Pin	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{IOEN}}$	I/O Enable Pin	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{CPA}}$	Core Priority Access High to Low	1.5	0.5	4.0	1.0	0.75	2.0	SCLK
	Core Priority Access Low to High	1.5	0.5	29.5	2.0	0.75	2.0	SCLK
$\overline{\text{DPA}}$	DMA Priority Access High to Low	1.5	0.5	4.0	1.0	0.75	2.0	SCLK
	DMA Priority Access Low to High	1.5	0.5	29.5	2.0	0.75	2.0	SCLK
$\overline{\text{BMS}}$	Boot Memory Select	—	—	4.0	1.0	1.15	2.0	SCLK
FLAG3–0[2]	FLAG Pins	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{RST\_IN}}$[3, 4]	Global Reset Pin	1.5	2.5	—	—	—	—	SCLK[5]
TMS	Test Mode Select (JTAG)	1.5	0.5	—	—	—	—	TCK
TDI	Test Data Input (JTAG)	1.5	0.5	—	—	—	—	TCK
TDO	Test Data Output (JTAG)	—	—	4.0	1.0	0.75	2.0	TCK[6]
$\overline{\text{TRST}}$[3, 4]	Test Reset (JTAG)	1.5	0.5	—	—	—	—	TCK
$\overline{\text{EMU}}$[7]	Emulation High to Low	—	—	5.5	2.0	1.15	4.0	TCK or SCLK
ID2–0[8]	Static Pins—Must Be Constant	—	—	—	—	—	—	—
CONTROLIMP1–0[8]	Static Pins—Must Be Constant	—	—	—	—	—	—	—

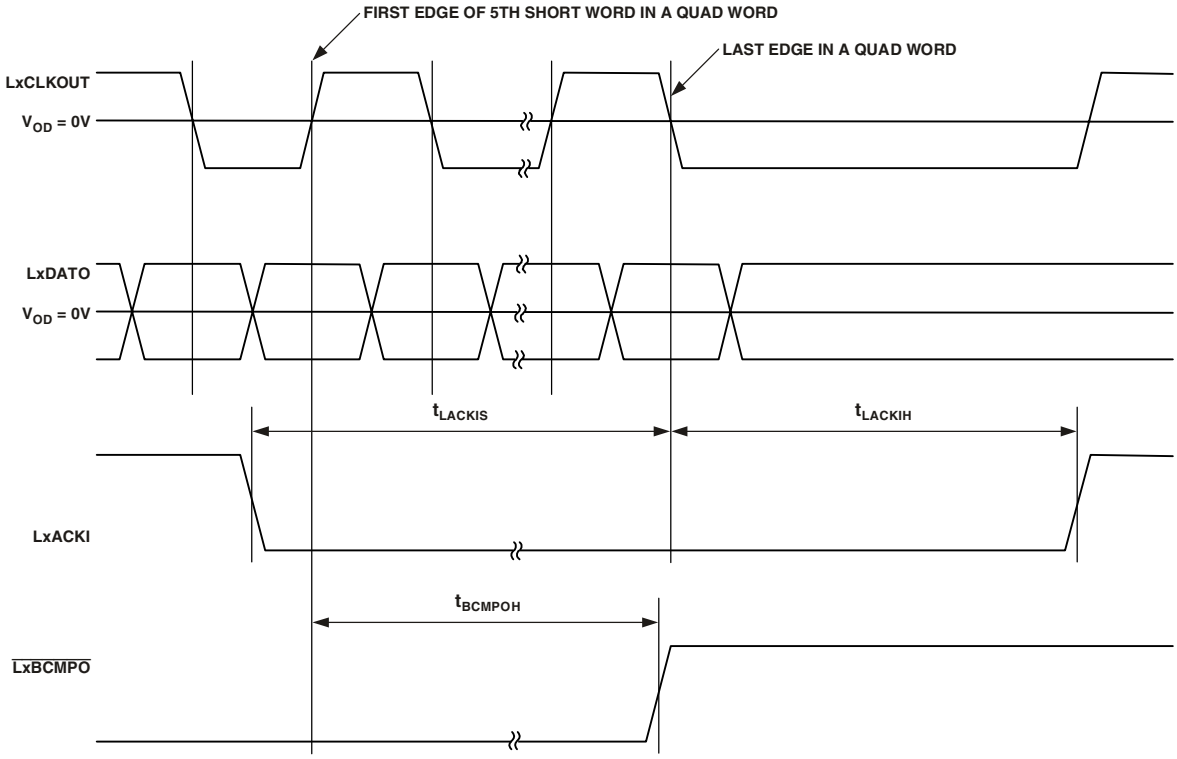

Figure 22. Link Ports—Transmission End and Stops

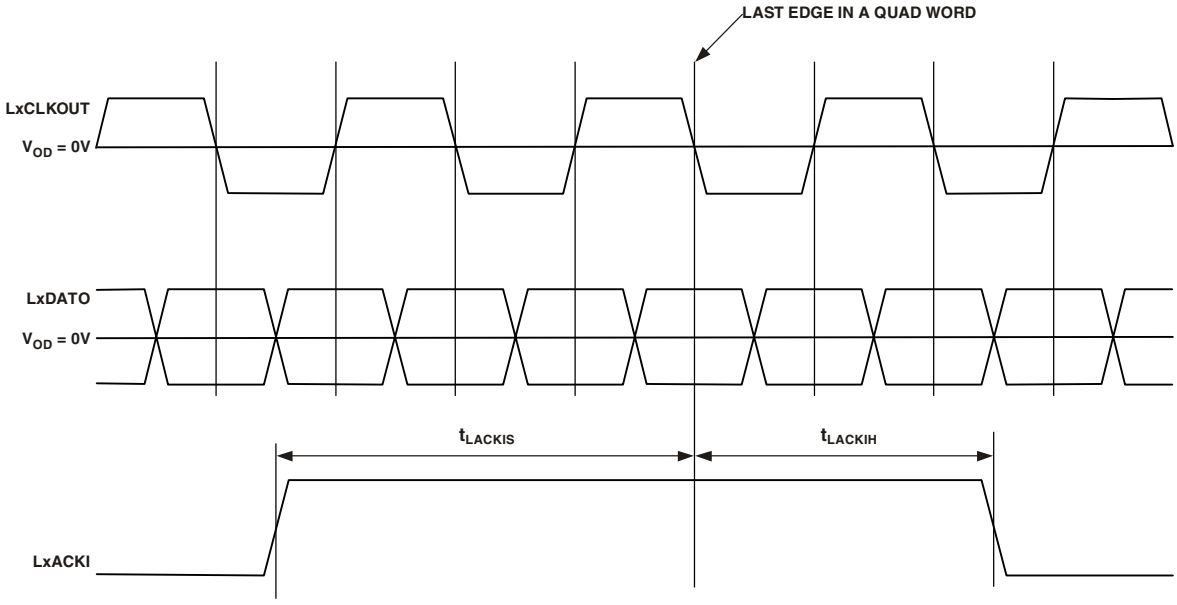

Figure 23. Link Ports—Back to Back Transmission

Link Port—Data In Timing

Table 33 with Figure 24 and Figure 25 provide the data in timing for the LVDS link ports.

Table 33. Link Port—Data In Timing

Parameter	Description	Min	Max	Unit
Inputs				
t_{LCLKIP}	LxCLKIN Period (Figure 25)	Greater of 1.8 or $0.9 \times t_{CCLK}$[1]	12.5	ns
t_{LDIS}	LxDATI Input Setup (Figure 25)	0.20[1, 2]		ns
		0.25[1, 3]		ns
		0.30[1, 4]		ns
		0.35[1, 5]		ns
t_{LDIH}	LxDATI Input Hold (Figure 25)	0.20[1, 2]		ns
		0.25[1, 3]		ns
		0.30[1, 4]		ns
		0.35[1, 5]		ns
t_{BCMPIS}	$\overline{\text{LxBCMPI}}$ Setup (Figure 24)	$2 \times t_{LCLKIP}$[1]		ns
t_{BCMPIH}	$\overline{\text{LxBCMPI}}$ Hold (Figure 24)	$2 \times t_{LCLKIP}$[1]		ns

[1] Timing is relative to the 0 differential voltage (V_{OD} = 0).
[2] $|V_{ID}|$ = 250 mV
[3] $|V_{ID}|$ = 217 mV
[4] $|V_{ID}|$ = 206 mV
[5] $|V_{ID}|$ = 195 mV

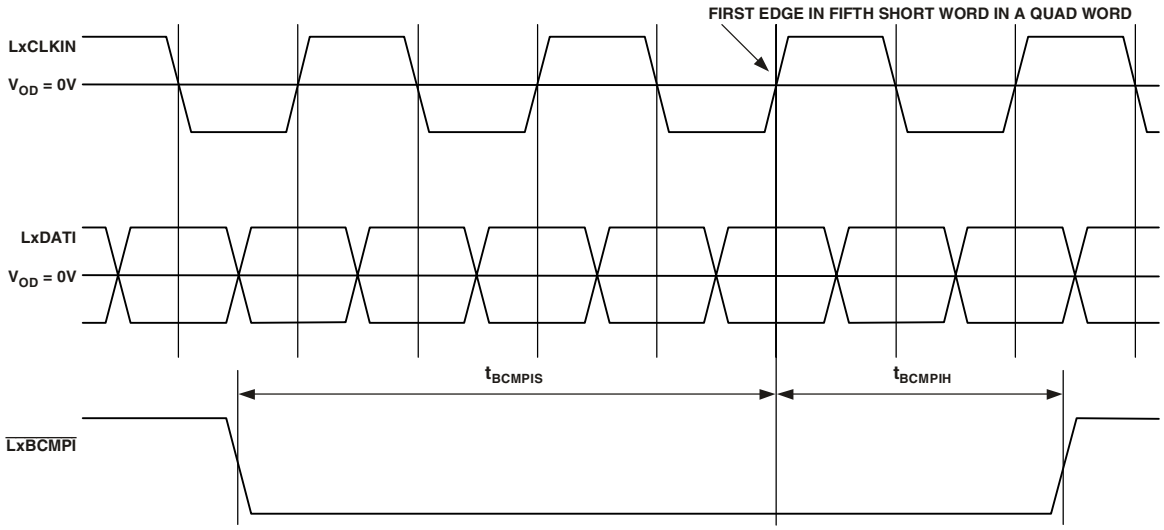

Figure 24. Link Ports—Last Received Quad Word

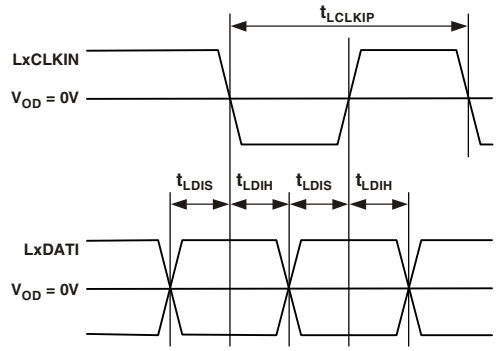

Figure 25. Link Ports—Data Input Setup and Hold[1]

[1] These parameters are valid for both clock edges.

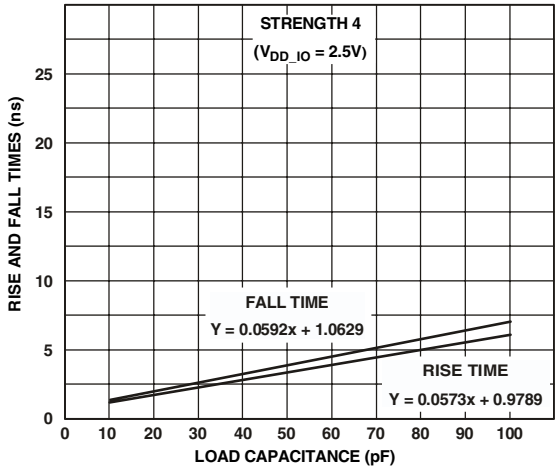

Figure 41. Typical Output Rise and Fall Time (10% to 90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 4

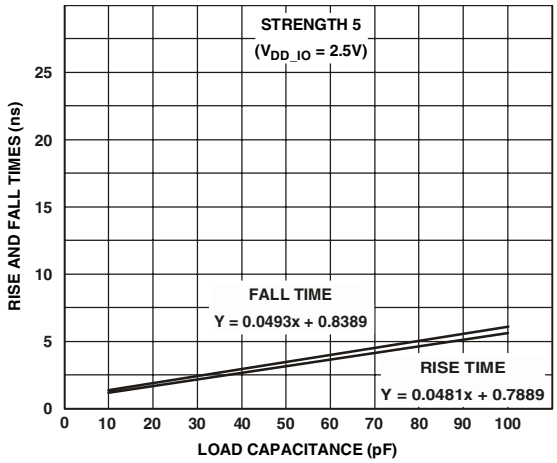

Figure 42. Typical Output Rise and Fall Time (10% to 90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 5

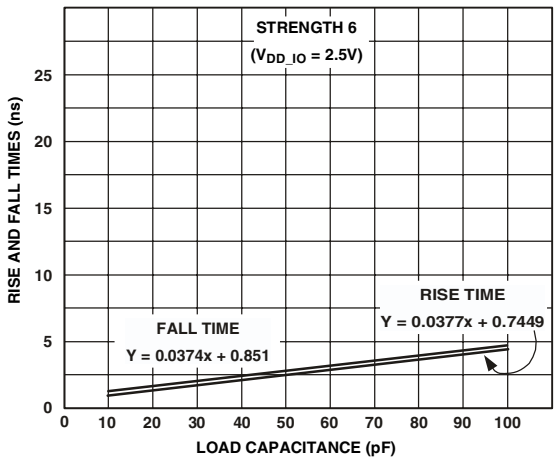

Figure 43. Typical Output Rise and Fall Time (10% to 90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 6

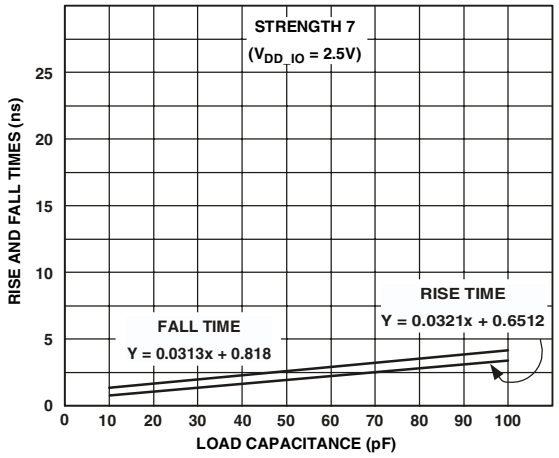

Figure 44. Typical Output Rise and Fall Time (10% to 90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 7

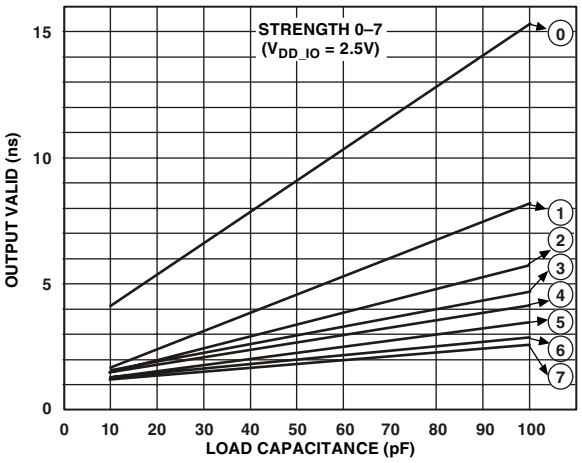

Figure 45. Typical Output Valid (V_{DD_IO} = 2.5 V) vs. Load Capacitance at Max Case Temperature and Strength 0 to 7[1]

[1] The line equations for the output valid vs. load capacitance are:
Strength 0: y = 0.1255x + 2.7873
Strength 1: y = 0.0764x + 1.0492
Strength 2: y = 0.0474x + 1.0806
Strength 3: y = 0.0345x + 1.2329
Strength 4: y = 0.0296x + 1.2064
Strength 5: y = 0.0246x + 1.0944
Strength 6: y = 0.0187x + 1.1005
Strength 7: y = 0.0156x + 1.084

Table 35. 576-Ball (25 mm × 25 mm) BGA_ED Ball Assignments (Continued)

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
J1	$\overline{RAS}$	K1	SDA10	L1	$\overline{SDWE}$	M1	$\overline{BR3}$
J2	$\overline{CAS}$	K2	SDCKE	L2	$\overline{BR0}$	M2	SCLKRAT1
J3	V_{SS}	K3	LDQM	L3	$\overline{BR1}$	M3	$\overline{BR5}$
J4	V_{REF}	K4	HDQM	L4	$\overline{BR2}$	M4	$\overline{BR6}$
J5	V_{SS}	K5	V_{DD_IO}	L5	V_{DD_IO}	M5	V_{DD_IO}
J6	V_{DD}	K6	V_{DD}	L6	V_{DD}	M6	V_{DD}
J7	V_{DD}	K7	V_{DD}	L7	V_{DD}	M7	V_{DD}
J8	V_{SS}	K8	V_{SS}	L8	V_{SS}	M8	V_{SS}
J9	V_{SS}	K9	V_{SS}	L9	V_{SS}	M9	V_{SS}
J10	V_{SS}	K10	V_{SS}	L10	V_{SS}	M10	V_{SS}
J11	V_{SS}	K11	V_{SS}	L11	V_{SS}	M11	V_{SS}
J12	V_{SS}	K12	V_{SS}	L12	V_{SS}	M12	V_{SS}
J13	V_{SS}	K13	V_{SS}	L13	V_{SS}	M13	V_{SS}
J14	V_{SS}	K14	V_{SS}	L14	V_{SS}	M14	V_{SS}
J15	V_{SS}	K15	V_{SS}	L15	V_{SS}	M15	V_{SS}
J16	V_{SS}	K16	V_{SS}	L16	V_{SS}	M16	V_{SS}
J17	V_{SS}	K17	V_{SS}	L17	V_{SS}	M17	V_{SS}
J18	V_{DD}	K18	V_{DD_DRAM}	L18	V_{DD_DRAM}	M18	V_{DD}
J19	V_{DD}	K19	V_{DD_DRAM}	L19	V_{DD_DRAM}	M19	V_{DD}
J20	V_{SS}	K20	V_{DD_IO}	L20	V_{DD_IO}	M20	V_{DD_IO}
J21	L0ACKO	K21	L0DATI1_N	L21	L0DATI3_N	M21	V_{SS}
J22	$\overline{L0BCMPI}$	K22	L0DATI1_P	L22	L0DATI3_P	M22	V_{SS}
J23	L0DATI0_N	K23	L0CLKINN	L23	L0DATI2_N	M23	L0DATO3_N
J24	L0DATI0_P	K24	L0CLKINP	L24	L0DATI2_P	M24	L0DATO3_P
N1	ID0	P1	SCLK	R1	V_{SS}	T1	$\overline{RST\_IN}$
N2	V_{SS}	P2	SCLK_VREF	R2	NC (SCLK)[1]	T2	SCLKRAT2
N3	V_{DD_A}	P3	V_{SS}	R3	NC (SCLK_VREF)[1]	T3	$\overline{BR4}$
N4	V_{DD_A}	P4	$\overline{BM}$	R4	$\overline{BR7}$	T4	DS0
N5	V_{DD_IO}	P5	V_{DD_IO}	R5	V_{DD_IO}	T5	V_{SS}
N6	V_{DD}	P6	V_{DD}	R6	V_{DD}	T6	V_{DD}
N7	V_{DD}	P7	V_{DD}	R7	V_{DD}	T7	V_{DD}
N8	V_{SS}	P8	V_{SS}	R8	V_{SS}	T8	V_{SS}
N9	V_{SS}	P9	V_{SS}	R9	V_{SS}	T9	V_{SS}
N10	V_{SS}	P10	V_{SS}	R10	V_{SS}	T10	V_{SS}
N11	V_{SS}	P11	V_{SS}	R11	V_{SS}	T11	V_{SS}
N12	V_{SS}	P12	V_{SS}	R12	V_{SS}	T12	V_{SS}
N13	V_{SS}	P13	V_{SS}	R13	V_{SS}	T13	V_{SS}
N14	V_{SS}	P14	V_{SS}	R14	V_{SS}	T14	V_{SS}
N15	V_{SS}	P15	V_{SS}	R15	V_{SS}	T15	V_{SS}
N16	V_{SS}	P16	V_{SS}	R16	V_{SS}	T16	V_{SS}
N17	V_{SS}	P17	V_{SS}	R17	V_{SS}	T17	V_{SS}
N18	V_{DD}	P18	V_{DD_DRAM}	R18	V_{DD_DRAM}	T18	V_{DD}
N19	V_{DD}	P19	V_{DD_DRAM}	R19	V_{DD_DRAM}	T19	V_{DD}
N20	V_{DD_IO}	P20	V_{DD_IO}	R20	V_{DD_IO}	T20	V_{SS}
N21	L0DATO2_N	P21	L0DATO1_N	R21	NC	T21	L1DATI0_N
N22	L0DATO2_P	P22	L0DATO1_P	R22	V_{SS}	T22	L1DATI0_P
N23	L0CLKON	P23	L0DATO0_N	R23	$\overline{L0BCMPO}$	T23	L1ACKO
N24	L0CLKOP	P24	L0DATO0_P	R24	L0ACKI	T24	$\overline{L1BCMPI}$

D04324-0-11/06(C)