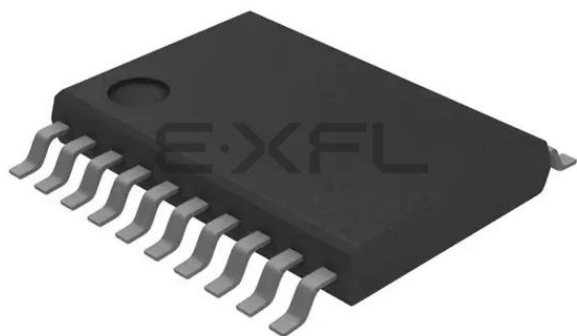




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	16
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s08rn16w2mtjr

- Peripherals
 - ACMP - one analog comparator with both positive and negative inputs; separately selectable interrupt on rising and falling comparator output; filtering
 - ADC - 12-channel, 12-bit resolution for 48-, 32-pin packages; 10-channel, 10-bit resolution for 20-pin package; 8-channel, 10-bit for 16-pin package; 2.5 μ s conversion time; data buffers with optional watermark; automatic compare function; internal bandgap reference channel; operation in stop mode; optional hardware trigger
 - CRC - programmable cyclic redundancy check module
 - FTM - two flex timer modulators modules including one 6-channel and one 2-channel ones; 16-bit counter; each channel can be configured for input capture, output compare, edge- or center-aligned PWM mode
 - IIC - One inter-integrated circuit module; up to 400 kbps; multi-master operation; programmable slave address; supporting broadcast mode and 10-bit addressing
 - MTIM - One modulo timer with 8-bit prescaler and overflow interrupt
 - RTC - 16-bit real time counter (RTC)
 - SCI - two serial communication interface (SCI/UART) modules optional 13-bit break; full duplex non-return to zero (NRZ); LIN extension support
 - SPI - one 8-bit serial peripheral interface (SPI) modules; full-duplex or single-wire bidirectional; master or slave mode
 - TSI - supporting up to 16 external electrodes; configurable software or hardware scan trigger; fully support freescale touch sensing software library; capability to wake MCU from stop3 mode
- Input/Output
 - Up to 35 GPIOs including one output-only pin
 - One 8-bit keyboard interrupt module (KBI)
 - Two true open-drain output pins
 - Four, ultra-high current sink pins supporting 20 mA source/sink current
- Package options
 - 48-pin LQFP
 - 32-pin LQFP
 - 20-pin TSSOP
 - 16-pin TSSOP

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1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: RN16 and RN8.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

S 9 S08 RN AA F1 B CC

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
S	Qualification status	S = fully qualified, general market flow
9	Memory	9 = flash based
S08	Core	S08 = 8-bit CPU
RN	Device family	RN
AA	Approximate flash size in KB	16 = 16 KB 8 = 8 KB
F1	Fab and mask set identifier	W2
B	Temperature range (°C)	M = -40 to 125
CC	Package designator	LF = 48-LQFP

Table 3. LVD and POR Specification

Symbol	C	Description		Min	Typ	Max	Unit
V _{POR}	D	POR re-arm voltage ^{1, 2}		1.5	1.75	2.0	V
V _{LVDH}	C	Falling low-voltage detect threshold - high range (LVDV = 1) ³		4.2	4.3	4.4	V
V _{LVW1H}	C	Falling low-voltage warning threshold - high range	Level 1 falling (LVWV = 00)	4.3	4.4	4.5	V
V _{LVW2H}	C		Level 2 falling (LVWV = 01)	4.5	4.5	4.6	V
V _{LVW3H}	C		Level 3 falling (LVWV = 10)	4.6	4.6	4.7	V
V _{LVW4H}	C		Level 4 falling (LVWV = 11)	4.7	4.7	4.8	V
V _{HYSH}	C	High range low-voltage detect/warning hysteresis		—	100	—	mV
V _{LVDL}	C	Falling low-voltage detect threshold - low range (LVDV = 0)		2.56	2.61	2.66	V
V _{LVDW1L}	C	Falling low-voltage warning threshold - low range	Level 1 falling (LVWV = 00)	2.62	2.7	2.78	V
V _{LVDW2L}	C		Level 2 falling (LVWV = 01)	2.72	2.8	2.88	V
V _{LVDW3L}	C		Level 3 falling (LVWV = 10)	2.82	2.9	2.98	V
V _{LVDW4L}	C		Level 4 falling (LVWV = 11)	2.92	3.0	3.08	V
V _{HYSDL}	C	Low range low-voltage detect hysteresis		—	40	—	mV
V _{HYSWL}	C	Low range low-voltage warning hysteresis		—	80	—	mV
V _{BG}	P	Buffered bandgap output ⁴		1.14	1.16	1.18	V

1. Maximum is highest voltage that POR is guaranteed.
2. POR ramp time must be longer than 20us/V to get a stable startup.
3. Rising thresholds are falling threshold + hysteresis.
4. Voltage factory trimmed at V_{DD} = 5.0 V, Temp = 125 °C

Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (low drive strength) ($V_{DD} = 5\text{ V}$)

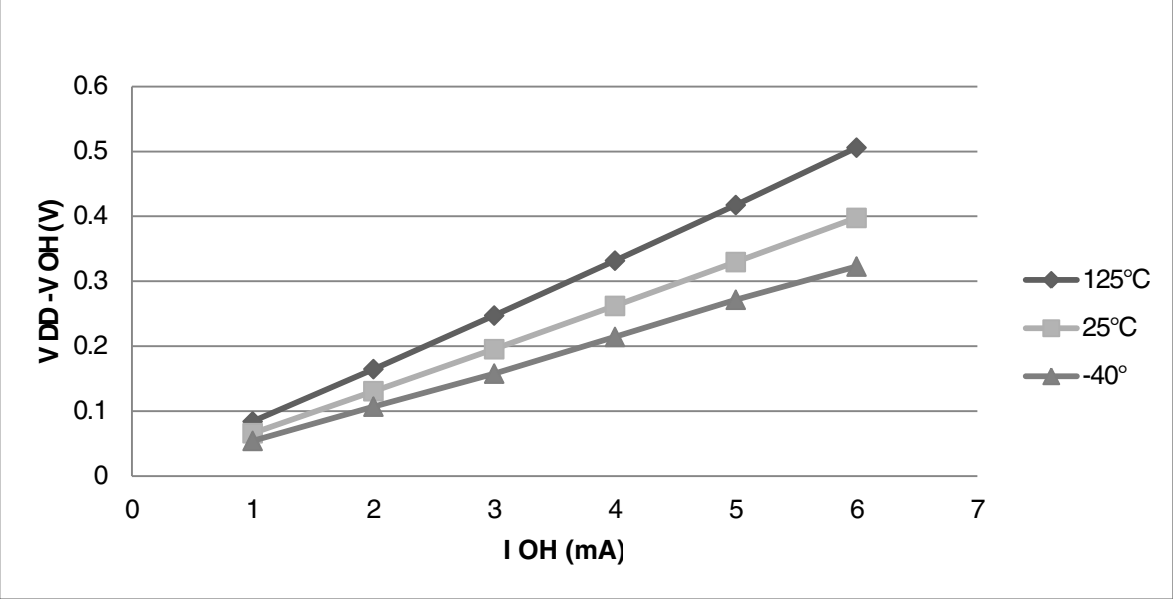


Figure 1. Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (standard drive strength) ($V_{DD} = 5\text{ V}$)

Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (low drive strength) ($V_{DD} = 3\text{ V}$)

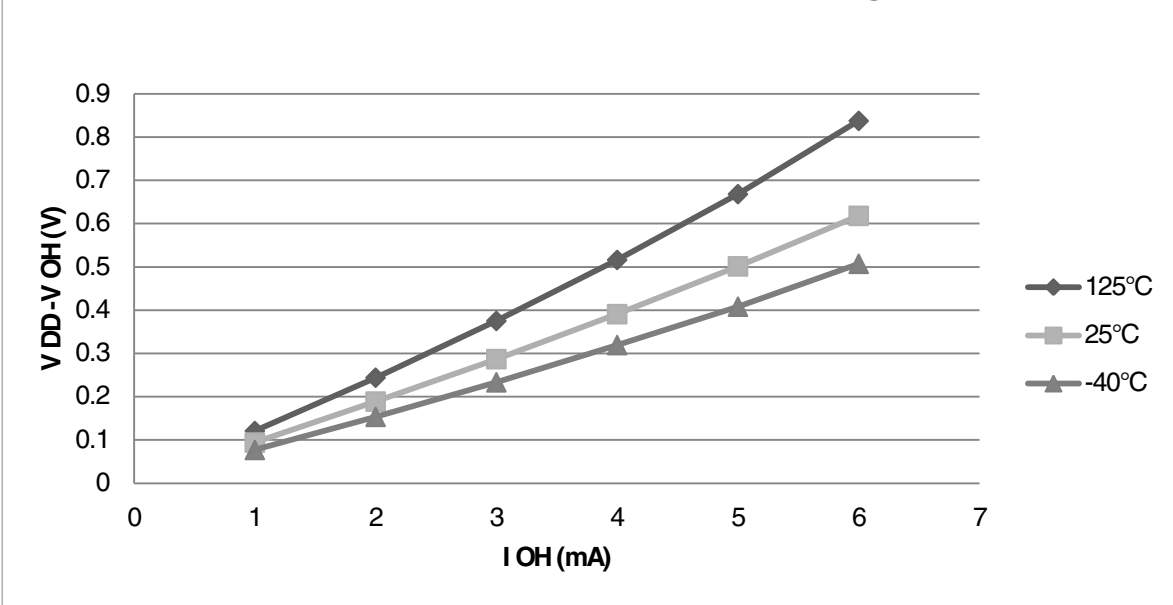


Figure 2. Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (standard drive strength) ($V_{DD} = 3\text{ V}$)

Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (high drive strength) ($V_{DD} = 5\text{ V}$)

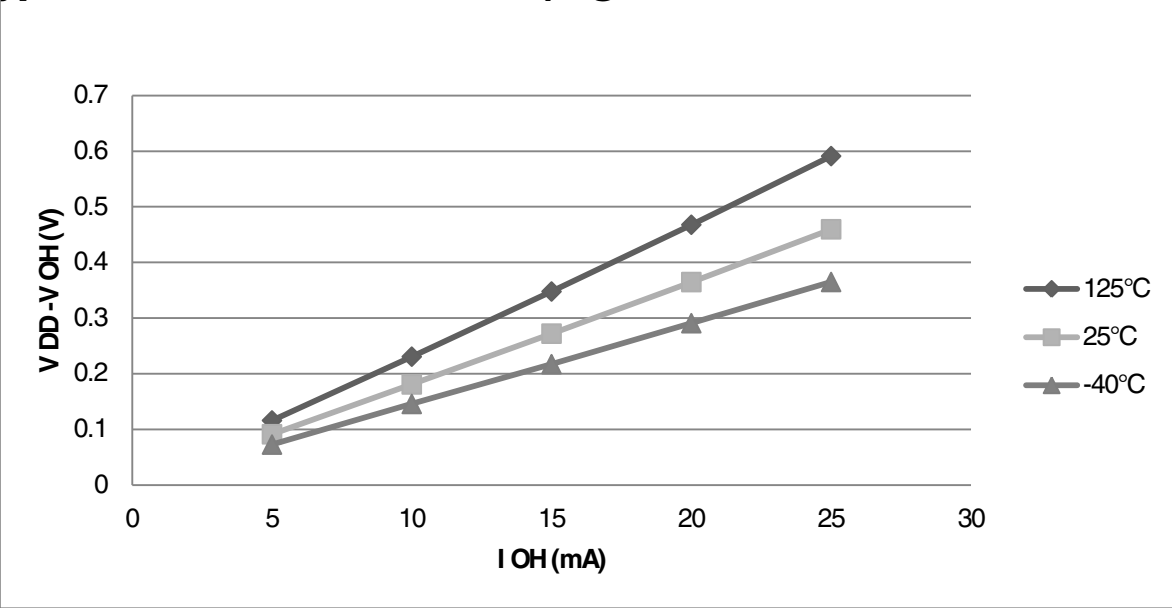


Figure 3. Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (high drive strength) ($V_{DD} = 5\text{ V}$)

Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (high drive strength) ($V_{DD} = 3\text{ V}$)

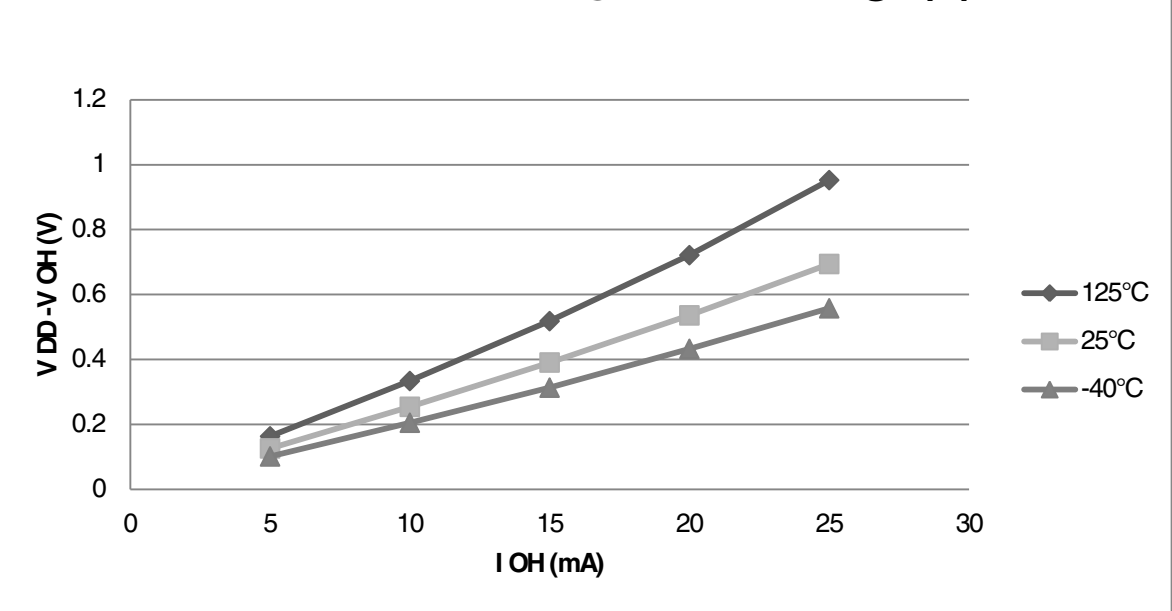


Figure 4. Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (high drive strength) ($V_{DD} = 3\text{ V}$)

Table 4. Supply current characteristics (continued)

Num	C	Parameter	Symbol	Bus Freq	V _{DD} (V)	Typical ¹	Max	Unit	Temp
	C	ADLPC = 1 ADLSMP = 1 ADCO = 1 MODE = 10B ADICLK = 11B			3	39	—		
8	C	TSI adder to stop3 ⁴	—	—	5	121	—	μA	-40 to 125 °C
	C	PS = 010B NSCN = 0x0F EXTCHRG = 0 REFCHRG = 0 DVOLT = 01B			3	120	—		
9	C	LVD adder to stop3 ⁵	—	—	5	128	—	μA	-40 to 125 °C
	C				3	124	—		

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. RTC adder cause <1 μA I_{DD} increase typically, RTC clock source is 1kHz LPO clock.
3. ACMP adder cause <10 μA I_{DD} increase typically.
4. The current varies with TSI configuration and capacity of touch electrode. Please refer to [TSI electrical specifications](#).
5. LVD is periodically woken up from stop3 by 5% duty cycle. The period is equal to or less than 2 ms.

5.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as [AN2321](#), [AN1050](#), [AN1263](#), [AN2764](#), and [AN1259](#) for advice and guidance specifically targeted at optimizing EMC performance.

5.2 Switching specifications

5.2.1 Control timing

Table 5. Control timing

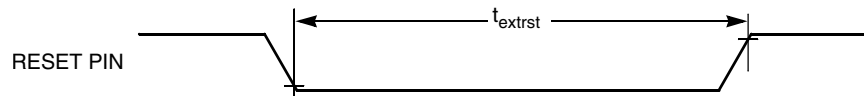
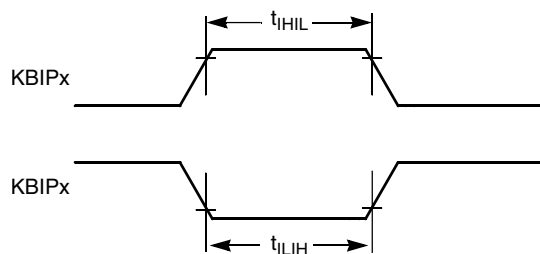
Num	C	Rating	Symbol	Min	Typical ¹	Max	Unit
1	P	Bus frequency (t _{cyc} = 1/f _{Bus})	f _{Bus}	DC	—	20	MHz
2	P	Internal low power oscillator frequency	f _{LPO}	0.67	1.0	1.25	KHz

Table continues on the next page...

Table 5. Control timing (continued)

Num	C	Rating	Symbol	Min	Typical ¹	Max	Unit
3	D	External reset pulse width ²	t_{extrst}	$1.5 \times t_{Self_reset}$	—	—	ns
4	D	Reset low drive	t_{rstdrv}	$34 \times t_{cyc}$	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes ³	t_{MSH}	100	—	—	ns
7	D	Keyboard interrupt pulse width	Asynchronous path ²	t_{LIH}	100	—	ns
	D		Synchronous path	t_{IHIL}	$1.5 \times t_{cyc}$	—	ns
8	C	Port rise and fall time - standard drive strength (load = 50 pF) ⁴	—	t_{Rise}	—	10.2	ns
	C		—	t_{Fall}	—	9.5	ns
	C	Port rise and fall time - high drive strength (load = 50 pF) ⁴	—	t_{Rise}	—	5.4	ns
	C		—	t_{Fall}	—	4.6	ns

- Typical values are based on characterization data at $V_{DD} = 5.0\text{ V}$, $25\text{ }^{\circ}\text{C}$ unless otherwise stated.
- This is the shortest pulse that is guaranteed to be recognized as a reset pin request.
- To enter BDM mode following a POR, BKGD/MS must be held low during the powerup and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD} .
- Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range $-40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$.


Figure 9. Reset timing

Figure 10. KBIPx timing

5.2.2 Debug trace timing specifications

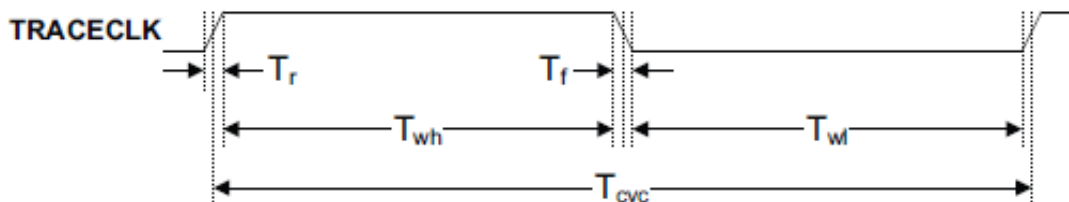
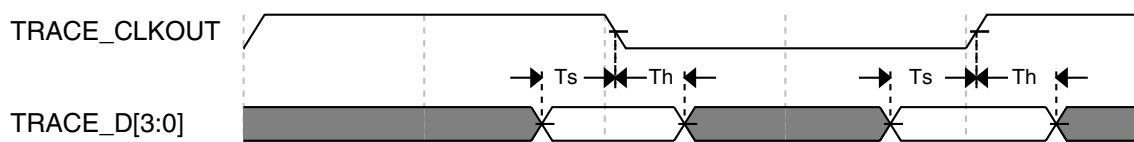
Table 6. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
t_{cyc}	Clock period	Frequency dependent		MHz
t_{wl}	Low pulse width	2	—	ns

Table continues on the next page...

Table 6. Debug trace operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit
t_{wh}	High pulse width	2	—	ns
t_r	Clock and data rise time	—	3	ns
t_f	Clock and data fall time	—	3	ns
t_s	Data setup	3	—	ns
t_h	Data hold	2	—	ns


Figure 11. TRACE_CLKOUT specifications

Figure 12. Trace data specifications

5.2.3 FTM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 7. FTM input timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

6.1 External oscillator (XOSC) and ICS characteristics

Table 9. XOSC and ICS specifications (temperature range = -40 to 125 °C ambient)

Num	C	Characteristic		Symbol	Min	Typical ¹	Max	Unit
1	C	Oscillator crystal or resonator	Low range (RANGE = 0)	f_{lo}	32	—	40	kHz
	C		High range (RANGE = 1) FEE or FBE mode ²	f_{hi}	4	—	20	MHz
	C		High range (RANGE = 1), high gain (HGO = 1), FBELP mode	f_{hi}	4	—	20	MHz
	C		High range (RANGE = 1), low power (HGO = 0), FBELP mode	f_{hi}	4	—	20	MHz
2	D	Load capacitors		C1, C2	See Note ³			
3	D	Feedback resistor	Low Frequency, Low-Power Mode ⁴	R_F	—	—	—	MΩ
			Low Frequency, High-Gain Mode		—	10	—	MΩ
			High Frequency, Low-Power Mode		—	1	—	MΩ
			High Frequency, High-Gain Mode		—	1	—	MΩ
4	D	Series resistor - Low Frequency	Low-Power Mode ⁴	R_S	—	—	—	kΩ
			High-Gain Mode		—	200	—	kΩ
5	D	Series resistor - High Frequency	Low-Power Mode ⁴	R_S	—	—	—	kΩ
	D	Series resistor - High Frequency, High-Gain Mode	4 MHz		—	0	—	kΩ
	D		8 MHz		—	0	—	kΩ
	D		16 MHz		—	0	—	kΩ
6	C	Crystal start-up time Low range = 39.0625 kHz crystal; High range = 20 MHz crystal ^{5, 6}	Low range, low power	t_{CSTL}	—	1000	—	ms
	C		Low range, high power		—	800	—	ms
	C		High range, low power	t_{CSTH}	—	3	—	ms
	C		High range, high power		—	1.5	—	ms
7	T	Internal reference start-up time		t_{IRST}	—	20	50	μs
8	D	Square wave input clock frequency	FEE or FBE mode ²	f_{extal}	0.03125	—	5	MHz
	D		FBELP mode		0	—	20	MHz
9	P	Average internal reference frequency - trimmed		f_{int_t}	—	39.0625	—	kHz
10	P	DCO output frequency range - trimmed		f_{dco_t}	16	—	20	MHz
11	P	Total deviation of DCO output from trimmed frequency ⁵	Over full voltage range and temperature range of -40 to 125 °C	Δf_{dco_t}	—	—	±2.0	
	C		Over full voltage range and temperature range of -40 to 105 °C				±1.5	% f_{dco}

Table continues on the next page...

**Table 9. XOSC and ICS specifications (temperature range = -40 to 125 °C ambient)
(continued)**

Num	C	Characteristic	Symbol	Min	Typical ¹	Max	Unit
	C	Over fixed voltage and temperature range of 0 to 70 °C				±1.0	
12	C	FLL acquisition time ^{5, 7}	$t_{Acquire}$	—	—	2	ms
13	C	Long term jitter of DCO output clock (averaged over 2 ms interval) ⁸	C_{Jitter}	—	0.02	0.2	% f_{dco}

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. When ICS is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.
3. See crystal or resonator manufacturer's recommendation.
4. Load capacitors (C_1, C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.
5. This parameter is characterized and not tested on each device.
6. Proper PC board layout procedures must be followed to achieve specifications.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

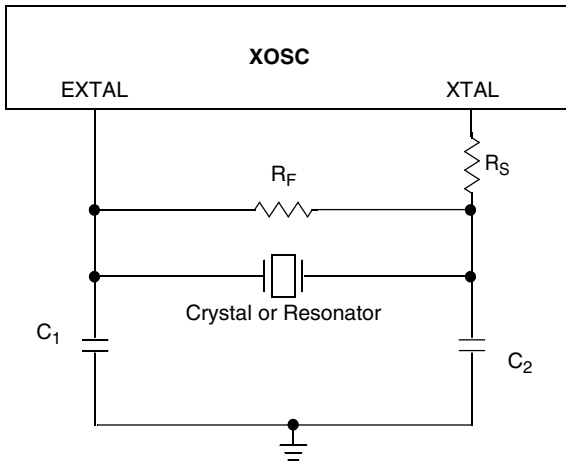


Figure 15. Typical crystal or resonator circuit

6.2 NVM specifications

This section provides details about program/erase times and program/erase endurance for the flash and EEPROM memories.

Table 10. Flash characteristics

C	Characteristic	Symbol	Min ¹	Typical ²	Max ³	Unit ⁴
D	Supply voltage for program/erase -40 °C to 125 °C	V _{prog/erase}	2.7	—	5.5	V
D	Supply voltage for read operation	V _{Read}	2.7	—	5.5	V
D	NVM Bus frequency	f _{NVMBUS}	1	—	25	MHz
D	NVM Operating frequency	f _{NVMOP}	0.8	1	1.05	MHz
D	Erase Verify All Blocks	t _{VFYALL}	—	—	17338	t _{cyc}
D	Erase Verify Flash Block	t _{RD1BLK}	—	—	16913	t _{cyc}
D	Erase Verify EEPROM Block	t _{RD1BLK}	—	—	810	t _{cyc}
D	Erase Verify Flash Section	t _{RD1SEC}	—	—	484	t _{cyc}
D	Erase Verify EEPROM Section	t _{DRD1SEC}	—	—	555	t _{cyc}
D	Read Once	t _{RDONCE}	—	—	450	t _{cyc}
D	Program Flash (2 word)	t _{PGM2}	0.12	0.12	0.29	ms
D	Program Flash (4 word)	t _{PGM4}	0.20	0.21	0.46	ms
D	Program Once	t _{PGMONCE}	0.20	0.21	0.21	ms
D	Program EEPROM (1 Byte)	t _{DPGM1}	0.10	0.10	0.27	ms
D	Program EEPROM (2 Byte)	t _{DPGM2}	0.17	0.18	0.43	ms
D	Program EEPROM (3 Byte)	t _{DPGM3}	0.25	0.26	0.60	ms
D	Program EEPROM (4 Byte)	t _{DPGM4}	0.32	0.33	0.77	ms
D	Erase All Blocks	t _{ERSALL}	96.01	100.78	101.49	ms
D	Erase Flash Block	t _{ERSBLK}	95.98	100.75	101.44	ms
D	Erase Flash Sector	t _{ERSPG}	19.10	20.05	20.08	ms
D	Erase EEPROM Sector	t _{DERSPG}	4.81	5.05	20.57	ms
D	Unsecure Flash	t _{UNSECU}	96.01	100.78	101.48	ms
D	Verify Backdoor Access Key	t _{VFYKEY}	—	—	464	t _{cyc}
D	Set User Margin Level	t _{MLOADU}	—	—	407	t _{cyc}
C	FLASH Program/erase endurance T _L to T _H = -40 °C to 125 °C	n _{FLPE}	10 k	100 k	—	Cycles
C	EEPROM Program/erase endurance T _L to T _H = -40 °C to 125 °C	n _{FLPE}	50 k	500 k	—	Cycles
C	Data retention at an average junction temperature of T _{Javg} = 85°C after up to 10,000 program/erase cycles	t _{D_ret}	15	100	—	years

1. Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}
2. Typical times are based on typical f_{NVMOP} and maximum f_{NVMBUS}
3. Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging
4. t_{cyc} = 1 / f_{NVMBUS}

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

6.3 Analog

6.3.1 ADC characteristics

Table 11. 5 V 12-bit ADC operating conditions

Characteristic	Conditions	Symb	Min	Typ ¹	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	—
	Delta to V_{DD} ($V_{DD}-V_{DDAD}$)	ΔV_{DDA}	-100	0	+100	mV	
Ground voltage	Delta to V_{SS} ($V_{SS}-V_{SSA}$) ²	ΔV_{SSA}	-100	0	+100	mV	
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input resistance		R_{ADIN}	—	3	5	k Ω	—
Analog source resistance	12-bit mode	R_{AS}	—	—	2	k Ω	External to MCU
	• $f_{ADCK} > 4$ MHz		—	—	5		
	• $f_{ADCK} < 4$ MHz		—	—	5		
	10-bit mode		—	—	5		
	• $f_{ADCK} > 4$ MHz		—	—	10		
	• $f_{ADCK} < 4$ MHz		—	—	10		
	8-bit mode		—	—	10		
ADC conversion clock frequency	High speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	—
	Low power (ADLPC=1)		0.4	—	4.0		

1. Typical values assume $V_{DDA} = 5.0$ V, Temp = 25°C, $f_{ADCK}=1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.

Table 12. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Characteristic	Conditions	C	Symb	Min	Typ ¹	Max	Unit
	Low power (ADLPC = 1)			1.25	2	3.3	
Conversion time (including sample time)	Short sample (ADLSMP = 0)	T	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	40	—	
Sample time	Short sample (ADLSMP = 0)	T	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	23.5	—	
Total unadjusted Error ²	12-bit mode	T	E_{TUE}	—	±5.0	—	LSB ³
	10-bit mode	P		—	±1.5	±2.0	
	8-bit mode	P ⁴		—	±0.7	±1.0	
Differential Non-Linearity	12-bit mode	T	DNL	—	±1.0	—	LSB ³
	10-bit mode ⁵	P		—	±0.25	±0.5	
	8-bit mode ⁵	P ⁴		—	±0.15	±0.25	
Integral Non-Linearity	12-bit mode	T	INL	—	±1.0	—	LSB ³
	10-bit mode	T		—	±0.3	±0.5	
	8-bit mode	T		—	±0.15	±0.25	
Zero-scale error ⁶	12-bit mode	C	E_{ZS}	—	±2.0	—	LSB ³
	10-bit mode	P		—	±0.25	±1.0	
	8-bit mode	P ⁴		—	±0.65	±1.0	
Full-scale error ⁷	12-bit mode	T	E_{FS}	—	±2.5	—	LSB ³
	10-bit mode	T		—	±0.5	±1.0	
	8-bit mode	T		—	±0.5	±1.0	
Quantization error	≤12 bit modes	D	E_Q	—	—	±0.5	LSB ³
Input leakage error ⁸	all modes	D	E_{IL}	$I_{in} * R_{AS}$			mV
Temp sensor slope	-40°C– 25°C	D	m	—	3.266	—	mV/°C
	25°C– 125°C			—	3.638	—	
Temp sensor voltage	25°C	D	V_{TEMP25}	—	1.396	—	V

- Typical values assume $V_{DDA} = 5.0$ V, Temp = 25°C, $f_{ADCK} = 1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- Includes quantization.
- 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
- 10-bit mode only for package LQFP48/32, TSSOP20/16. Those parameters are only achieved by the design characterization.
- Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes
- $V_{ADIN} = V_{SSA}$
- $V_{ADIN} = V_{DDA}$
- I_{in} = leakage current (refer to DC characteristics)

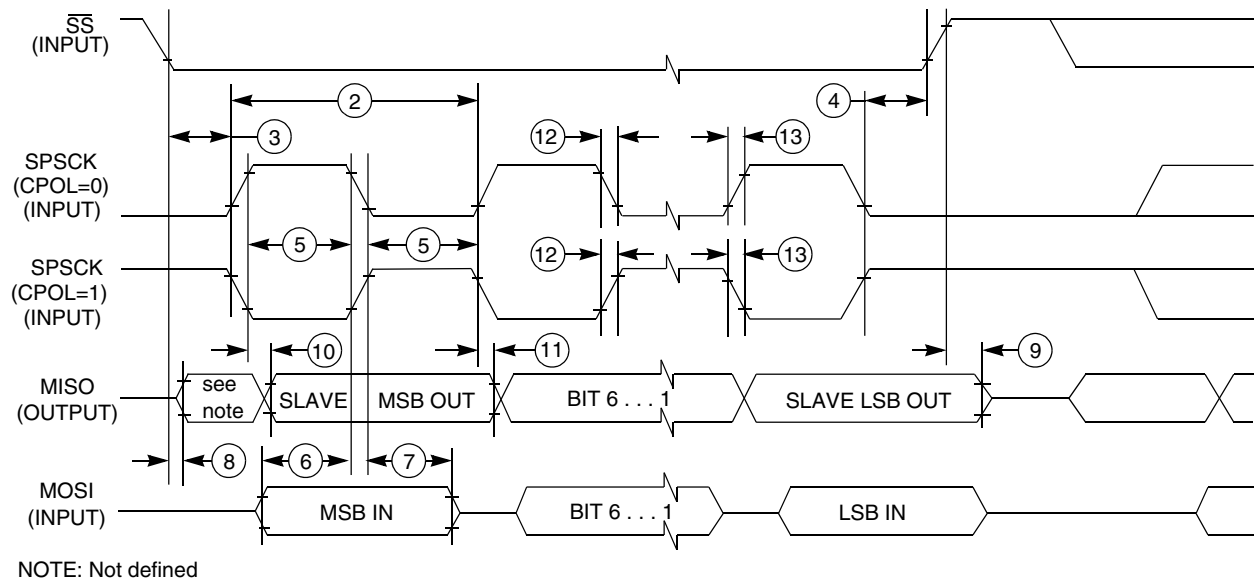


Figure 20. SPI slave mode timing (CPHA=1)

6.5 Human-machine interfaces (HMI)

6.5.1 TSI electrical specifications

Table 16. TSI electrical specifications

Symbol	Description	Min.	Type	Max	Unit
TSI_RUNF	Fixed power consumption in run mode	—	100	—	μA
TSI_RUNV	Variable power consumption in run mode (depends on oscillator's current selection)	1.0	—	128	μA
TSI_EN	Power consumption in enable mode	—	100	—	μA
TSI_DIS	Power consumption in disable mode	—	1.2	—	μA
TSI_TEN	TSI analog enable time	—	66	—	μs
TSI_CREF	TSI reference capacitor	—	1.0	—	pF
TSI_DVOLT	Voltage variation of VP & VM around nominal values	-10	—	10	%

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
16-pin TSSOP	98ASH70247A
20-pin TSSOP	98ASH70169A
32-pin LQFP	98ASH70029A
48-pin LQFP	98ASH00962A

8 Pinout

8.1 Signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

Table 17. Pin availability by package pin-count

Pin Number				Lowest Priority <-- --> Highest				
48-LQFP	32-LQFP	20-TSSOP	16-TSSOP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
1	1	—	—	PTD1 ¹	—	FTM2CH3	—	—
2	2	—	—	PTD0 ¹	—	FTM2CH2	—	—
3	—	—	—	PTE4	—	TCLK2	—	—
4	—	—	—	PTE3	—	BUSOUT	—	—
5	3	3	3	—	—	—	—	V _{DD}
6	4	—	—	—	—	—	V _{DDA}	V _{REFH}
7	5	—	—	—	—	—	V _{SSA}	V _{REFL}
8	6	4	4	—	—	—	—	V _{SS}
9	7	5	5	PTB7	—	—	SCL	EXTAL
10	8	6	6	PTB6	—	—	SDA	XTAL
11	—	—	—	—	—	—	—	V _{ss}
12	—	—	—	NC				
13	—	—	—	NC				
14	9	7	7	PTB5 ¹	—	FTM2CH5	SS0	—
15	10	8	8	PTB4 ¹	—	FTM2CH4	MISO0	—
16	11	9	—	PTC3	—	FTM2CH3	ADP11	TSI9
17	12	10	—	PTC2	—	FTM2CH2	ADP10	TSI8
18	—	—	—	PTD7	—	—	—	—

Table continues on the next page...

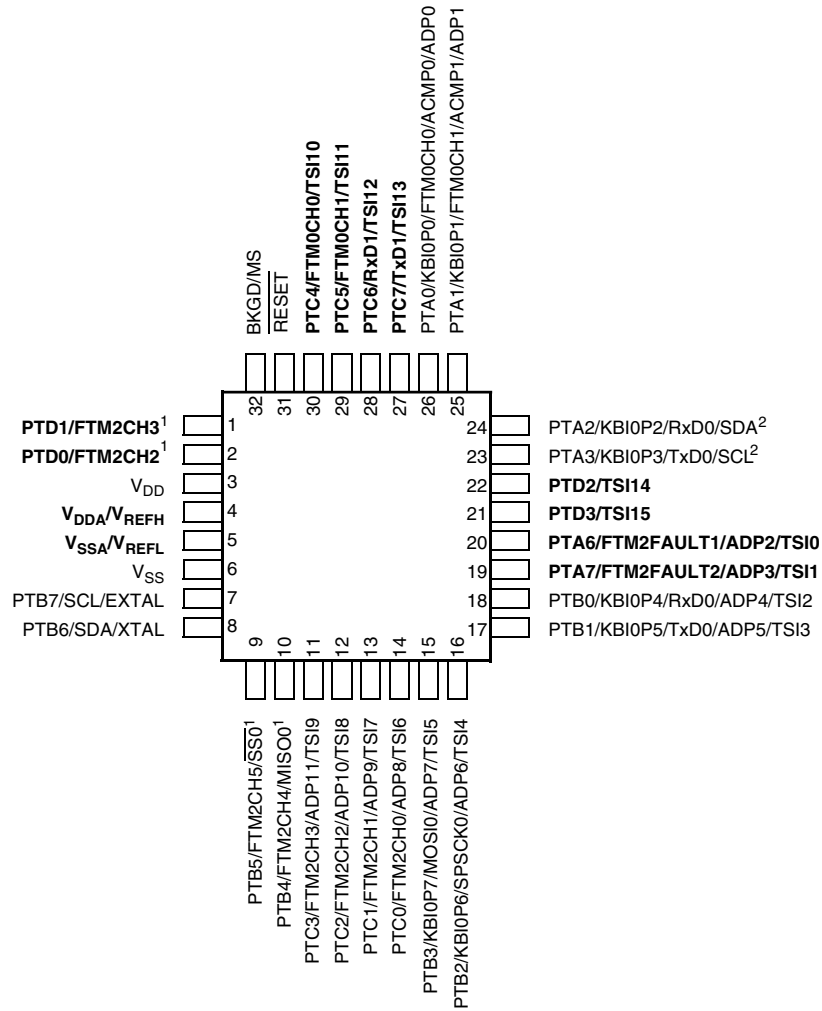
Table 17. Pin availability by package pin-count (continued)

Pin Number				Lowest Priority <-- --> Highest				
48-LQFP	32-LQFP	20-TSSOP	16-TSSOP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
19	—	—	—	PTD6	—	—	—	—
20	—	—	—	PTD5	—	—	—	—
21	13	11	—	PTC1	—	FTM2CH1	ADP9	TSI7
22	14	12	—	PTC0	—	FTM2CH0	ADP8	TSI6
23	15	13	9	PTB3	KBI0P7	MOSI0	ADP7	TSI5
24	16	14	10	PTB2	KBI0P6	SPSCK0	ADP6	TSI4
25	17	15	11	PTB1	KBI0P5	TXD0	ADP5	TSI3
26	18	16	12	PTB0	KBI0P4	RXD0	ADP4	TSI2
27	19	—	—	PTA7	—	FTM2FAULT2	ADP3	TSI1
28	20	—	—	PTA6	—	FTM2FAULT1	ADP2	TSI0
29	—	—	—	NC				
30	—	—	—	—	—	—	—	V _{ss}
31	—	—	—	—	—	—	—	V _{DD}
32	—	—	—	PTD4	—	—	—	—
33	21	—	—	PTD3	—	—	—	TSI15
34	22	—	—	PTD2	—	—	—	TSI14
35	23	17	13	PTA3 ²	KBI0P3	TXD0	SCL	—
36	24	18	14	PTA2 ²	KBI0P2	RXD0	SDA	—
37	25	19	15	PTA1	KBI0P1	FTM0CH1	ACMP1	ADP1
38	26	20	16	PTA0	KBI0P0	FTM0CH0	ACMP0	ADP0
39	27	—	—	PTC7	—	TxD1	—	TSI13
40	28	—	—	PTC6	—	RxD1	—	TSI12
41	—	—	—	NC				
42	—	—	—	PTE2	—	MISO0	—	—
43	—	—	—	PTE1	—	MOSI0	—	—
44	—	—	—	PTE0	—	SPSCK0	—	—
45	29	—	—	PTC5	—	FTM0CH1	—	TSI11
46	30	—	—	PTC4	—	FTM0CH0	—	TSI10
47	31	1	1	—	—	—	—	RESET
48	32	2	2	—	—	—	BKGD	MS

1. This is a high current drive pin when operated as output.
2. This is a true open-drain pin when operated as output.

Note

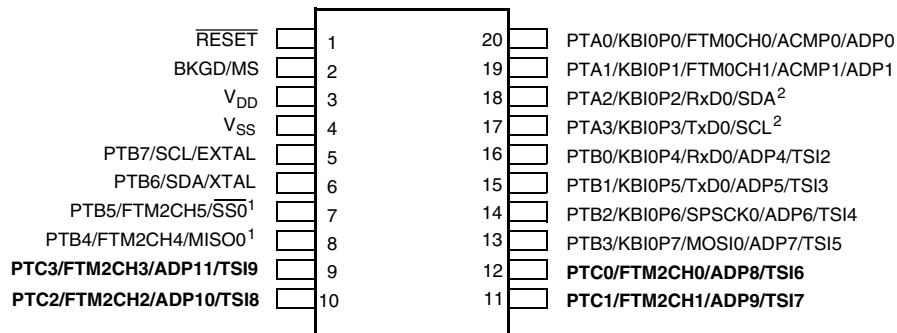
When an alternative function is first enabled, it is possible to get a spurious edge to the module. User software must clear any associated flags before interrupts are enabled. The table above illustrates the priority if multiple modules are enabled. The



Pins in **bold** are not available on less pin-count packages.

1. High source/sink current pins
2. True open drain pins

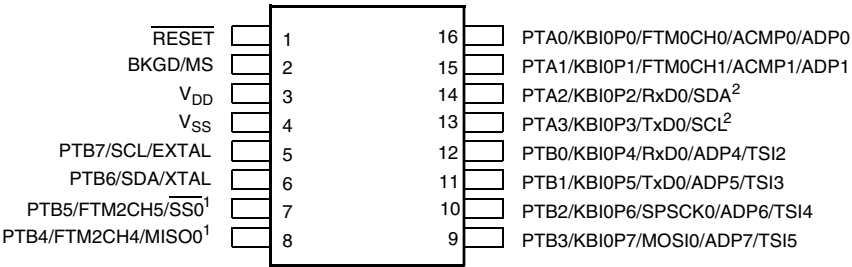
Figure 22. S9S08RN16 32-pin LQFP package



Pins in **bold** are not available on less pin-count packages.

1. High source/sink current pins
2. True open drain pins

Figure 23. S9S08RN16 20-pin TSSOP package



1. High source/sink current pins
2. True open drain pins

Figure 24. S9S08RN16 16-pin TSSOP package

9 Revision history

The following table provides a revision history for this document.

Table 18. Revision history

Rev. No.	Date	Substantial Changes
1	02/2014	Initial Release

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