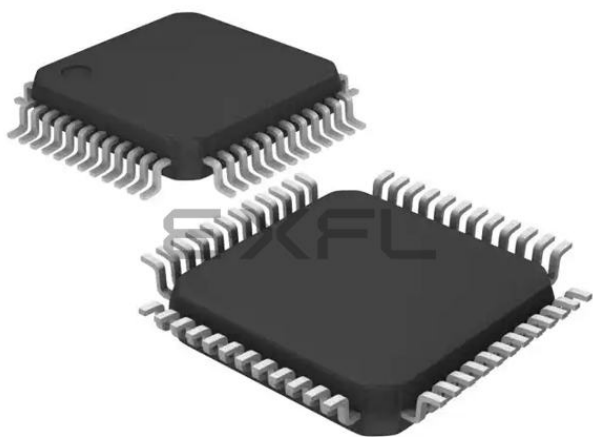




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	39
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s08rn8w2mlf

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- Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

- Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-6000	+6000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 125°C	-100	+100	mA	3

- Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
- Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
- Determined according to JEDEC Standard JESD78D, IC Latch-up Test.
 - Test was performed at 125 °C case temperature (Class II).
 - I/O pins pass +100/-100 mA I-test with Idd current limit at 400mA.
 - I/O pins pass +20/-100 mA I-test with Idd current limit at 1000mA.
 - Supply groups pass 1.5 Vccmax.
 - RESET_B pin was only tested with negative I-test due to product conditioning requirement.

4.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in below table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Table 2. DC characteristics (continued)

Symbol	C	Descriptions			Min	Typical ¹	Max	Unit
	C		High current drive pins, high-drive strength ²	5 V, $I_{load} = 20$ mA	—	—	0.8	V
	C			3 V, $I_{load} = 10$ mA	—	—	0.8	V
I_{OLT}	D	Output low current	Max total I_{OL} for all ports	5 V	—	—	100	mA
				3 V	—	—	50	
V_{IH}	P	Input high voltage	All digital inputs	$V_{DD} > 4.5V$	$0.70 \times V_{DD}$	—	—	V
	C			$V_{DD} > 2.7V$	$0.75 \times V_{DD}$	—	—	
V_{IL}	P	Input low voltage	All digital inputs	$V_{DD} > 4.5V$	—	—	$0.30 \times V_{DD}$	V
	C			$V_{DD} > 2.7V$	—	—	$0.35 \times V_{DD}$	
V_{hys}	C	Input hysteresis	All digital inputs	—	$0.06 \times V_{DD}$	—	—	mV
$ I_{in} $	P	Input leakage current	All input only pins (per pin)	$V_{IN} = V_{DD}$ or V_{SS}	—	0.1	1	μA
$ I_{OZ} $	P	Hi-Z (off-state) leakage current	All input/output (per pin)	$V_{IN} = V_{DD}$ or V_{SS}	—	0.1	1	μA
$ I_{OZTOT} $	C	Total leakage combined for all inputs and Hi-Z pins	All input only and I/O	$V_{IN} = V_{DD}$ or V_{SS}	—	—	2	μA
R_{PU}	P	Pullup resistors	All digital inputs, when enabled (all I/O pins other than PTA2 and PTA3)	—	30.0	—	50.0	k Ω
R_{PU}^3	P	Pullup resistors	PTA2 and PTA3 pin	—	30.0	—	60.0	k Ω
I_{IC}	D	DC injection current ^{4, 5, 6}	Single pin limit	$V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$	-0.2	—	2	mA
			Total MCU limit, includes sum of all stressed pins		-5	—	25	
C_{in}	C	Input capacitance, all pins			—	—	7	pF
V_{RAM}	C	RAM retention voltage			2.0	—	—	V

- Typical values are measured at 25 °C. Characterized, not tested.
- Only PTB4, PTB5 support ultra high current output.
- The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
- All functional non-supply pins, except for PTA2 and PTA3, are internally clamped to V_{SS} and V_{DD} .
- Input must be current-limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the large one.
- Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{IN} > V_{DD}$) is higher than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current higher than maximum injection current when the MCU is not consuming power, such as no system clock is present, or clock rate is very low (which would reduce overall power consumption).

Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (low drive strength) ($V_{DD} = 5\text{ V}$)

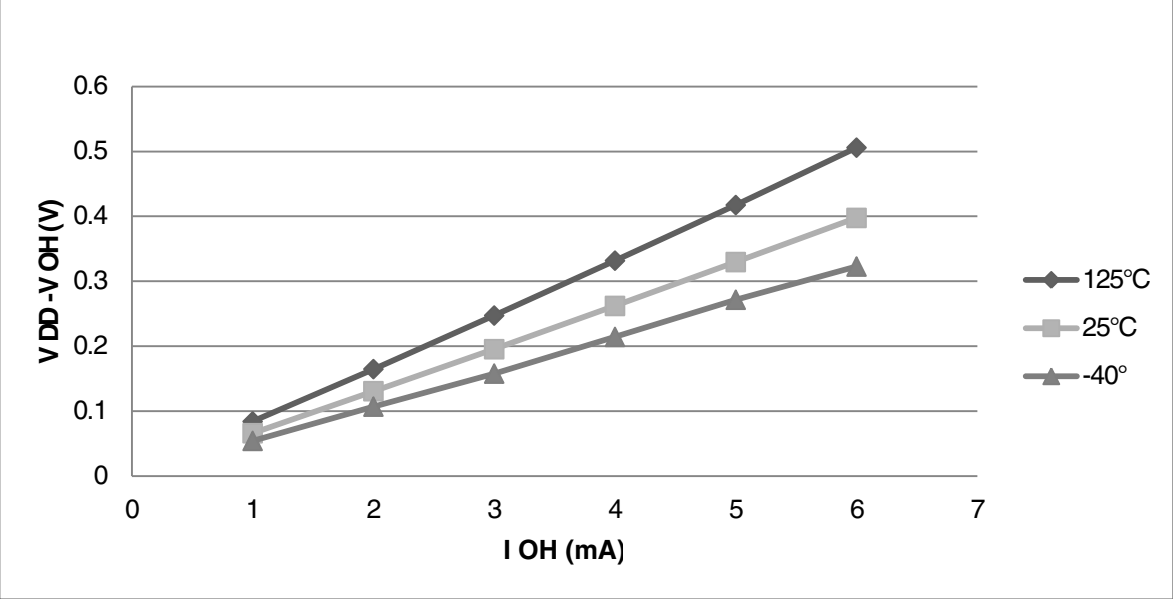


Figure 1. Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (standard drive strength) ($V_{DD} = 5\text{ V}$)

Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (low drive strength) ($V_{DD} = 3\text{ V}$)

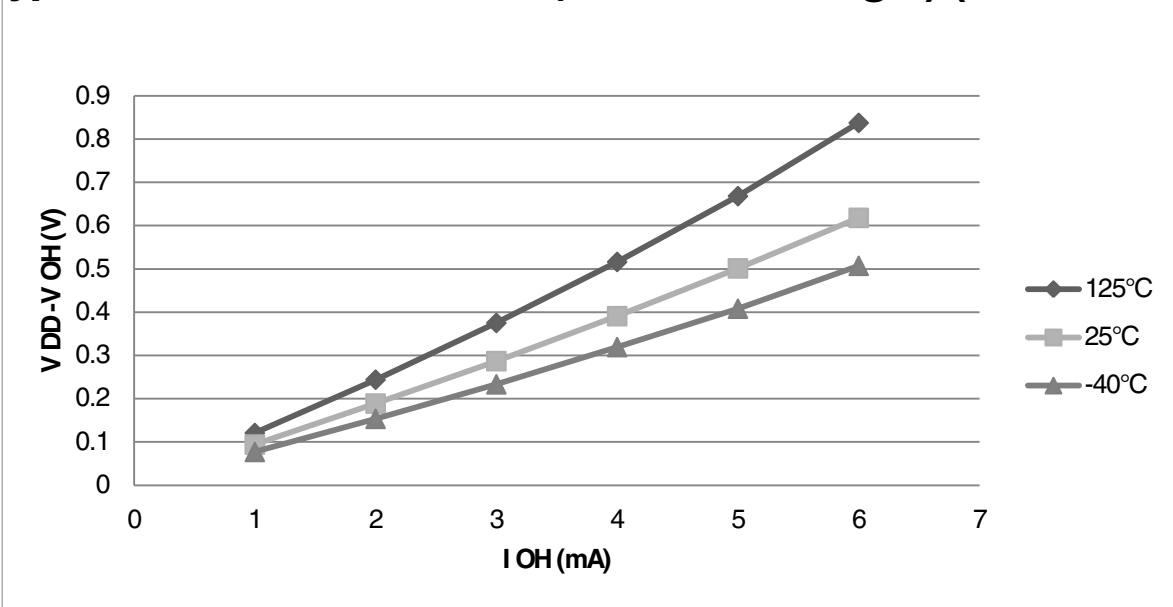


Figure 2. Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (standard drive strength) ($V_{DD} = 3\text{ V}$)

Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (high drive strength) ($V_{DD} = 5\text{ V}$)

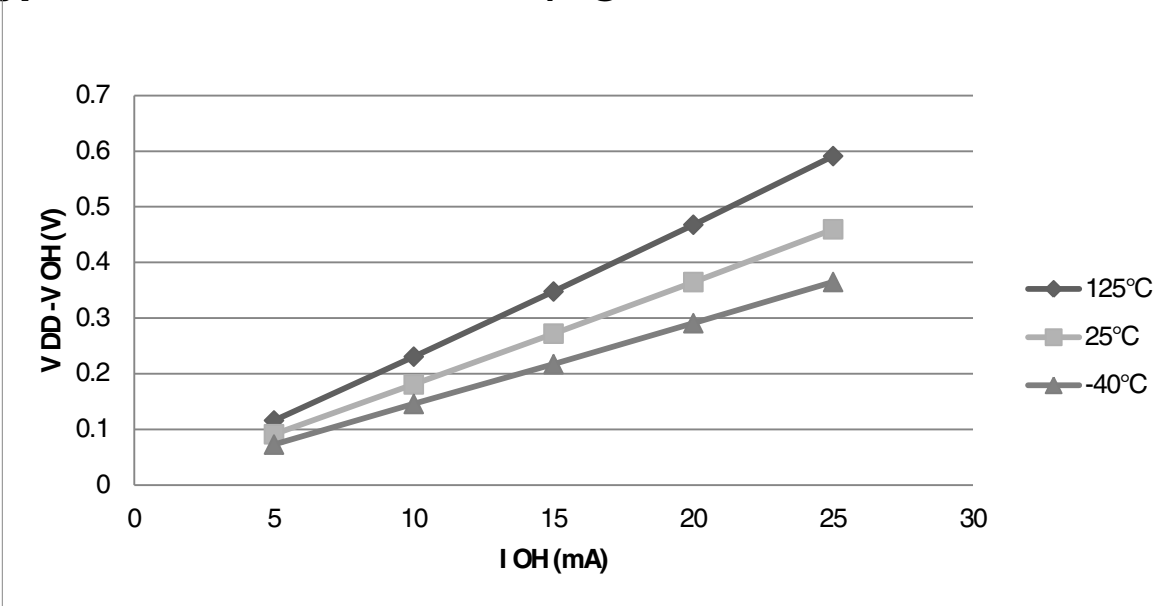


Figure 3. Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (high drive strength) ($V_{DD} = 5\text{ V}$)

Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (high drive strength) ($V_{DD} = 3\text{ V}$)

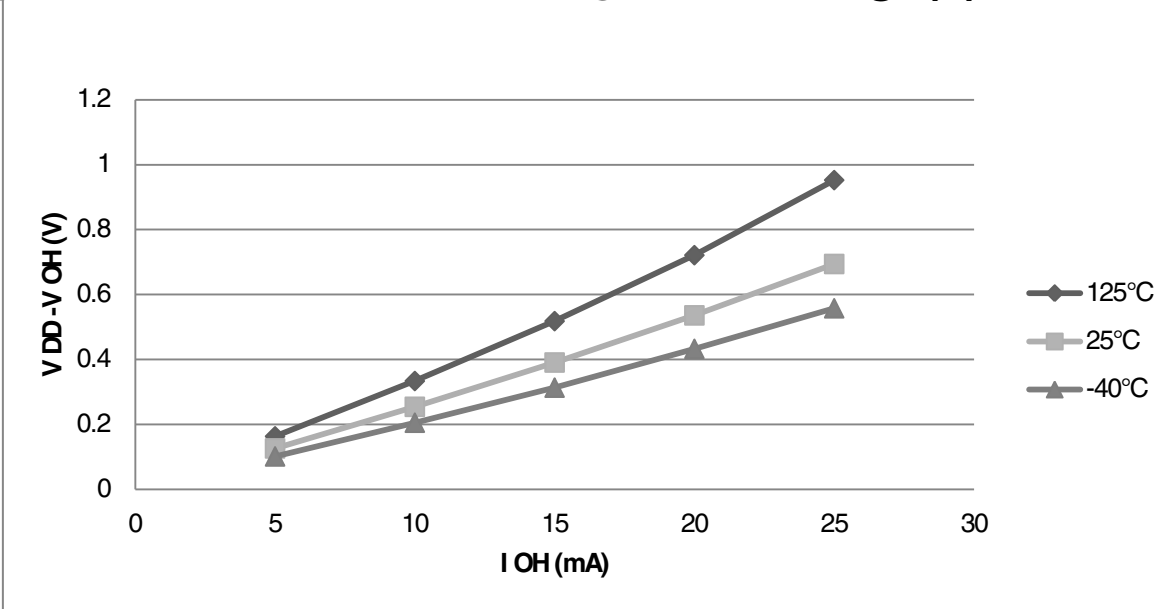


Figure 4. Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (high drive strength) ($V_{DD} = 3\text{ V}$)

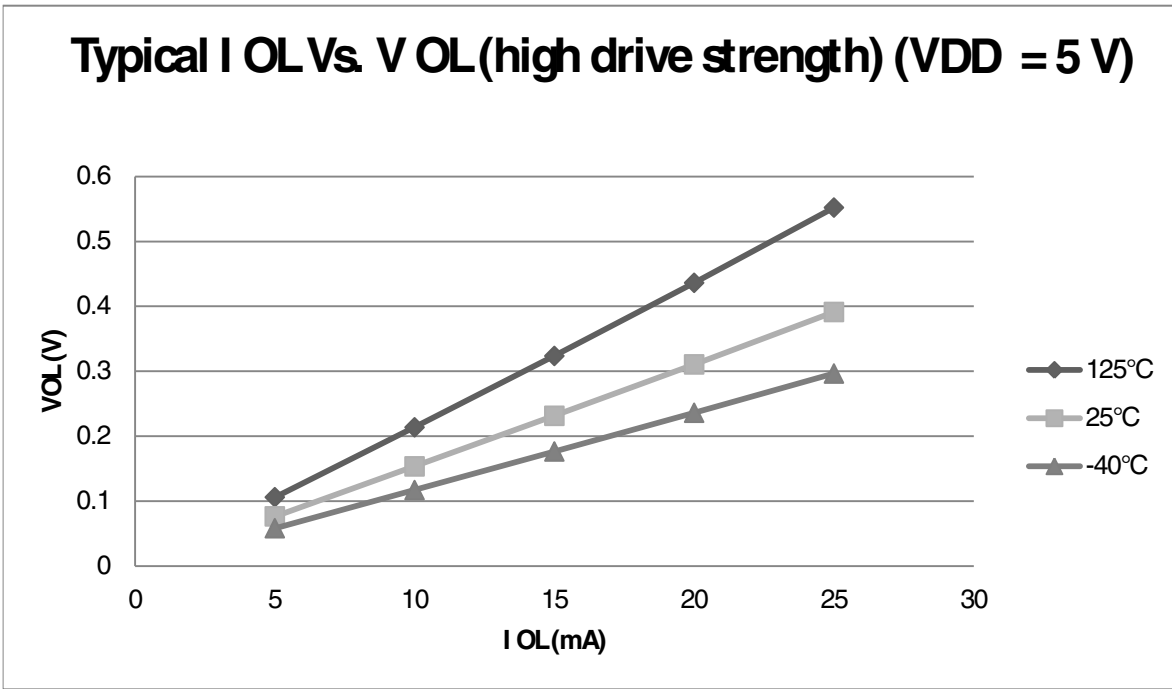


Figure 7. Typical I_{OL} Vs. V_{OL} (high drive strength) ($V_{DD} = 5\text{ V}$)

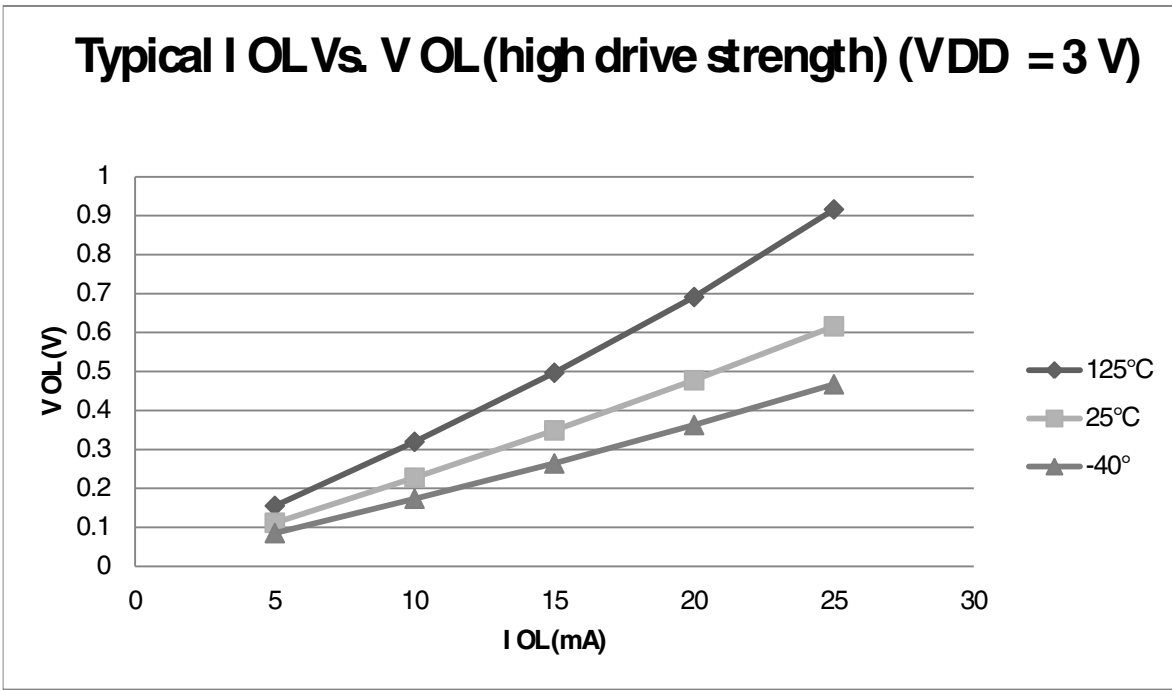


Figure 8. Typical I_{OL} Vs. V_{OL} (high drive strength) ($V_{DD} = 3\text{ V}$)

5.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 4. Supply current characteristics

Num	C	Parameter	Symbol	Bus Freq	V _{DD} (V)	Typical ¹	Max	Unit	Temp
1	C	Run supply current FEI mode, all modules on; run from flash	RI _{DD}	20 MHz	5	7.60	—	mA	-40 to 125 °C
	C			10 MHz		4.65	—		
	C			1 MHz		1.90	—		
	C			20 MHz	3	7.05	—		
	C			10 MHz		4.40	—		
	C			1 MHz		1.85	—		
2	C	Run supply current FEI mode, all modules off & gated; run from flash	RI _{DD}	20 MHz	5	5.88	—	mA	-40 to 125 °C
	C			10 MHz		3.70	—		
	C			1 MHz		1.85	—		
	C			20 MHz	3	5.35	—		
	C			10 MHz		3.42	—		
	C			1 MHz		1.80	—		
3	P	Run supply current FBE mode, all modules on; run from RAM	RI _{DD}	20 MHz	5	10.9	14.0	mA	-40 to 125 °C
	C			10 MHz		6.10	—		
	C			1 MHz		1.69	—		
	C			20 MHz	3	8.18	—		
	C			10 MHz		5.14	—		
	C			1 MHz		1.44	—		
4	P	Run supply current FBE mode, all modules off & gated; run from RAM	RI _{DD}	20 MHz	5	8.50	13.0	mA	-40 to 125 °C
	C			10 MHz		5.07	—		
	C			1 MHz		1.59	—		
	C			20 MHz	3	6.11	—		
	C			10 MHz		4.10	—		
	C			1 MHz		1.34	—		
5	C	Wait mode current FEI mode, all modules on	WI _{DD}	20 MHz	5	5.95	—	mA	-40 to 125 °C
	C			10 MHz		3.50	—		
	C			1 MHz		1.24	—		
	C			20 MHz	3	5.45	—		
	C			10 MHz		3.25	—		
	C			1 MHz		1.20	—		
6	C	Stop3 mode supply current no clocks active (except 1kHz LPO clock) ^{2,3}	S3I _{DD}	—	5	4.6	—	μA	-40 to 125 °C
	C			—	3	4.5	—		-40 to 125 °C
7	C	ADC adder to stop3	—	—	5	40	—	μA	-40 to 125 °C

Table continues on the next page...

Table 4. Supply current characteristics (continued)

Num	C	Parameter	Symbol	Bus Freq	V _{DD} (V)	Typical ¹	Max	Unit	Temp
	C	ADLPC = 1 ADLSMP = 1 ADCO = 1 MODE = 10B ADICLK = 11B			3	39	—		
8	C	TSI adder to stop3 ⁴	—	—	5	121	—	μA	-40 to 125 °C
	C	PS = 010B NSCN = 0x0F EXTCHRG = 0 REFCHRG = 0 DVOLT = 01B			3	120	—		
9	C	LVD adder to stop3 ⁵	—	—	5	128	—	μA	-40 to 125 °C
	C				3	124	—		

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. RTC adder cause <1 μA I_{DD} increase typically, RTC clock source is 1kHz LPO clock.
3. ACMP adder cause <10 μA I_{DD} increase typically.
4. The current varies with TSI configuration and capacity of touch electrode. Please refer to [TSI electrical specifications](#).
5. LVD is periodically woken up from stop3 by 5% duty cycle. The period is equal to or less than 2 ms.

5.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as [AN2321](#), [AN1050](#), [AN1263](#), [AN2764](#), and [AN1259](#) for advice and guidance specifically targeted at optimizing EMC performance.

5.2 Switching specifications

5.2.1 Control timing

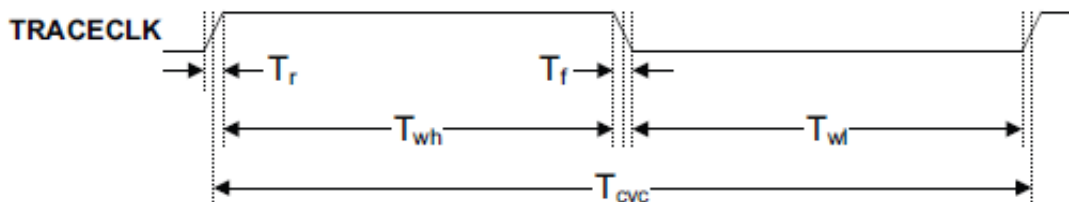
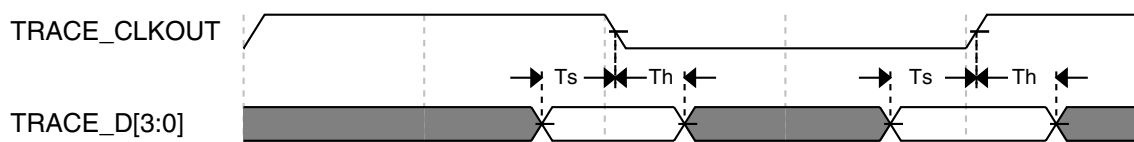
Table 5. Control timing

Num	C	Rating	Symbol	Min	Typical ¹	Max	Unit
1	P	Bus frequency (t _{cyc} = 1/f _{Bus})	f _{Bus}	DC	—	20	MHz
2	P	Internal low power oscillator frequency	f _{LPO}	0.67	1.0	1.25	KHz

Table continues on the next page...

Table 6. Debug trace operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit
t_{wh}	High pulse width	2	—	ns
t_r	Clock and data rise time	—	3	ns
t_f	Clock and data fall time	—	3	ns
t_s	Data setup	3	—	ns
t_h	Data hold	2	—	ns


Figure 11. TRACE_CLKOUT specifications

Figure 12. Trace data specifications

5.2.3 FTM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 7. FTM input timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

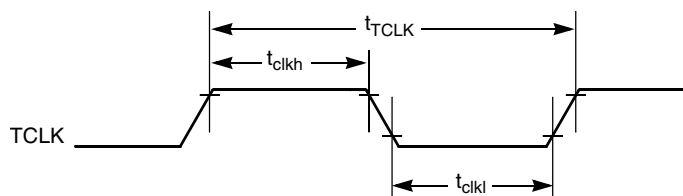


Figure 13. Timer external clock

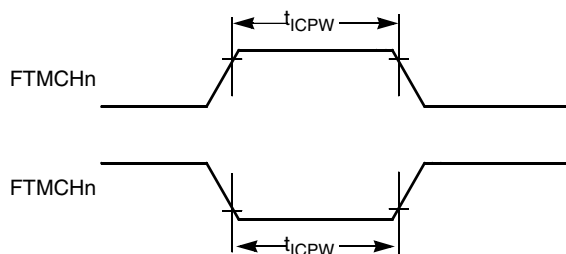


Figure 14. Timer input capture pulse

5.3 Thermal specifications

5.3.1 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 8. Thermal characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H -40 to 125	$^{\circ}\text{C}$
Junction temperature range	T_J	-40 to 135	$^{\circ}\text{C}$
Thermal resistance single-layer board			
48-pin LQFP	θ_{JA}	82	$^{\circ}\text{C/W}$
32-pin LQFP	θ_{JA}	88	$^{\circ}\text{C/W}$
20-pin TSSOP	θ_{JA}	116	$^{\circ}\text{C/W}$
16-pin TSSOP	θ_{JA}	130	$^{\circ}\text{C/W}$
Thermal resistance four-layer board			

Table continues on the next page...

**Table 9. XOSC and ICS specifications (temperature range = -40 to 125 °C ambient)
(continued)**

Num	C	Characteristic	Symbol	Min	Typical ¹	Max	Unit
	C	Over fixed voltage and temperature range of 0 to 70 °C				±1.0	
12	C	FLL acquisition time ^{5, 7}	$t_{Acquire}$	—	—	2	ms
13	C	Long term jitter of DCO output clock (averaged over 2 ms interval) ⁸	C_{Jitter}	—	0.02	0.2	% f_{dco}

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. When ICS is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.
3. See crystal or resonator manufacturer's recommendation.
4. Load capacitors (C_1, C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.
5. This parameter is characterized and not tested on each device.
6. Proper PC board layout procedures must be followed to achieve specifications.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

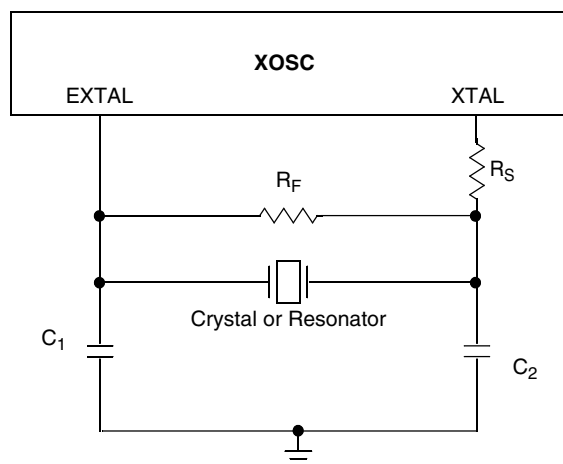


Figure 15. Typical crystal or resonator circuit

6.2 NVM specifications

This section provides details about program/erase times and program/erase endurance for the flash and EEPROM memories.

Table 10. Flash characteristics

C	Characteristic	Symbol	Min ¹	Typical ²	Max ³	Unit ⁴
D	Supply voltage for program/erase -40 °C to 125 °C	V _{prog/erase}	2.7	—	5.5	V
D	Supply voltage for read operation	V _{Read}	2.7	—	5.5	V
D	NVM Bus frequency	f _{NVMBUS}	1	—	25	MHz
D	NVM Operating frequency	f _{NVMOP}	0.8	1	1.05	MHz
D	Erase Verify All Blocks	t _{VFYALL}	—	—	17338	t _{cyc}
D	Erase Verify Flash Block	t _{RD1BLK}	—	—	16913	t _{cyc}
D	Erase Verify EEPROM Block	t _{RD1BLK}	—	—	810	t _{cyc}
D	Erase Verify Flash Section	t _{RD1SEC}	—	—	484	t _{cyc}
D	Erase Verify EEPROM Section	t _{DRD1SEC}	—	—	555	t _{cyc}
D	Read Once	t _{RDONCE}	—	—	450	t _{cyc}
D	Program Flash (2 word)	t _{PGM2}	0.12	0.12	0.29	ms
D	Program Flash (4 word)	t _{PGM4}	0.20	0.21	0.46	ms
D	Program Once	t _{PGMONCE}	0.20	0.21	0.21	ms
D	Program EEPROM (1 Byte)	t _{DPGM1}	0.10	0.10	0.27	ms
D	Program EEPROM (2 Byte)	t _{DPGM2}	0.17	0.18	0.43	ms
D	Program EEPROM (3 Byte)	t _{DPGM3}	0.25	0.26	0.60	ms
D	Program EEPROM (4 Byte)	t _{DPGM4}	0.32	0.33	0.77	ms
D	Erase All Blocks	t _{ERSALL}	96.01	100.78	101.49	ms
D	Erase Flash Block	t _{ERSBLK}	95.98	100.75	101.44	ms
D	Erase Flash Sector	t _{ERSPG}	19.10	20.05	20.08	ms
D	Erase EEPROM Sector	t _{DERSPG}	4.81	5.05	20.57	ms
D	Unsecure Flash	t _{UNSECU}	96.01	100.78	101.48	ms
D	Verify Backdoor Access Key	t _{VFYKEY}	—	—	464	t _{cyc}
D	Set User Margin Level	t _{MLOADU}	—	—	407	t _{cyc}
C	FLASH Program/erase endurance T _L to T _H = -40 °C to 125 °C	n _{FLPE}	10 k	100 k	—	Cycles
C	EEPROM Program/erase endurance T _L to T _H = -40 °C to 125 °C	n _{FLPE}	50 k	500 k	—	Cycles
C	Data retention at an average junction temperature of T _{Javg} = 85°C after up to 10,000 program/erase cycles	t _{D_ret}	15	100	—	years

1. Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}
2. Typical times are based on typical f_{NVMOP} and maximum f_{NVMBUS}
3. Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging
4. t_{cyc} = 1 / f_{NVMBUS}

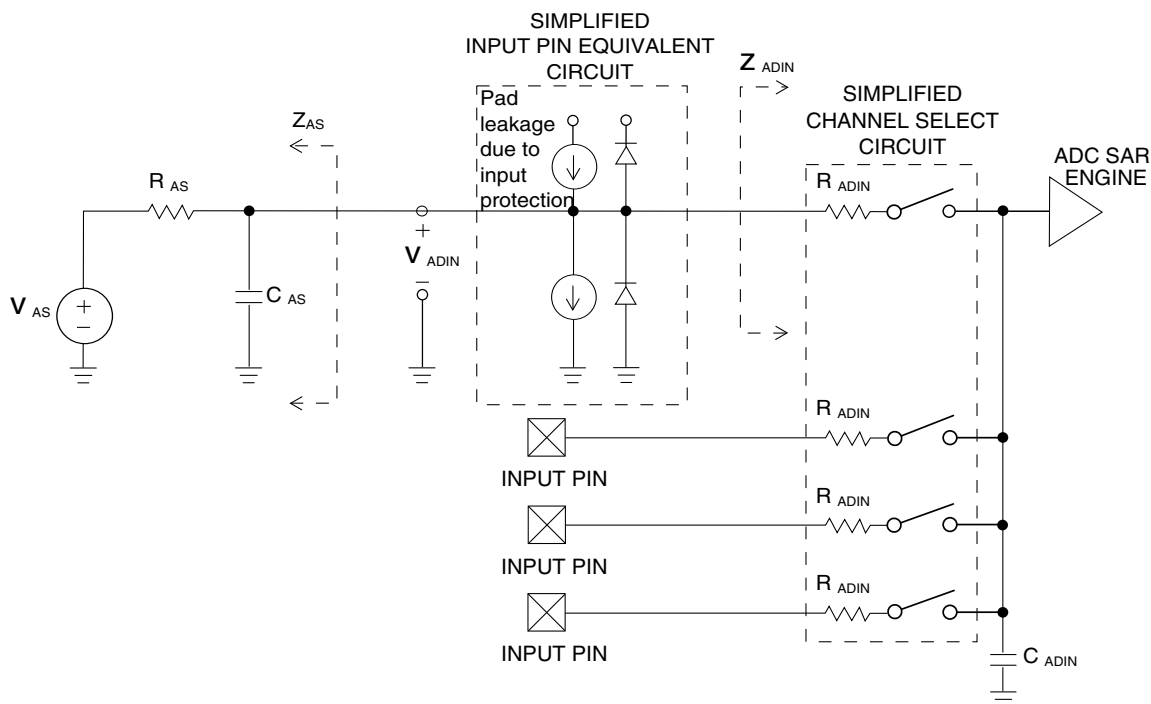


Figure 16. ADC input impedance equivalency diagram

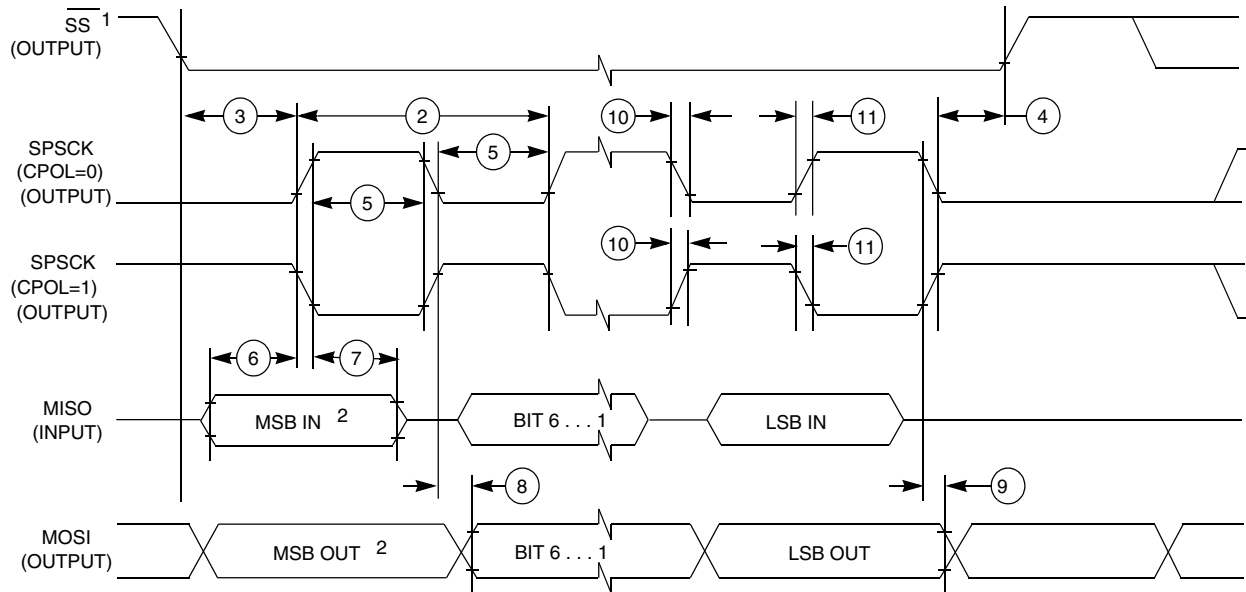
Table 12. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Characteristic	Conditions	C	Symb	Min	Typ ¹	Max	Unit
Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	133	—	μA
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		T	I_{DDA}	—	218	—	μA
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	327	—	μA
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		T	I_{DDAD}	—	582	990	μA
Supply current	Stop, reset, module off	T	I_{DDA}	—	0.011	1	μA
ADC asynchronous clock source	High speed (ADLPC = 0)	P	f_{ADACK}	2	3.3	5	MHz

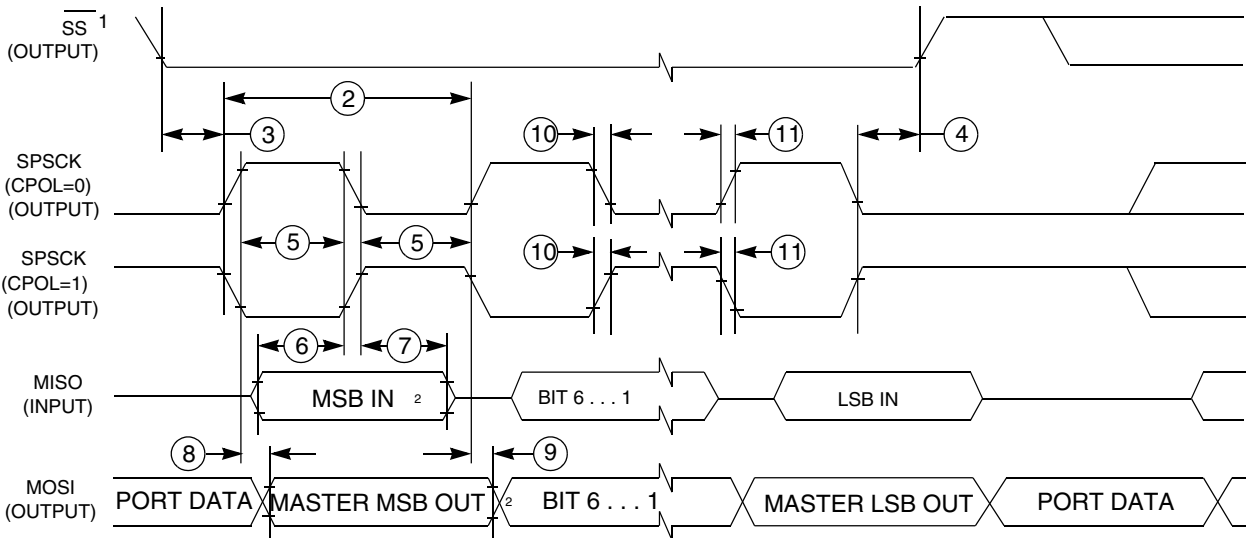
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Table 14. SPI master mode timing (continued)

Nu m.	Symbol	Description	Min.	Max.	Unit	Comment
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

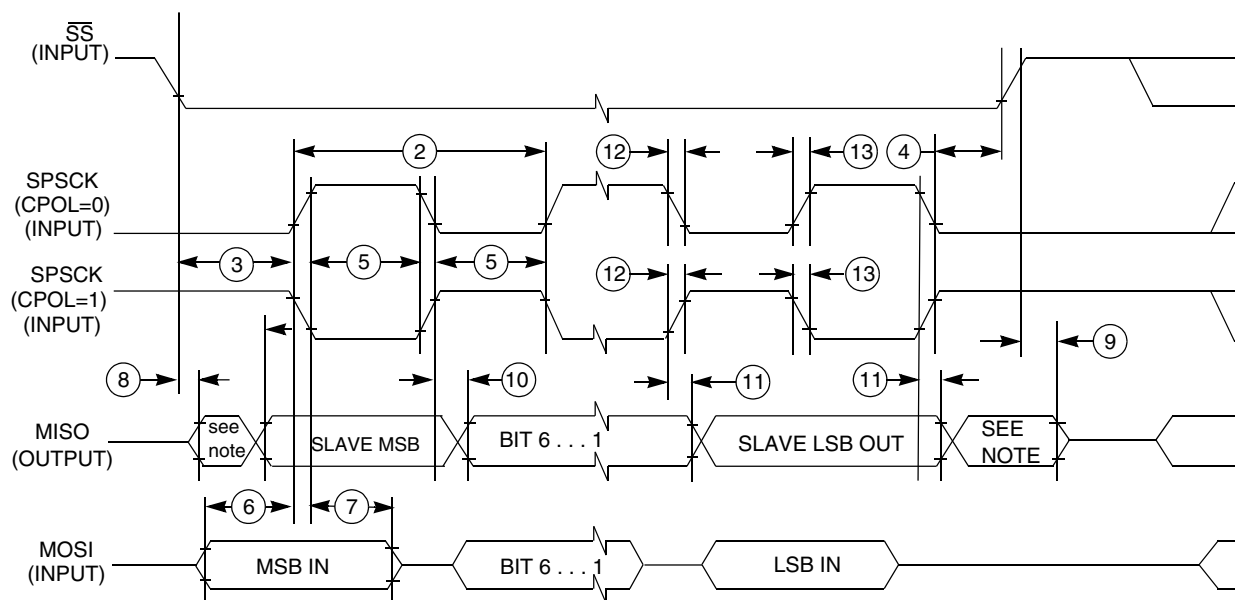
Figure 17. SPI master mode timing (CPHA=0)


1. If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. SPI master mode timing (CPHA=1)

Table 15. SPI slave mode timing

Nu m.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	0	$f_{Bus}/4$	Hz	f_{Bus} is the bus clock as defined in .
2	t_{SPSCK}	SPSCK period	$4 \times t_{Bus}$	—	ns	$t_{Bus} = 1/f_{Bus}$
3	t_{Lead}	Enable lead time	1	—	t_{Bus}	—
4	t_{Lag}	Enable lag time	1	—	t_{Bus}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	$t_{Bus} - 30$	—	ns	—
6	t_{SU}	Data setup time (inputs)	15	—	ns	—
7	t_{HI}	Data hold time (inputs)	25	—	ns	—
8	t_a	Slave access time	—	t_{Bus}	ns	Time to data active from high-impedance state
9	t_{dis}	Slave MISO disable time	—	t_{Bus}	ns	Hold time to high-impedance state
10	t_v	Data valid (after SPSCK edge)	—	25	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	$t_{Bus} - 25$	ns	—
	t_{FI}	Fall time input	—	$t_{Bus} - 25$	ns	—
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output	—	25	ns	—



NOTE: Not defined

Figure 19. SPI slave mode timing (CPHA = 0)

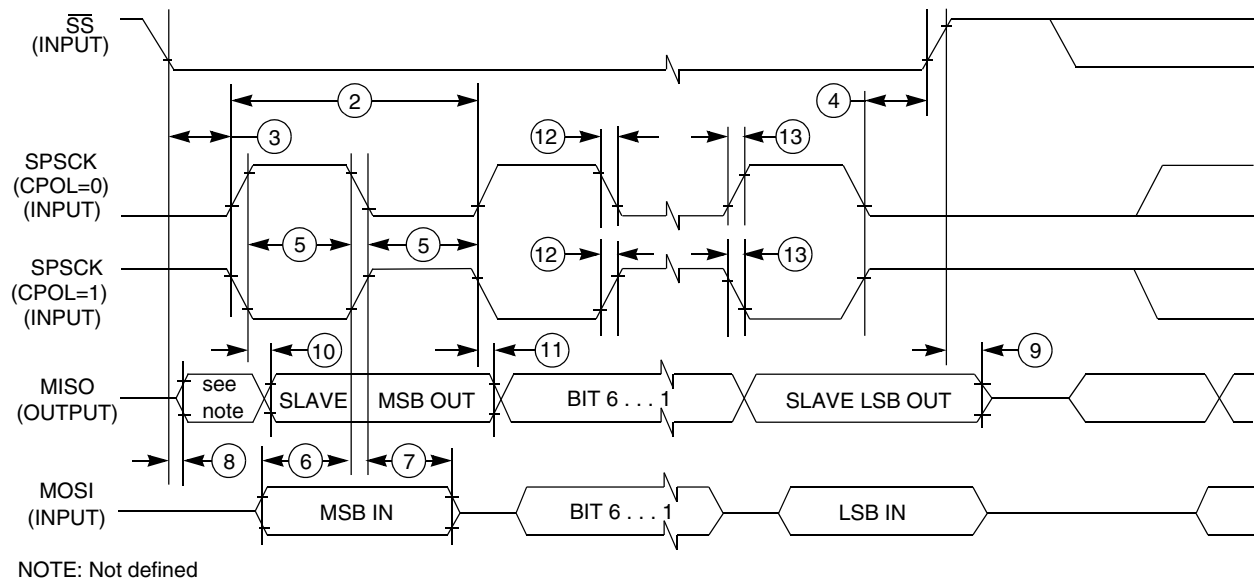


Figure 20. SPI slave mode timing (CPHA=1)

6.5 Human-machine interfaces (HMI)

6.5.1 TSI electrical specifications

Table 16. TSI electrical specifications

Symbol	Description	Min.	Type	Max	Unit
TSI_RUNF	Fixed power consumption in run mode	—	100	—	μA
TSI_RUNV	Variable power consumption in run mode (depends on oscillator's current selection)	1.0	—	128	μA
TSI_EN	Power consumption in enable mode	—	100	—	μA
TSI_DIS	Power consumption in disable mode	—	1.2	—	μA
TSI_TEN	TSI analog enable time	—	66	—	μs
TSI_CREF	TSI reference capacitor	—	1.0	—	pF
TSI_DVOLT	Voltage variation of VP & VM around nominal values	-10	—	10	%

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

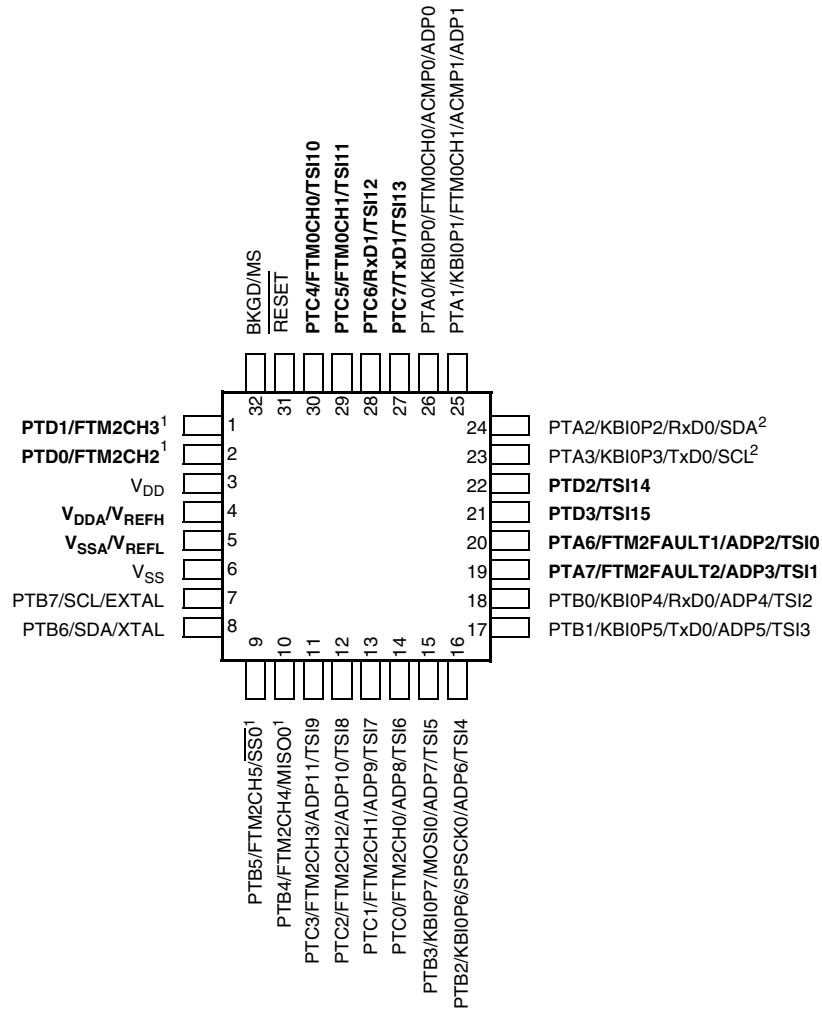
Table 17. Pin availability by package pin-count (continued)

Pin Number				Lowest Priority <-- --> Highest				
48-LQFP	32-LQFP	20-TSSOP	16-TSSOP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
19	—	—	—	PTD6	—	—	—	—
20	—	—	—	PTD5	—	—	—	—
21	13	11	—	PTC1	—	FTM2CH1	ADP9	TSI7
22	14	12	—	PTC0	—	FTM2CH0	ADP8	TSI6
23	15	13	9	PTB3	KBI0P7	MOSI0	ADP7	TSI5
24	16	14	10	PTB2	KBI0P6	SPSCK0	ADP6	TSI4
25	17	15	11	PTB1	KBI0P5	TXD0	ADP5	TSI3
26	18	16	12	PTB0	KBI0P4	RXD0	ADP4	TSI2
27	19	—	—	PTA7	—	FTM2FAULT2	ADP3	TSI1
28	20	—	—	PTA6	—	FTM2FAULT1	ADP2	TSI0
29	—	—	—	NC				
30	—	—	—	—	—	—	—	V _{ss}
31	—	—	—	—	—	—	—	V _{DD}
32	—	—	—	PTD4	—	—	—	—
33	21	—	—	PTD3	—	—	—	TSI15
34	22	—	—	PTD2	—	—	—	TSI14
35	23	17	13	PTA3 ²	KBI0P3	TXD0	SCL	—
36	24	18	14	PTA2 ²	KBI0P2	RXD0	SDA	—
37	25	19	15	PTA1	KBI0P1	FTM0CH1	ACMP1	ADP1
38	26	20	16	PTA0	KBI0P0	FTM0CH0	ACMP0	ADP0
39	27	—	—	PTC7	—	TxD1	—	TSI13
40	28	—	—	PTC6	—	RxD1	—	TSI12
41	—	—	—	NC				
42	—	—	—	PTE2	—	MISO0	—	—
43	—	—	—	PTE1	—	MOSI0	—	—
44	—	—	—	PTE0	—	SPSCK0	—	—
45	29	—	—	PTC5	—	FTM0CH1	—	TSI11
46	30	—	—	PTC4	—	FTM0CH0	—	TSI10
47	31	1	1	—	—	—	—	RESET
48	32	2	2	—	—	—	BKGD	MS

1. This is a high current drive pin when operated as output.
2. This is a true open-drain pin when operated as output.

Note

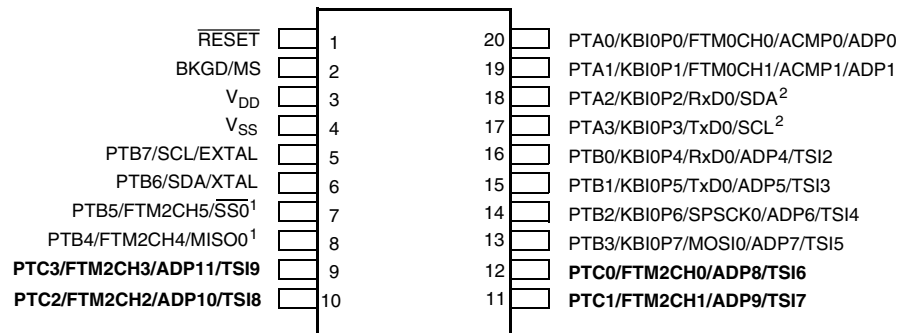
When an alternative function is first enabled, it is possible to get a spurious edge to the module. User software must clear any associated flags before interrupts are enabled. The table above illustrates the priority if multiple modules are enabled. The



Pins in **bold** are not available on less pin-count packages.

1. High source/sink current pins
2. True open drain pins

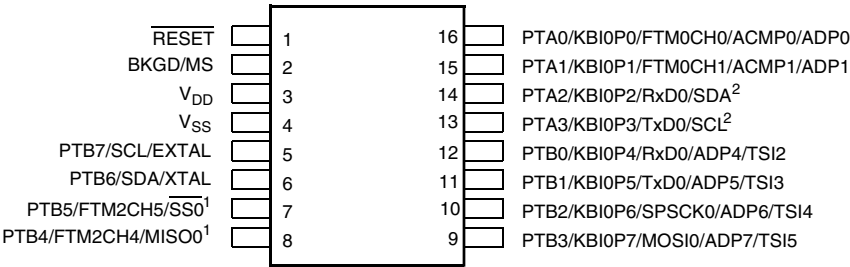
Figure 22. S9S08RN16 32-pin LQFP package



Pins in **bold** are not available on less pin-count packages.

1. High source/sink current pins
2. True open drain pins

Figure 23. S9S08RN16 20-pin TSSOP package



1. High source/sink current pins
2. True open drain pins

Figure 24. S9S08RN16 16-pin TSSOP package

9 Revision history

The following table provides a revision history for this document.

Table 18. Revision history

Rev. No.	Date	Substantial Changes
1	02/2014	Initial Release

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