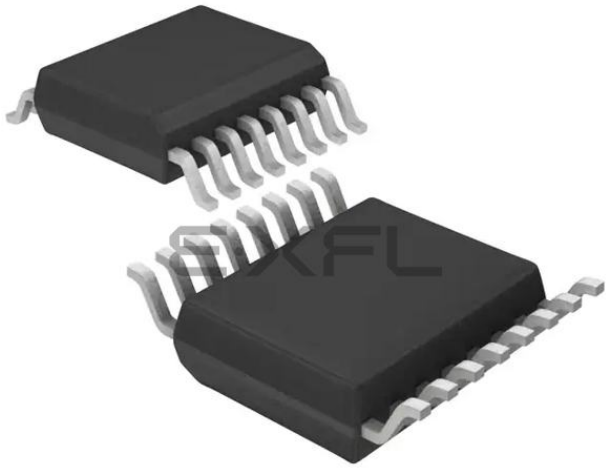

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	12
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	16-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s08rna16w2mtg

- Peripherals
  - ACMP - one analog comparator with both positive and negative inputs; separately selectable interrupt on rising and falling comparator output; filtering
  - ADC - 12-channel, 12-bit resolution for 48-, 32-pin packages; 10-channel, 10-bit resolution for 20-pin package; 8-channel, 10-bit for 16-pin package; 2.5 µs conversion time; data buffers with optional watermark; automatic compare function; internal bandgap reference channel; operation in stop mode; optional hardware trigger
  - CRC - programmable cyclic redundancy check module
  - FTM - two flex timer modulators modules including one 6-channel and one 2-channel ones; 16-bit counter; each channel can be configured for input capture, output compare, edge- or center-aligned PWM mode
  - IIC - One inter-integrated circuit module; up to 400 kbps; multi-master operation; programmable slave address; supporting broadcast mode and 10-bit addressing
  - MTIM - One modulo timer with 8-bit prescaler and overflow interrupt
  - RTC - 16-bit real time counter (RTC)
  - SCI - two serial communication interface (SCI/UART) modules optional 13-bit break; full duplex non-return to zero (NRZ); LIN extension support
  - SPI - one 8-bit serial peripheral interface (SPI) modules; full-duplex or single-wire bidirectional; master or slave mode
  - TSI - supporting up to 16 external electrodes; configurable software or hardware scan trigger; fully support freescale touch sensing software library; capability to wake MCU from stop3 mode
- Input/Output
  - Up to 35 GPIOs including one output-only pin
  - One 8-bit keyboard interrupt module (KBI)
  - Two true open-drain output pins
  - Four, ultra-high current sink pins supporting 20 mA source/sink current
- Package options
  - 48-pin LQFP
  - 32-pin LQFP
  - 20-pin TSSOP
  - 16-pin TSSOP

Table of Contents

2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-6000	+6000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 125°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78D, IC Latch-up Test.
   - Test was performed at 125 °C case temperature (Class II).
   - I/O pins pass +100/-100 mA I-test with Idd current limit at 400mA.
   - I/O pins pass +20/-100 mA I-test with Idd current limit at 1000mA.
   - Supply groups pass 1.5 Vccmax.
   - RESET_B pin was only tested with negative I-test due to product conditioning requirement.

4.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in below table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

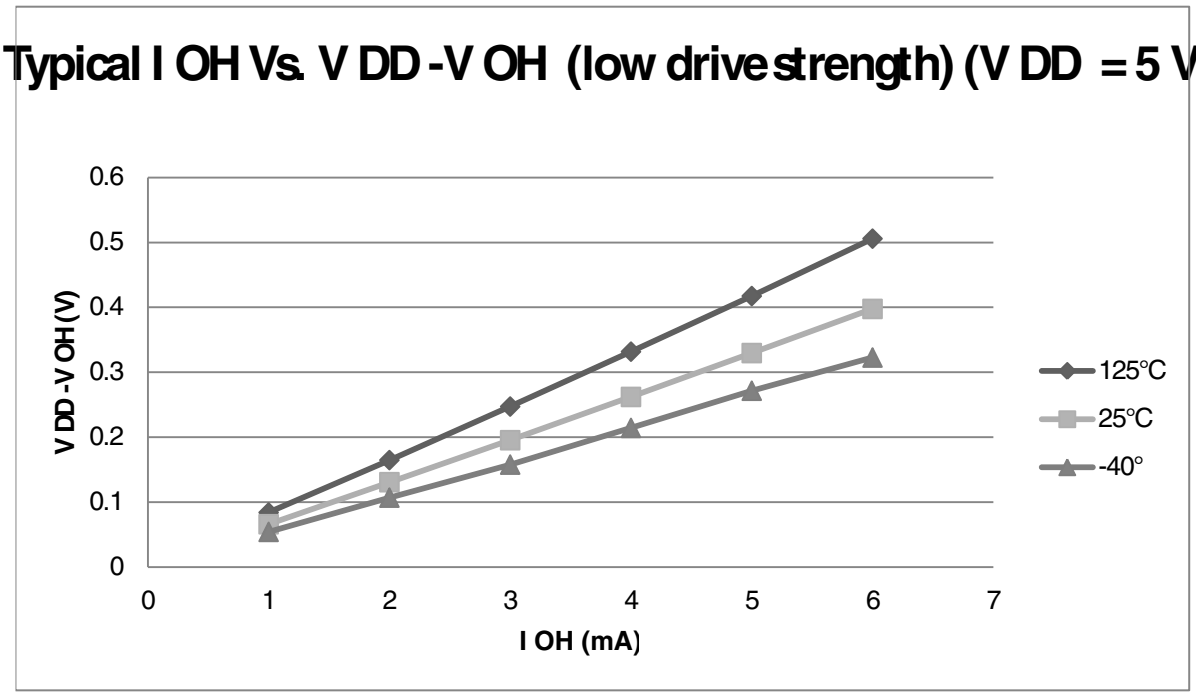


Figure 1. Typical I_{OH} Vs. V_{DD}-V_{OH} (standard drive strength) (V_{DD} = 5 V)

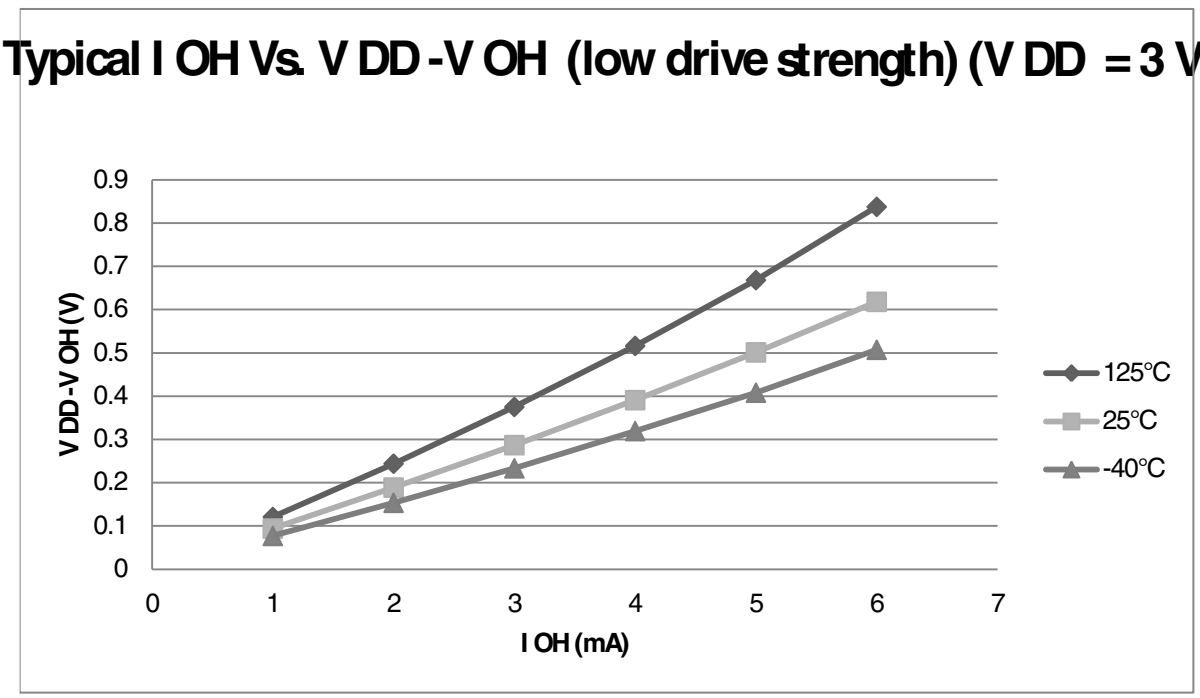


Figure 2. Typical I_{OH} Vs. V_{DD}-V_{OH} (standard drive strength) (V_{DD} = 3 V)

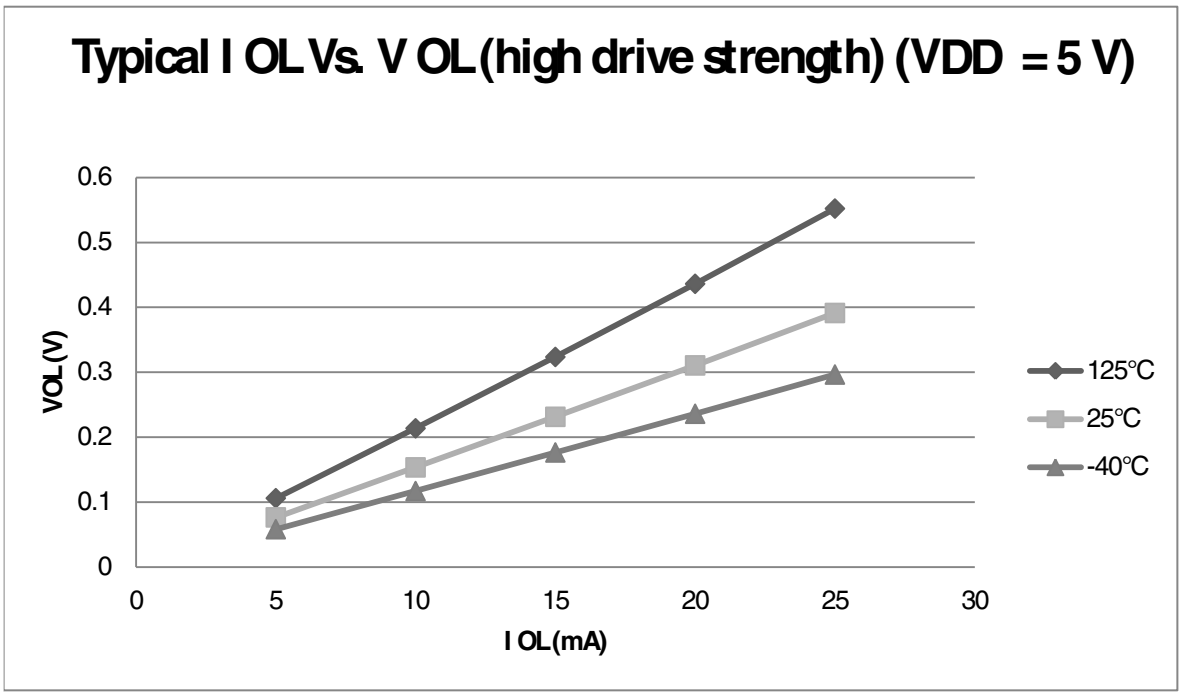


Figure 7. Typical I_{OL} Vs. V_{OL} (high drive strength) (V_{DD} = 5 V)

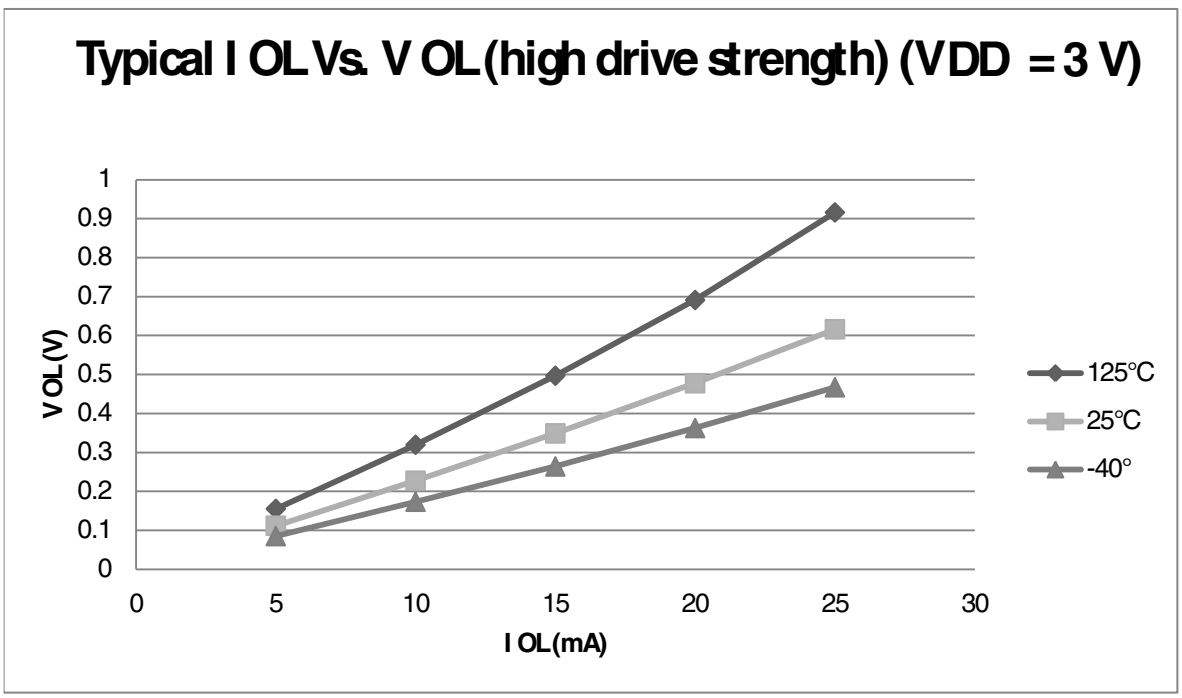


Figure 8. Typical I_{OL} Vs. V_{OL} (high drive strength) (V_{DD} = 3 V)

5.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 4. Supply current characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp
1	C	Run supply current FEI mode, all modules on; run from flash	RI_{DD}	20 MHz	5	7.60	—	mA	-40 to 125 °C
	C			10 MHz		4.65	—		
				1 MHz		1.90	—		
	C			20 MHz	3	7.05	—		
	C			10 MHz		4.40	—		
				1 MHz		1.85	—		
2	C	Run supply current FEI mode, all modules off & gated; run from flash	RI_{DD}	20 MHz	5	5.88	—	mA	-40 to 125 °C
	C			10 MHz		3.70	—		
				1 MHz		1.85	—		
	C			20 MHz	3	5.35	—		
	C			10 MHz		3.42	—		
				1 MHz		1.80	—		
3	P	Run supply current FBE mode, all modules on; run from RAM	RI_{DD}	20 MHz	5	10.9	14.0	mA	-40 to 125 °C
	C			10 MHz		6.10	—		
				1 MHz		1.69	—		
	C			20 MHz	3	8.18	—		
				10 MHz		5.14	—		
				1 MHz		1.44	—		
4	P	Run supply current FBE mode, all modules off & gated; run from RAM	RI_{DD}	20 MHz	5	8.50	13.0	mA	-40 to 125 °C
	C			10 MHz		5.07	—		
				1 MHz		1.59	—		
	C			20 MHz	3	6.11	—		
				10 MHz		4.10	—		
				1 MHz		1.34	—		
5	C	Wait mode current FEI mode, all modules on	WI_{DD}	20 MHz	5	5.95	—	mA	-40 to 125 °C
				10 MHz		3.50	—		
				1 MHz		1.24	—		
	C			20 MHz	3	5.45	—		
				10 MHz		3.25	—		
				1 MHz		1.20	—		
6	C	Stop3 mode supply current no clocks active (except 1kHz LPO clock)[2, 3]	$S3I_{DD}$	—	5	4.6	—	µA	-40 to 125 °C
	C			—	3	4.5	—		-40 to 125 °C
7	C	ADC adder to stop3	—	—	5	40	—	µA	-40 to 125 °C

Table continues on the next page...

Table 4. Supply current characteristics (continued)

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp
	C	ADLPC = 1 ADLSMP = 1 ADCO = 1 MODE = 10B ADICLK = 11B			3	39	—		
8	C	TSI adder to stop3[4]	—	—	5	121	—	µA	-40 to 125 °C
	C	PS = 010B NSCN = 0x0F EXTCHRG = 0 REFCHRG = 0 DVOLT = 01B			3	120	—		
9	C	LVD adder to stop3[5]	—	—	5	128	—	µA	-40 to 125 °C
	C				3	124	—		

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. RTC adder cause <1 µA I_{DD} increase typically, RTC clock source is 1kHz LPO clock.
3. ACMP adder cause <10 µA I_{DD} increase typically.
4. The current varies with TSI configuration and capacity of touch electrode. Please refer toTSI electrical specifications.
5. LVD is periodically woken up from stop3 by 5% duty cycle. The period is equal to or less than 2 ms.

5.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

5.2 Switching specifications

5.2.1 Control timing

Table 5. Control timing

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
1	P	Bus frequency (t_{cyc} = 1/f_{Bus})	f_{Bus}	DC	—	20	MHz
2	P	Internal low power oscillator frequency	f_{LPO}	0.67	1.0	1.25	KHz

Table continues on the next page...

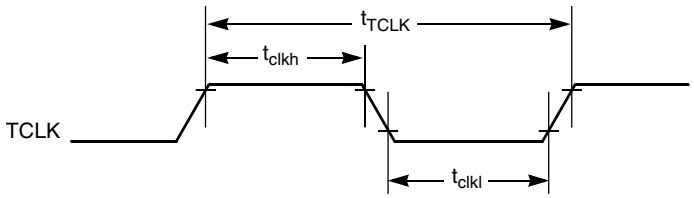


Figure 13. Timer external clock

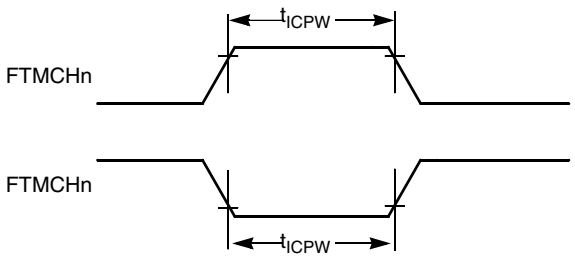


Figure 14. Timer input capture pulse

5.3 Thermal specifications

5.3.1 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 8. Thermal characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H -40 to 125	°C
Junction temperature range	T_J	-40 to 135	°C
Thermal resistance single-layer board			
48-pin LQFP	θ_{JA}	82	°C/W
32-pin LQFP	θ_{JA}	88	°C/W
20-pin TSSOP	θ_{JA}	116	°C/W
16-pin TSSOP	θ_{JA}	130	°C/W
Thermal resistance four-layer board			

Table continues on the next page...

6.1 External oscillator (XOSC) and ICS characteristics

Table 9. XOSC and ICS specifications (temperature range = -40 to 125 °C ambient)

Num	C	Characteristic		Symbol	Min	Typical[1]	Max	Unit
1	C	Oscillator crystal or resonator	Low range (RANGE = 0)	f_{lo}	32	—	40	kHz
	C		High range (RANGE = 1) FEE or FBE mode[2]	f_{hi}	4	—	20	MHz
	C		High range (RANGE = 1), high gain (HGO = 1), FBELP mode	f_{hi}	4	—	20	MHz
	C		High range (RANGE = 1), low power (HGO = 0), FBELP mode	f_{hi}	4	—	20	MHz
2	D	Load capacitors		C1, C2	See Note[3]			
3	D	Feedback resistor	Low Frequency, Low-Power Mode[4]	R_F	—	—	—	MΩ
			Low Frequency, High-Gain Mode		—	10	—	MΩ
			High Frequency, Low-Power Mode		—	1	—	MΩ
			High Frequency, High-Gain Mode		—	1	—	MΩ
4	D	Series resistor - Low Frequency	Low-Power Mode [4]	R_S	—	—	—	kΩ
			High-Gain Mode		—	200	—	kΩ
5	D	Series resistor - High Frequency	Low-Power Mode[4]	R_S	—	—	—	kΩ
	D	Series resistor - High Frequency, High-Gain Mode	4 MHz		—	0	—	kΩ
	D		8 MHz		—	0	—	kΩ
	D		16 MHz		—	0	—	kΩ
6	C	Crystal start-up time Low range = 39.0625 kHz crystal; High range = 20 MHz crystal[5, 6]	Low range, low power	t_{CSTL}	—	1000	—	ms
	C		Low range, high power		—	800	—	ms
	C		High range, low power	t_{CSTH}	—	3	—	ms
	C		High range, high power		—	1.5	—	ms
7	T	Internal reference start-up time		t_{IRST}	—	20	50	µs
8	D	Square wave input clock frequency	FEE or FBE mode[2]	f_{extal}	0.03125	—	5	MHz
	D		FBELP mode		0	—	20	MHz
9	P	Average internal reference frequency - trimmed		f_{int_t}	—	39.0625	—	kHz
10	P	DCO output frequency range - trimmed		f_{dco_t}	16	—	20	MHz
11	P	Total deviation of DCO output from trimmed frequency[5]	Over full voltage range and temperature range of -40 to 125 °C	Δf_{dco_t}	—	—	±2.0	
	C		Over full voltage range and temperature range of -40 to 105 °C				±1.5	$\%f_{dco}$

Table continues on the next page...

Table 9. XOSC and ICS specifications (temperature range = -40 to 125 °C ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
	C	Over fixed voltage and temperature range of 0 to 70 °C				±1.0	
12	C	FLL acquisition time[5, 7]	$t_{Acquire}$	—	—	2	ms
13	C	Long term jitter of DCO output clock (averaged over 2 ms interval)[8]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. When ICS is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.
3. See crystal or resonator manufacturer's recommendation.
4. Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.
5. This parameter is characterized and not tested on each device.
6. Proper PC board layout procedures must be followed to achieve specifications.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

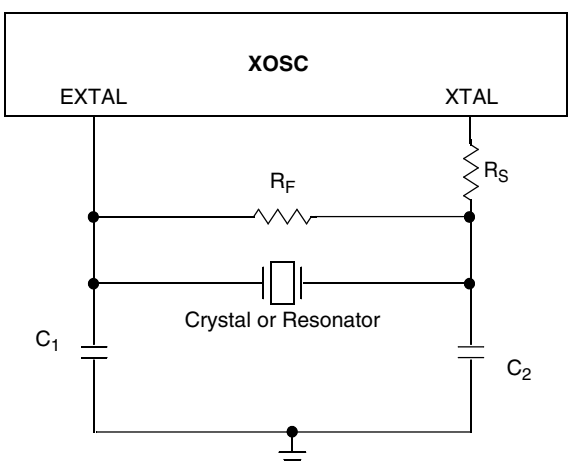


Figure 15. Typical crystal or resonator circuit

6.2 NVM specifications

This section provides details about program/erase times and program/erase endurance for the flash and EEPROM memories.

Table 10. Flash characteristics

C	Characteristic	Symbol	Min[1]	Typical[2]	Max[3]	Unit[4]
D	Supply voltage for program/erase -40 °C to 125 °C	$V_{prog/erase}$	2.7	—	5.5	V
D	Supply voltage for read operation	V_{Read}	2.7	—	5.5	V
D	NVM Bus frequency	f_{NVMBUS}	1	—	25	MHz
D	NVM Operating frequency	f_{NVMOP}	0.8	1	1.05	MHz
D	Erase Verify All Blocks	t_{VFYALL}	—	—	17338	t_{cyc}
D	Erase Verify Flash Block	t_{RD1BLK}	—	—	16913	t_{cyc}
D	Erase Verify EEPROM Block	t_{RD1BLK}	—	—	810	t_{cyc}
D	Erase Verify Flash Section	t_{RD1SEC}	—	—	484	t_{cyc}
D	Erase Verify EEPROM Section	$t_{DRD1SEC}$	—	—	555	t_{cyc}
D	Read Once	t_{RDONCE}	—	—	450	t_{cyc}
D	Program Flash (2 word)	t_{PGM2}	0.12	0.12	0.29	ms
D	Program Flash (4 word)	t_{PGM4}	0.20	0.21	0.46	ms
D	Program Once	$t_{PGMONCE}$	0.20	0.21	0.21	ms
D	Program EEPROM (1 Byte)	t_{DPGM1}	0.10	0.10	0.27	ms
D	Program EEPROM (2 Byte)	t_{DPGM2}	0.17	0.18	0.43	ms
D	Program EEPROM (3 Byte)	t_{DPGM3}	0.25	0.26	0.60	ms
D	Program EEPROM (4 Byte)	t_{DPGM4}	0.32	0.33	0.77	ms
D	Erase All Blocks	t_{ERSALL}	96.01	100.78	101.49	ms
D	Erase Flash Block	t_{ERSBLK}	95.98	100.75	101.44	ms
D	Erase Flash Sector	t_{ERSPG}	19.10	20.05	20.08	ms
D	Erase EEPROM Sector	t_{DERSPG}	4.81	5.05	20.57	ms
D	Unsecure Flash	t_{UNSECU}	96.01	100.78	101.48	ms
D	Verify Backdoor Access Key	t_{VFYKEY}	—	—	464	t_{cyc}
D	Set User Margin Level	t_{MLOADU}	—	—	407	t_{cyc}
C	FLASH Program/erase endurance T_L to T_H = -40 °C to 125 °C	n_{FLPE}	10 k	100 k	—	Cycles
C	EEPROM Program/erase endurance TL to TH = -40 °C to 125 °C	n_{FLPE}	50 k	500 k	—	Cycles
C	Data retention at an average junction temperature of T_{Javg} = 85°C after up to 10,000 program/erase cycles	t_{D_ret}	15	100	—	years

1. Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}
2. Typical times are based on typical f_{NVMOP} and maximum f_{NVMBUS}
3. Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging
4. $t_{cyc} = 1 / f_{NVMBUS}$

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

6.3 Analog

6.3.1 ADC characteristics

Table 11. 5 V 12-bit ADC operating conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	—
	Delta to V_{DD} (V_{DD}-V_{DDAD})	ΔV_{DDA}	-100	0	+100	mV	
Ground voltage	Delta to V_{SS} (V_{SS}-V_{SSA})[2]	ΔV_{SSA}	-100	0	+100	mV	
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input resistance		R_{ADIN}	—	3	5	kΩ	—
Analog source resistance	12-bit mode • f_{ADCK} > 4 MHz • f_{ADCK} < 4 MHz	R_{AS}	— —	— —	2 5	kΩ	External to MCU
	10-bit mode • f_{ADCK} > 4 MHz • f_{ADCK} < 4 MHz		— —	— —	5 10		
	8-bit mode (all valid f_{ADCK})		—	—	10		
ADC conversion clock frequency	High speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	—
	Low power (ADLPC=1)		0.4	—	4.0		

1. Typical values assume V_{DDA} = 5.0 V, Temp = 25°C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.

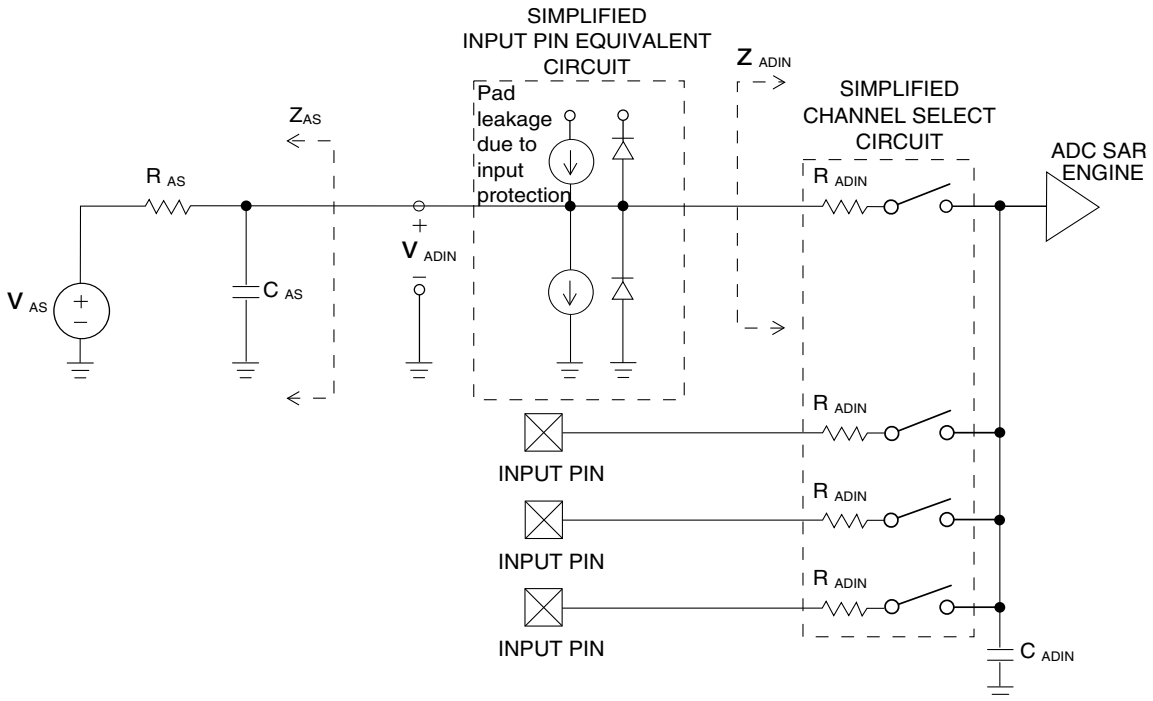


Figure 16. ADC input impedance equivalency diagram

Table 12. 12-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit
Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	133	—	µA
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		T	I_{DDA}	—	218	—	µA
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	327	—	µA
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		T	I_{DDAD}	—	582	990	µA
Supply current	Stop, reset, module off	T	I_{DDA}	—	0.011	1	µA
ADC asynchronous clock source	High speed (ADLPC = 0)	P	f_{ADACK}	2	3.3	5	MHz

Table continues on the next page...

6.3.2 Analog comparator (ACMP) electricals

Table 13. Comparator electrical specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{DDA}	2.7	—	5.5	V
T	Supply current (Operation mode)	I_{DDA}	—	10	20	µA
D	Analog input voltage	V_{AIN}	V_{SS} - 0.3	—	V_{DDA}	V
P	Analog input offset voltage	V_{AIO}	—	—	40	mV
C	Analog comparator hysteresis (HYST=0)	V_H	—	15	20	mV
C	Analog comparator hysteresis (HYST=1)	V_H	—	20	30	mV
T	Supply current (Off mode)	I_{DDAOFF}	—	60	—	nA
C	Propagation Delay	t_D	—	0.4	1	µs

6.4 Communication interfaces

6.4.1 SPI switching specifications

The serial peripheral interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. Refer to the SPI chapter of the chip's reference manual for information about the modified transfer formats used for communicating with slower peripheral devices. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless noted, and 100 pF load on all SPI pins. All timing assumes slew rate control is disabled and high drive strength is enabled for SPI output pins.

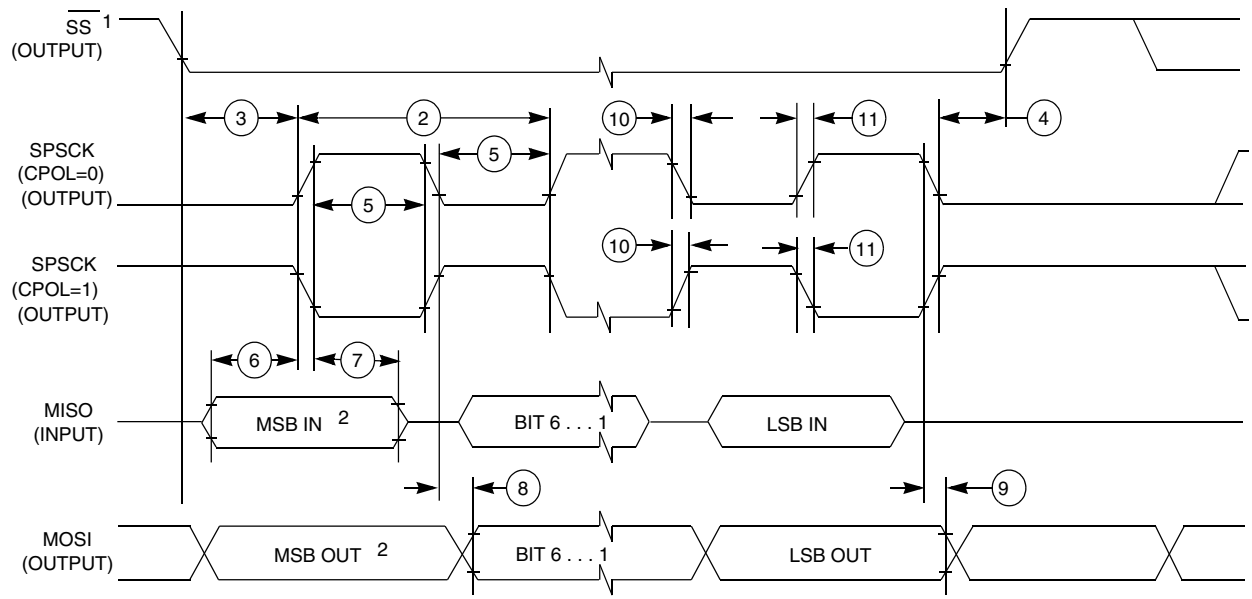
Table 14. SPI master mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	$f_{Bus}/2048$	$f_{Bus}/2$	Hz	f_{Bus} is the bus clock
2	t_{SPSCK}	SPSCK period	2 x t_{Bus}	2048 x t_{Bus}	ns	$t_{Bus} = 1/f_{Bus}$
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{Bus} - 30	1024 x t_{Bus}	ns	—
6	t_{SU}	Data setup time (inputs)	15	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_v	Data valid (after SPSCK edge)	—	25	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{Bus} - 25	ns	—

Table continues on the next page...

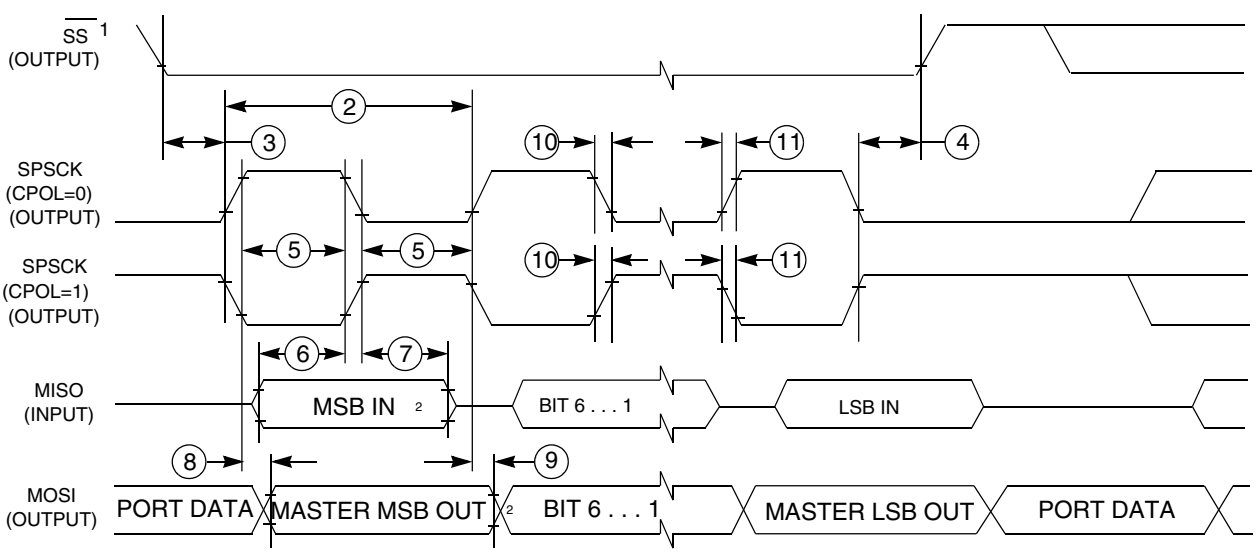
Table 14. SPI master mode timing (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Comment
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 17. SPI master mode timing (CPHA=0)



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. SPI master mode timing (CPHA=1)

Table 15. SPI slave mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	0	$f_{Bus}/4$	Hz	f_{Bus} is the bus clock as defined in .
2	t_{SPSCK}	SPSCK period	4 x t_{Bus}	—	ns	$t_{Bus} = 1/f_{Bus}$
3	t_{Lead}	Enable lead time	1	—	t_{Bus}	—
4	t_{Lag}	Enable lag time	1	—	t_{Bus}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{Bus} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	15	—	ns	—
7	t_{HI}	Data hold time (inputs)	25	—	ns	—
8	t_a	Slave access time	—	t_{Bus}	ns	Time to data active from high-impedance state
9	t_{dis}	Slave MISO disable time	—	t_{Bus}	ns	Hold time to high-impedance state
10	t_v	Data valid (after SPSCK edge)	—	25	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{Bus} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

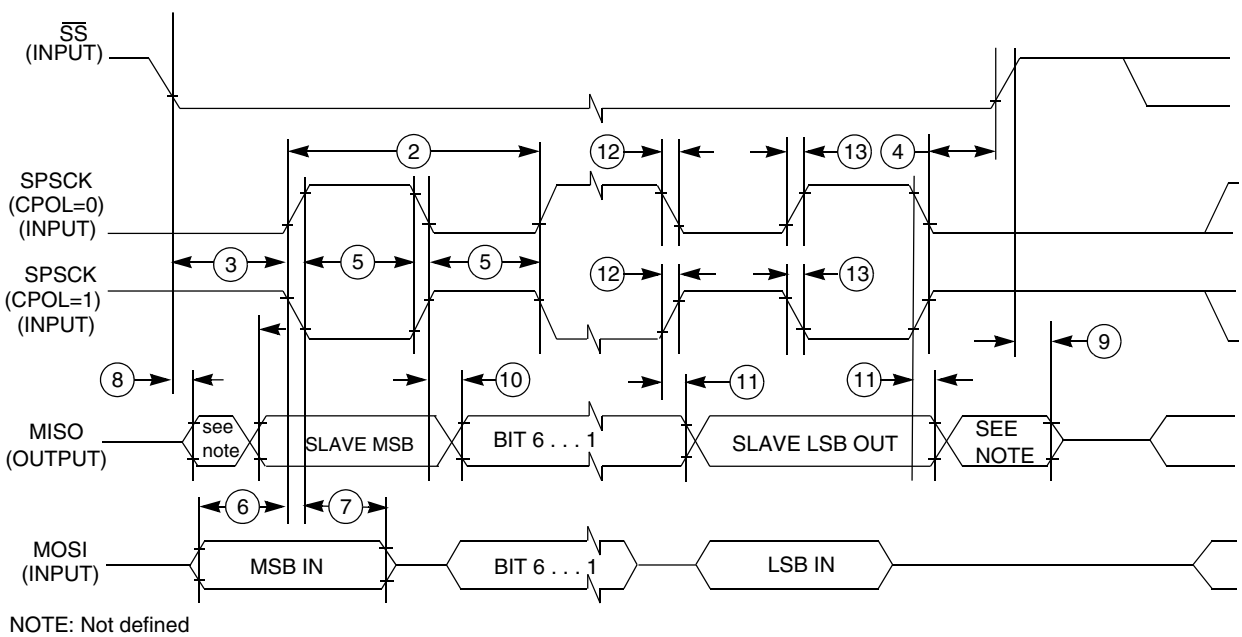
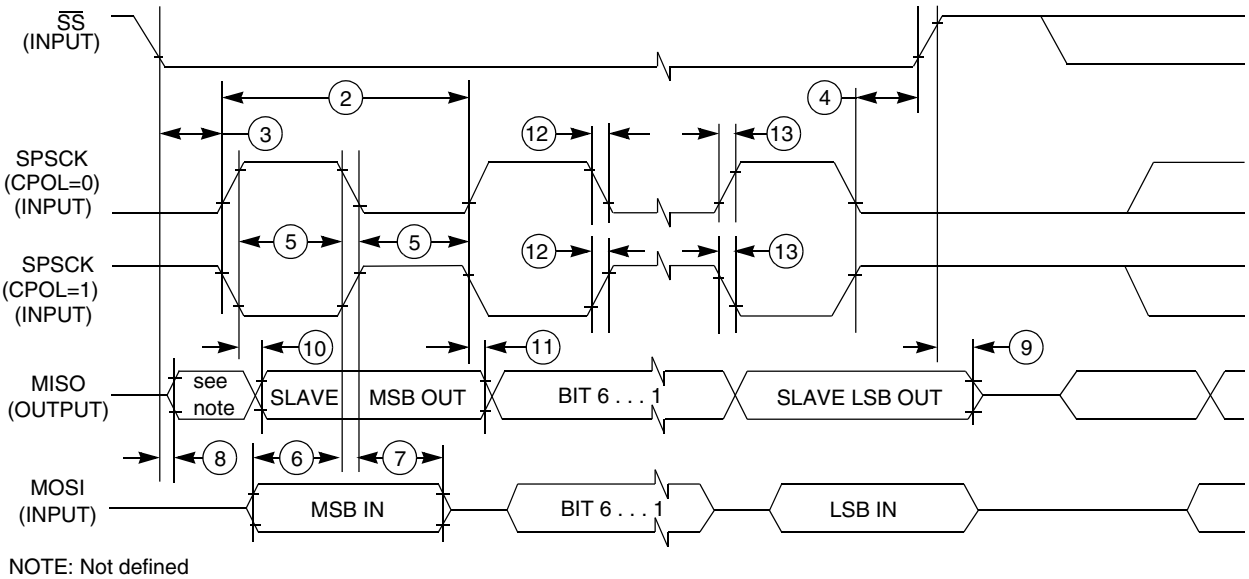


Figure 19. SPI slave mode timing (CPHA = 0)



NOTE: Not defined

Figure 20. SPI slave mode timing (CPHA=1)

6.5 Human-machine interfaces (HMI)

6.5.1 TSI electrical specifications

Table 16. TSI electrical specifications

Symbol	Description	Min.	Type	Max	Unit
TSI_RUNF	Fixed power consumption in run mode	—	100	—	µA
TSI_RUNV	Variable power consumption in run mode (depends on oscillator's current selection)	1.0	—	128	µA
TSI_EN	Power consumption in enable mode	—	100	—	µA
TSI_DIS	Power consumption in disable mode	—	1.2	—	µA
TSI_TEN	TSI analog enable time	—	66	—	µs
TSI_CREF	TSI reference capacitor	—	1.0	—	pF
TSI_DVOLT	Voltage variation of VP & VM around nominal values	-10	—	10	%

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

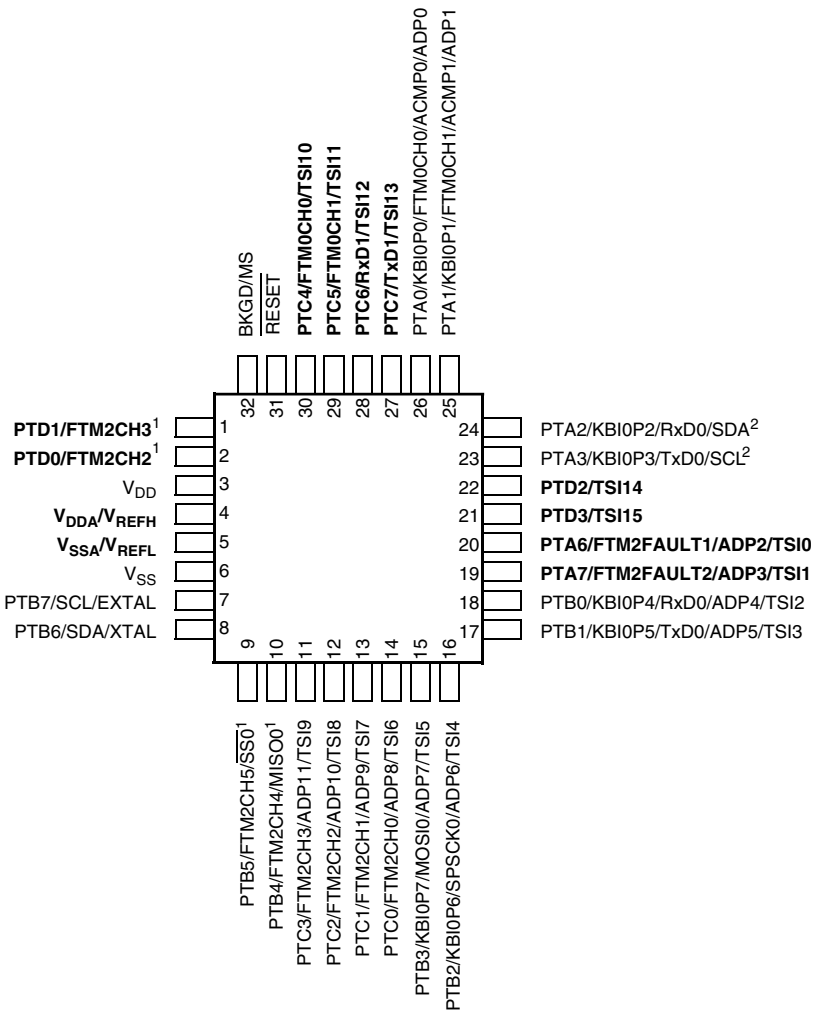
Table 17. Pin availability by package pin-count (continued)

Pin Number				Lowest Priority <-- --> Highest				
48-LQFP	32-LQFP	20-TSSOP	16-TSSOP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
19	—	—	—	PTD6	—	—	—	—
20	—	—	—	PTD5	—	—	—	—
21	13	11	—	PTC1	—	FTM2CH1	ADP9	TSI7
22	14	12	—	PTC0	—	FTM2CH0	ADP8	TSI6
23	15	13	9	PTB3	KBI0P7	MOSI0	ADP7	TSI5
24	16	14	10	PTB2	KBI0P6	SPSCK0	ADP6	TSI4
25	17	15	11	PTB1	KBI0P5	TXD0	ADP5	TSI3
26	18	16	12	PTB0	KBI0P4	RXD0	ADP4	TSI2
27	19	—	—	PTA7	—	FTM2FAULT2	ADP3	TSI1
28	20	—	—	PTA6	—	FTM2FAULT1	ADP2	TSI0
29	—	—	—	NC				
30	—	—	—	—	—	—	—	Vss
31	—	—	—	—	—	—	—	V_{DD}
32	—	—	—	PTD4	—	—	—	—
33	21	—	—	PTD3	—	—	—	TSI15
34	22	—	—	PTD2	—	—	—	TSI14
35	23	17	13	PTA3[2]	KBI0P3	TXD0	SCL	—
36	24	18	14	PTA2[2]	KBI0P2	RXD0	SDA	—
37	25	19	15	PTA1	KBI0P1	FTM0CH1	ACMP1	ADP1
38	26	20	16	PTA0	KBI0P0	FTM0CH0	ACMP0	ADP0
39	27	—	—	PTC7	—	TxD1	—	TSI13
40	28	—	—	PTC6	—	RxD1	—	TSI12
41	—	—	—	NC				
42	—	—	—	PTE2	—	MISO0	—	—
43	—	—	—	PTE1	—	MOSI0	—	—
44	—	—	—	PTE0	—	SPSCK0	—	—
45	29	—	—	PTC5	—	FTM0CH1	—	TSI11
46	30	—	—	PTC4	—	FTM0CH0	—	TSI10
47	31	1	1	—	—	—	—	$\overline{\text{RESET}}$
48	32	2	2	—	—	—	BKGD	MS

1. This is a high current drive pin when operated as output.
2. This is a true open-drain pin when operated as output.

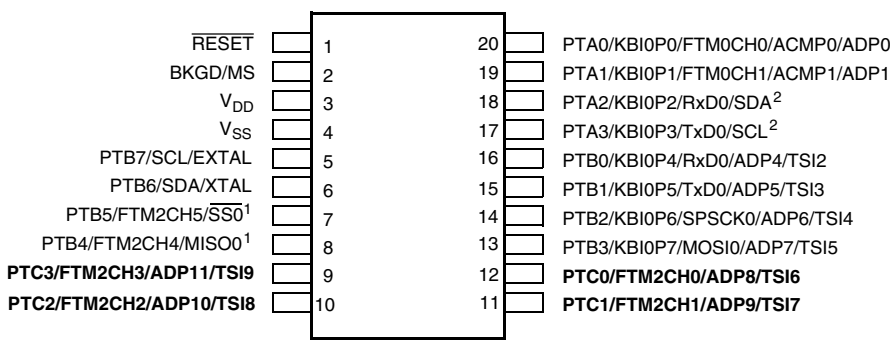
Note

When an alternative function is first enabled, it is possible to get a spurious edge to the module. User software must clear any associated flags before interrupts are enabled. The table above illustrates the priority if multiple modules are enabled. The



Pins in **bold** are not available on less pin-count packages.
1. High source/sink current pins
2. True open drain pins

Figure 22. S9S08RN16 32-pin LQFP package



Pins in **bold** are not available on less pin-count packages.
1. High source/sink current pins
2. True open drain pins

Figure 23. S9S08RN16 20-pin TSSOP package

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Document Number S9S08RN16DS
Revision 1, 02/2014