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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	nX-U8/100
Core Size	8-Bit
Speed	4.2MHz
Connectivity	I ² C, SSP, UART/USART
Peripherals	LCD, Melody Driver, POR, PWM, WDT
Number of I/O	20
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	7K x 8
Voltage - Supply (Vcc/Vdd)	1.1V ~ 3.6V
Data Converters	A/D 2x12b, 2x24b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/rohm-semi/ml610q438p-nnntc03a7

Type E : 16com x 40seg (seg63 to seg40: output port, seg39 to seg0: segment port)

Type F : 16com x 32seg (seg63 to seg32: output port, seg31 to seg0: segment port)

- Reset
 - Reset through the RESET_N pin
 - Power-on reset generation when powered on
 - Reset when oscillation stop of the low-speed clock is detected
 - Reset by the watchdog timer (WDT) overflow
- Power supply voltage detect function
 - Judgment voltages: One of 16 levels
 - Judgment accuracy: $\pm 2\%$ (Typ.)
- Clock
 - Low-speed clock: (This LSI can not guarantee the operation without low-speed clock)
Crystal oscillation (32.768 kHz)
 - High-speed clock:
Built-in RC oscillation (2M/500kHz)
Built-in PLL oscillation (8.192 MHz $\pm 2.5\%$), crystal/ceramic oscillation (4.096 MHz), external clock
 - Selection of high-speed clock mode by software:
Built-in RC oscillation, built-in PLL oscillation, crystal/ceramic oscillation, external clock
- Power management
 - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
 - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
 - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
 - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.
- Shipment
 - Chip (Die)
ML610Q438-xxxWA (Blank product: ML610Q438-NNNWA)
ML610Q438P-xxxWA (Blank product: ML610Q438P-NNNWA)
ML610Q439-xxxWA (Blank product: ML610Q439-NNNWA)
ML610Q439P-xxxWA (Blank product: ML610Q439P-NNNWA)
 - 144-pin plastic LQFP
ML610Q438-xxxTCZ03A (Blank product: ML610Q438-NNNTCZ03A)
ML610Q438P-xxxTCZ03A (Blank product: ML610Q438P-NNNTCZ03A)
ML610Q439-xxxTCZ03A (Blank product: ML610Q439-NNNTCZ03A)
ML610Q439P-xxxTCZ03A (Blank product: ML610Q439P-NNNTCZ03A)
xxx: ROM code number
- Guaranteed operating range
 - Operating temperature: -20°C to 70°C (P version : -40°C to 85°C)
 - Operating voltage: $V_{\text{DD}} = 1.1\text{V}$ to 3.6V , $AV_{\text{DD}} = 2.2\text{V}$ to 3.6V

BLOCK DIAGRAM

ML610Q438 Block Diagram

Figure 1 show the block diagram of the ML610Q438.

"*" indicates the secondary function of each port.

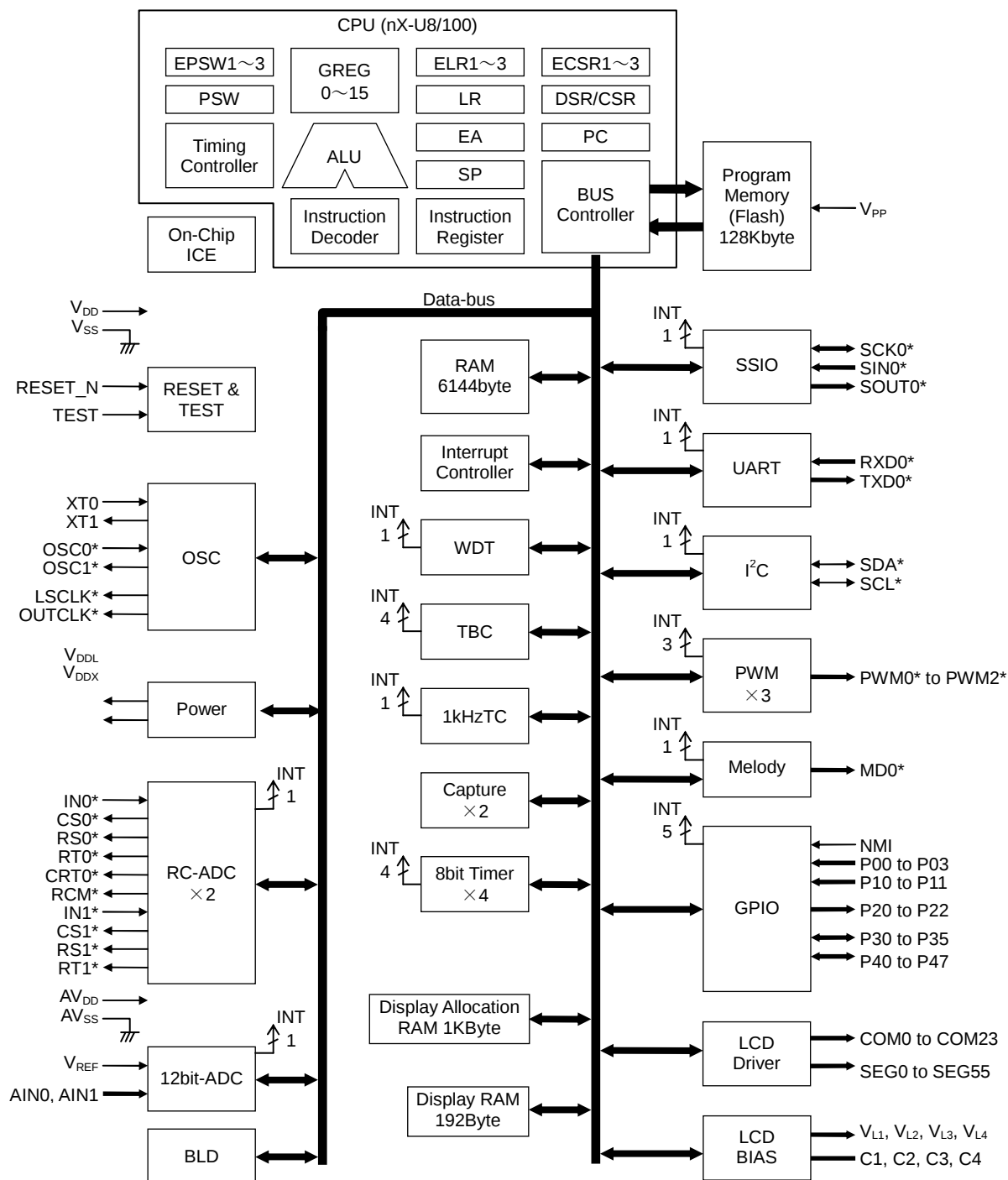


Figure 1 ML610Q438 Block Diagram

ML610Q439 Block Diagram

Figure 2 show the block diagram of the ML610Q439.

"*" indicates the secondary function of each port.

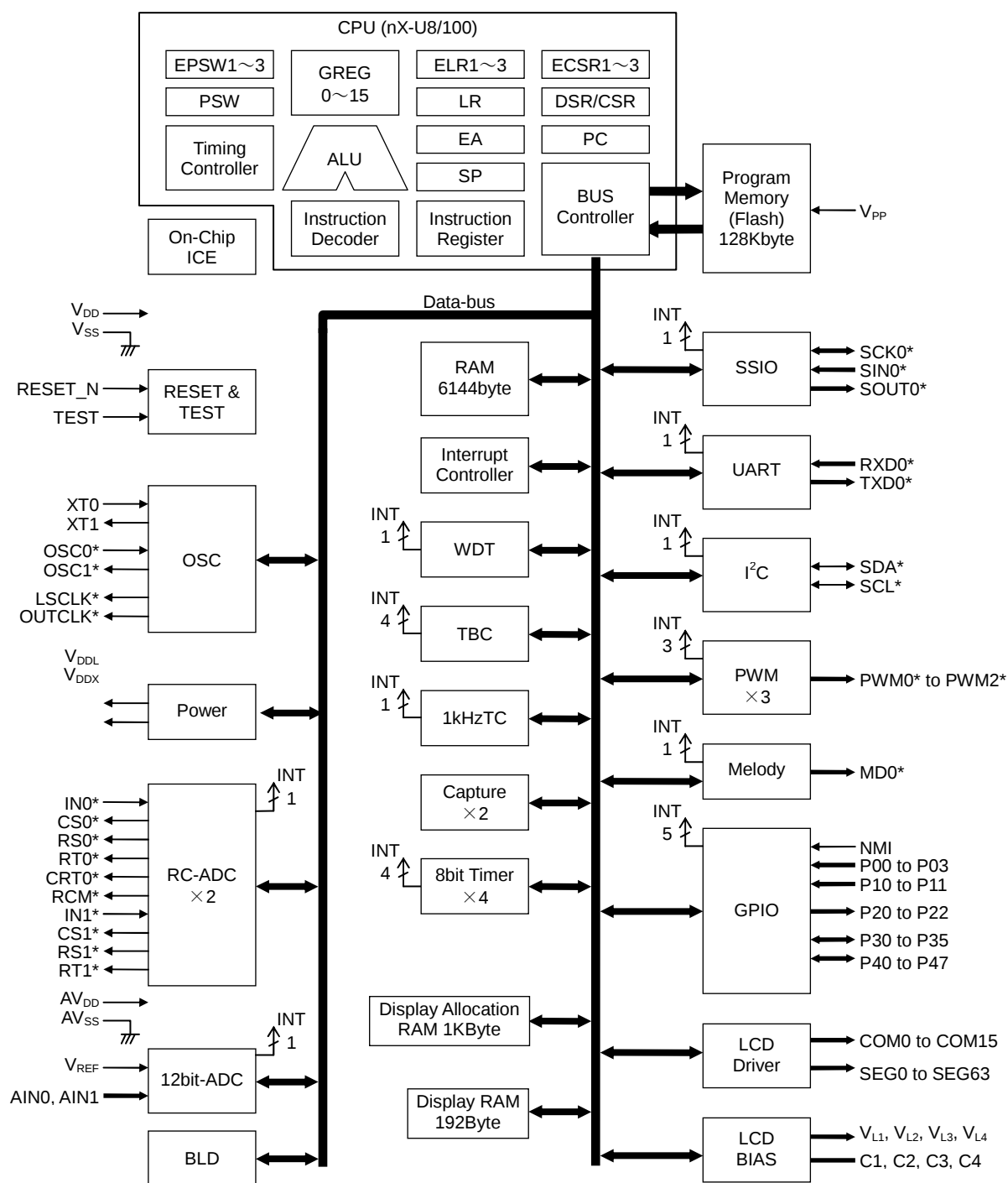
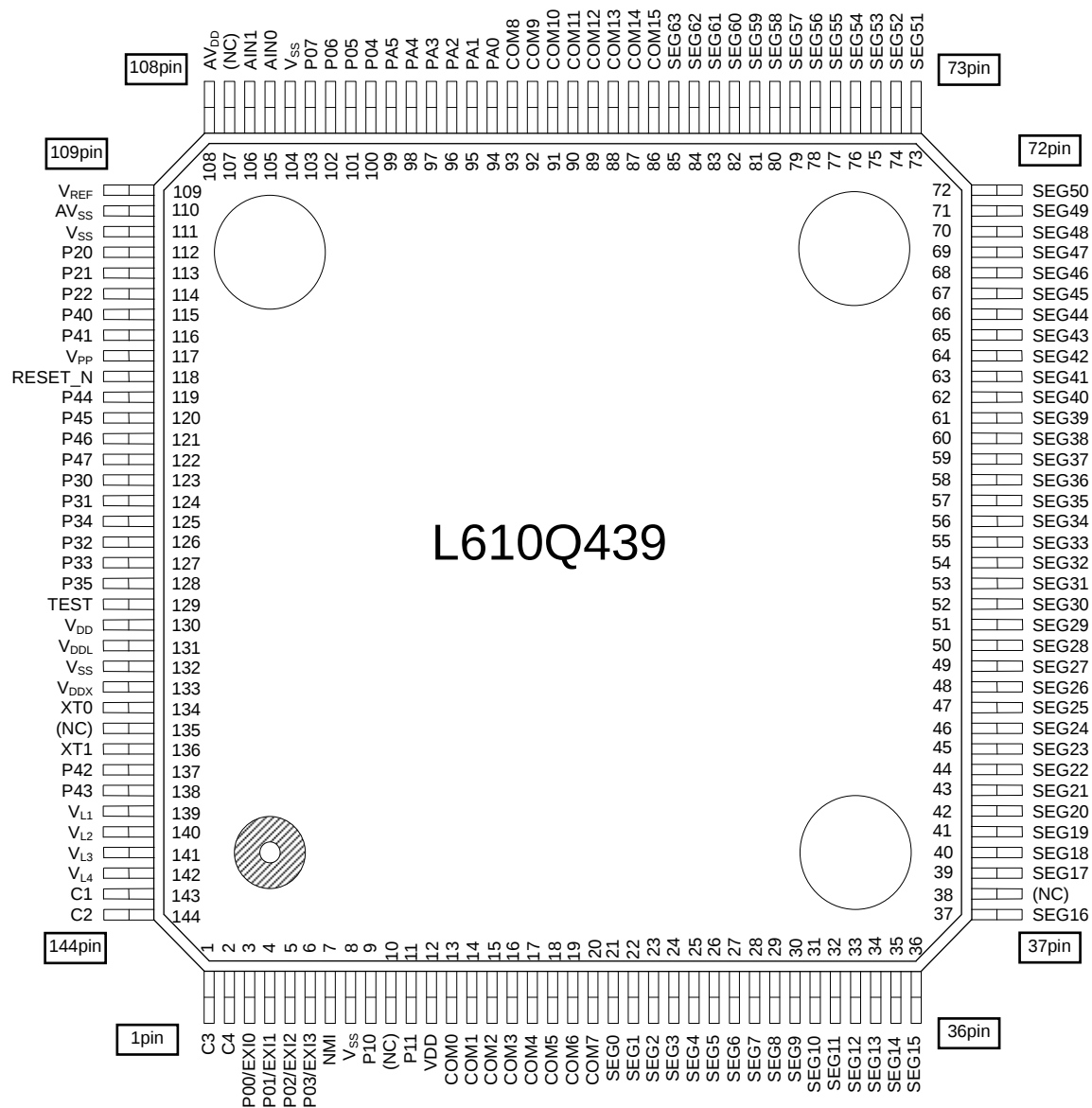


Figure 2 ML610Q439 Block Diagram

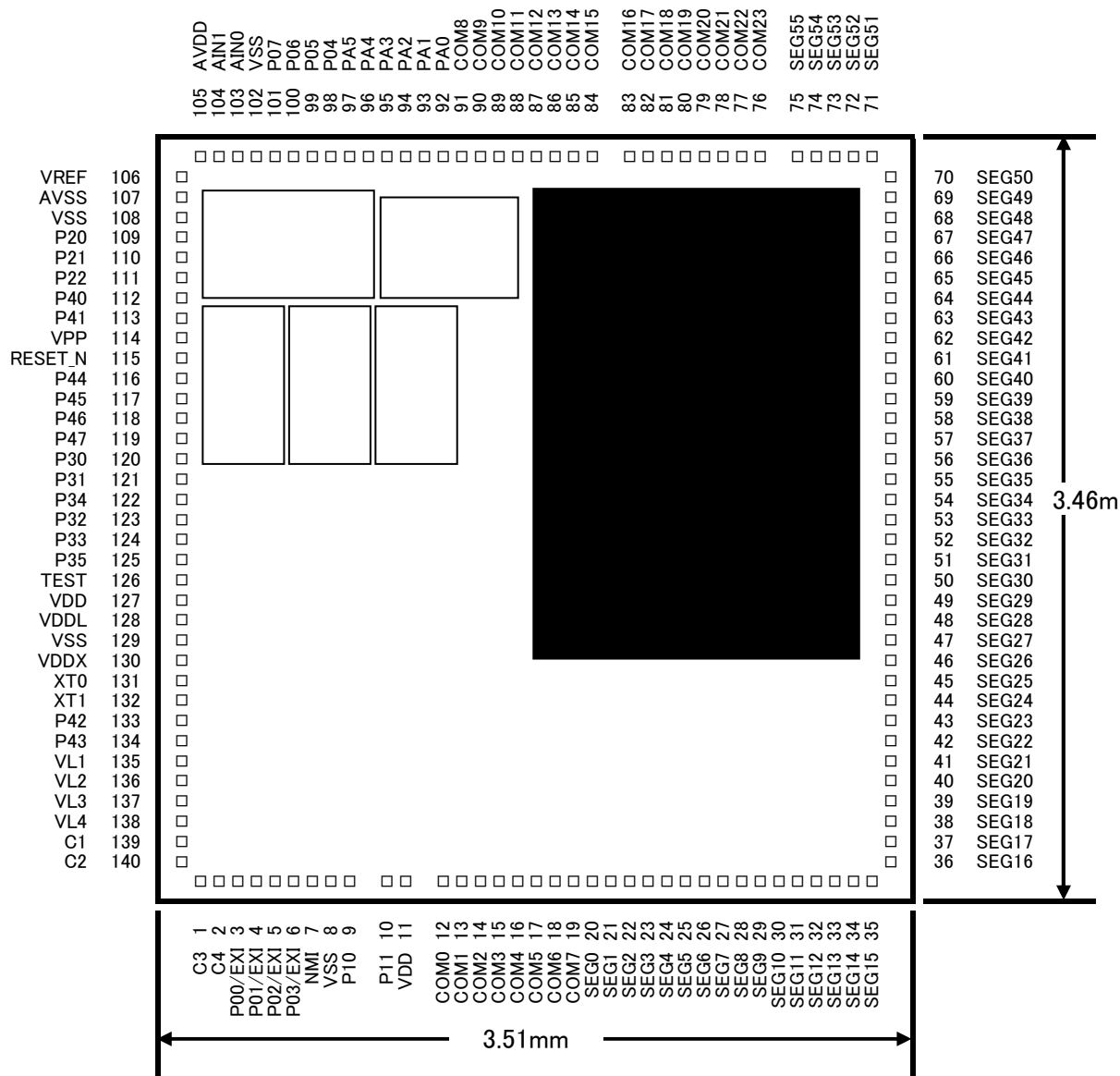
ML610Q439 LQFP144 Pin Layout



(NC): No Connection

Figure 4 ML610Q439 LQFP144 Pin Configuration

ML610Q438 Chip Pin Layout & Dimension



Chip size: 3.51 mm × 3.46 mm
 PAD count: 140 pins
 Minimum PAD pitch: 80 μm
 PAD aperture: 80 μm × 80 μm
 Chip thickness: 350 μm
 Voltage of the rear side of chip: V_{SS} level

Figure 5 ML610Q438 Chip Layout & Dimension

ML610Q438 Pad Coordinates

Table 1 ML610Q438 Pad Coordinates

Chip Center: X=0,Y=0

PAD No.	Pad Name	X (μm)	Y (μm)	PAD No.	Pad Name	X (μm)	Y (μm)	PAD No.	Pad Name	X (μm)	Y (μm)
1	C3	-1485	-1624	48	SEG28	1649	-400	95	PA3	-525	1624
2	C4	-1405	-1624	49	SEG29	1649	-320	96	PA4	-605	1624
3	P00/EXI0	-1315	-1624	50	SEG30	1649	-240	97	PA5	-685	1624
4	P01/EXI1	-1235	-1624	51	SEG31	1649	-160	98	P04	-765	1624
5	P02/EXI2 /RXD0/P2 CK	-1155	-1624	52	SEG32	1649	-80	99	P05	-845	1624
6	P03/EXI3	-1075	-1624	53	SEG33	1649	0	100	P06	-925	1624
7	NMI	-995	-1624	54	SEG34	1649	80	101	P07	-1005	1624
8	VSS	-865	-1624	55	SEG35	1649	160	102	VSS	-1106	1624
9	P10	-785	-1624	56	SEG36	1649	240	103	AIN0	-1186	1624
10	P11	-625	-1624	57	SEG37	1649	320	104	AIN1	-1366	1624
11	VDD	-545	-1624	58	SEG38	1649	400	105	AVDD	-1446	1624
12	COM0	-445	-1624	59	SEG39	1649	480	106	VREF	-1649	1430
13	COM1	-365	-1624	60	SEG40	1649	560	107	AVSS	-1649	1270
14	COM2	-285	-1624	61	SEG41	1649	640	108	VSS	-1649	1190
15	COM3	-205	-1624	62	SEG42	1649	720	109	P20	-1649	1095
16	COM4	-125	-1624	63	SEG43	1649	800	110	P21	-1649	1015
17	COM5	-45	-1624	64	SEG44	1649	880	111	P22	-1649	935
18	COM6	35	-1624	65	SEG45	1649	960	112	P40	-1649	855
19	COM7	115	-1624	66	SEG46	1649	1040	113	P41	-1649	775
20	SEG0	235	-1624	67	SEG47	1649	1120	114	VPP	-1649	695
21	SEG1	315	-1624	68	SEG48	1649	1200	115	RESET_N	-1649	615
22	SEG2	395	-1624	69	SEG49	1649	1280	116	P44	-1649	535
23	SEG3	475	-1624	70	SEG50	1649	1360	117	P45	-1649	455
24	SEG4	555	-1624	71	SEG51	1515	1624	118	P46	-1649	375
25	SEG5	635	-1624	72	SEG52	1435	1624	119	P47	-1649	295
26	SEG6	715	-1624	73	SEG53	1355	1624	120	P30	-1649	215
27	SEG7	795	-1624	74	SEG54	1275	1624	121	P31	-1649	135
28	SEG8	875	-1624	75	SEG55	1195	1624	122	P34	-1649	55
29	SEG9	955	-1624	76	COM23	1095	1624	123	P32	-1649	-25
30	SEG10	1035	-1624	77	COM22	1015	1624	124	P33	-1649	-105
31	SEG11	1115	-1624	78	COM21	935	1624	125	P35	-1649	-185
32	SEG12	1195	-1624	79	COM20	855	1624	126	TEST	-1649	-265
33	SEG13	1275	-1624	80	COM19	775	1624	127	VDD	-1649	-345
34	SEG14	1355	-1624	81	COM18	695	1624	128	VDDL	-1649	-425
35	SEG15	1435	-1624	82	COM17	615	1624	129	VSS	-1649	-505
36	SEG16	1649	-1360	83	COM16	535	1624	130	VDDX	-1649	-585
37	SEG17	1649	-1280	84	COM15	375	1624	131	XT0	-1649	-665
38	SEG18	1649	-1200	85	COM14	295	1624	132	XT1	-1649	-825
39	SEG19	1649	-1120	86	COM13	215	1624	133	P42	-1649	-905
40	SEG20	1649	-1040	87	COM12	135	1624	134	P43	-1649	-985
41	SEG21	1649	-960	88	COM11	55	1624	135	VL1	-1649	-1080
42	SEG22	1649	-880	89	COM10	-25	1624	136	VL2	-1649	-1160
43	SEG23	1649	-800	90	COM9	-105	1624	137	VL3	-1649	-1240
44	SEG24	1649	-720	91	COM8	-185	1624	138	VL4	-1649	-1320
45	SEG25	1649	-640	92	PA0	-285	1624	139	C1	-1649	-1400
46	SEG26	1649	-560	93	PA1	-365	1624	140	C2	-1649	-1480
47	SEG27	1649	-480	94	PA2	-445	1624				

PIN LIST

PAD No.		Primary function			Secondary function			Tertiary function		
Q439	Q438	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
8,102, 108,129	8,102, 108,129	V _{SS}	—	Negative power supply pin	—	—	—	—	—	—
11,127	11,127	V _{DD}	—	Positive power supply pin	—	—	—	—	—	—
128	128	V _{DDL}	—	Power supply pin for internal logic (internally generated)	—	—	—	—	—	—
130	130	V _{DDX}	—	Power supply pin for low-speed oscillation (internally generated)	—	—	—	—	—	—
114	114	V _{PP}	—	Power supply pin for Flash ROM	—	—	—	—	—	—
107	107	AV _{SS}	—	Negative power supply pin for successive approximation type ADC	—	—	—	—	—	—
105	105	AV _{DD}	—	Positive power supply pin for successive approximation type ADC	—	—	—	—	—	—
135	135	V _{L1}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
136	136	V _{L2}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
137	137	V _{L3}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
138	138	V _{L4}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
139	139	C1	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
140	140	C2	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
1	1	C3	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
2	2	C4	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
126	126	TEST	I/O	Input/output pin for testing	—	—	—	—	—	—
115	115	RESET _N	I	Reset input pin	—	—	—	—	—	—
131	131	XT0	I	Low-speed clock oscillation pin	—	—	—	—	—	—
132	132	XT1	O	Low-speed clock oscillation pin	—	—	—	—	—	—
106	106	V _{REF}	—	Reference power supply pin for successive approximation type ADC	—	—	—	—	—	—
103	103	AIN0	I	Successive approximation type ADC input	—	—	—	—	—	—

PAD No.		Primary function			Secondary function			Tertiary function		
Q439	Q438	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
104	104	AIN1	I	Successive approximation type ADC input	—	—	—	—	—	—
7	7	NMI	I	Non-maskable interrupt pin	—	—	—	—	—	—
3	3	P00/EXI0/CAP0	I	Input port, External interrupt 0 input, Capture 0 input	—	—	—	—	—	—
4	4	P01/EXI1/CAP1	I	Input port, External interrupt 1 input, Capture 1 input	—	—	—	—	—	—
5	5	P02/EXI2/RXD0/P2CK	I	Input port, External interrupt 2, UART0 receive, PWM2 external clock input	—	—	—	—	—	—
6	6	P03/EXI3	I	Input port, External interrupt 3	—	—	—	—	—	—
98	98	P04/EXI4	I/O	Input port, External interrupt 4	—	—	—	—	—	—
99	99	P05/EXI5	I/O	Input port, External interrupt 5	—	—	—	—	—	—
100	100	P06/EXI6	I/O	Input port, External interrupt 6	—	—	—	—	—	—
101	101	P07/EXI7	I/O	Input port, External interrupt 7	—	—	—	—	—	—
9	9	P10	I	Input port	OSC0	I	High-speed oscillation	—	—	—
10	10	P11	I	Input port	OSC1	O	High-speed oscillation	—	—	—
109	109	P20/LED0	O	Output port	LSCLK	O	Low-speed clock output	PWM2	O	PWM2 output
110	110	P21/LED1	O	Output port	OUTCLK	O	High-speed clock output	—	—	—
111	111	P22/LED2	O	Output port	MD0	O	Melody output	—	—	—
120	120	P30	I/O	Input/output port	IN0	I	RC type ADC0 oscillation input pin	PWM2	O	PWM2 output
121	121	P31	I/O	Input/output port	CS0	O	RC type ADC0 reference capacitor connection pin	—	—	—
123	123	P32	I/O	Input/output port	RS0	O	RC type ADC0 reference resistor connection pin	—	—	—
124	124	P33	I/O	Input/output port	RT0	O	RC type ADC0 resistor sensor connection pin	—	—	—
122	122	P34	I/O	Input/output port	RCT0	O	RC type ADC0 resistor/capacitor sensor connection pin	PWM0	O	PWM0 output
125	125	P35	I/O	Input/output port	RCM	O	RC type ADC oscillation monitor	PWM1	O	PWM1 output
112	112	P40	I/O	Input/output port	SDA	I/O	I2C data input/output	SIN0	I	SSIO data input
113	113	P41	I/O	Input/output port	SCL	I/O	I2C clock input/output	SCK0	I/O	SSIO synchronous clock
133	133	P42	I/O	Input/output port	RXD0	I	UART data input	SOUT0	O	SSIO data output
134	134	P43	I/O	Input/output port	TXD0	O	UART data output	PWM0	O	PWM0 output
116	116	P44/T02P0CK	I/O	Input/output port, Timer 0/Timer 2/PWM0 external clock input	IN1	I	RC type ADC1 oscillation input pin	SIN0	I	SSIO0 data input
117	117	P45/T13P1CK	I/O	Input/output port, Timer 1/Timer 3/PWM1 external clock input	CS1	O	RC type ADC1 reference capacitor connection pin	SCK0	I/O	SSIO0 synchronous clock
118	118	P46/T46P2CK	I/O	Input/output port, PWM2 external clock input	RS1	O	RC type ADC1 reference resistor connection pin	SOUT0	O	SSIO0 data output

PAD No.		Primary function			Secondary function			Tertiary function		
Q439	Q438	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
37	37	SEG17	O	LCD segment pin	—	—	—	—	—	—
38	38	SEG18	O	LCD segment pin	—	—	—	—	—	—
39	39	SEG19	O	LCD segment pin	—	—	—	—	—	—
40	40	SEG20	O	LCD segment pin	—	—	—	—	—	—
41	41	SEG21	O	LCD segment pin	—	—	—	—	—	—
42	42	SEG22	O	LCD segment pin	—	—	—	—	—	—
43	43	SEG23	O	LCD segment pin	—	—	—	—	—	—
44	44	SEG24	O	LCD segment pin	—	—	—	—	—	—
45	45	SEG25	O	LCD segment pin	—	—	—	—	—	—
46	46	SEG26	O	LCD segment pin	—	—	—	—	—	—
47	47	SEG27	O	LCD segment pin	—	—	—	—	—	—
48	48	SEG28	O	LCD segment pin	—	—	—	—	—	—
49	49	SEG29	O	LCD segment pin	—	—	—	—	—	—
50	50	SEG30	O	LCD segment pin	—	—	—	—	—	—
51	51	SEG31	O	LCD segment pin	—	—	—	—	—	—
52	52	SEG32	O	LCD segment pin	—	—	—	—	—	—
53	53	SEG33	O	LCD segment pin	—	—	—	—	—	—
54	54	SEG34	O	LCD segment pin	—	—	—	—	—	—
55	55	SEG35	O	LCD segment pin	—	—	—	—	—	—
56	56	SEG36	O	LCD segment pin	—	—	—	—	—	—
57	57	SEG37	O	LCD segment pin	—	—	—	—	—	—
58	58	SEG38	O	LCD segment pin	—	—	—	—	—	—
59	59	SEG39	O	LCD segment pin	—	—	—	—	—	—
60	60	SEG40	O	LCD segment pin	—	—	—	—	—	—
61	61	SEG41	O	LCD segment pin	—	—	—	—	—	—
62	62	SEG42	O	LCD segment pin	—	—	—	—	—	—
63	63	SEG43	O	LCD segment pin	—	—	—	—	—	—
64	64	SEG44	O	LCD segment pin	—	—	—	—	—	—
65	65	SEG45	O	LCD segment pin	—	—	—	—	—	—
66	66	SEG46	O	LCD segment pin	—	—	—	—	—	—
67	67	SEG47	O	LCD segment pin	—	—	—	—	—	—
68	68	SEG48	O	LCD segment pin	—	—	—	—	—	—
69	69	SEG49	O	LCD segment pin	—	—	—	—	—	—
70	70	SEG50	O	LCD segment pin	—	—	—	—	—	—
71	71	SEG51	O	LCD segment pin	—	—	—	—	—	—
72	72	SEG52	O	LCD segment pin	—	—	—	—	—	—
73	73	SEG53	O	LCD segment pin	—	—	—	—	—	—
74	74	SEG54	O	LCD segment pin	—	—	—	—	—	—
75	75	SEG55	O	LCD segment pin	—	—	—	—	—	—
76	—	SEG56	O	LCD segment pin	—	—	—	—	—	—
77	—	SEG57	O	LCD segment pin	—	—	—	—	—	—
78	—	SEG58	O	LCD segment pin	—	—	—	—	—	—
79	—	SEG59	O	LCD segment pin	—	—	—	—	—	—
80	—	SEG60	O	LCD segment pin	—	—	—	—	—	—
81	—	SEG61	O	LCD segment pin	—	—	—	—	—	—
82	—	SEG62	O	LCD segment pin	—	—	—	—	—	—
83	—	SEG63	O	LCD segment pin	—	—	—	—	—	—

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a “L” level, system reset mode is set and the internal section is initialized. When this pin is set to a “H” level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
XT0	I	Crystal connection pin for low-speed clock.	—	—
XT1	O	A 32.768 kHz crystal oscillator (see measuring circuit 1) is connected to this pin. Capacitors CDL and CGL are connected across this pin and V _{SS} as required.	—	—
OSC0	I	Crystal/ceramic connection pin for high-speed clock.	Secondary	—
OSC1	O	A crystal or ceramic is connected to this pin (4.1 MHz max.). Capacitors CDH and CGH (see measuring circuit 1) are connected across this pin and V _{SS} . This pin is used as the secondary function of the P10 pin(OSC0) and P11 pin(OSC1).	Secondary	—
LSCLK	O	Low-speed clock output pin. This pin is used as the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the secondary function of the P21 pin.	Secondary	—
General-purpose input port				
P00-P07	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P10-P11	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose output port				
P20-P22	O	General-purpose output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose input/output port				
P30-P35	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P40-P47	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
PA0-PA5	I/O	General-purpose input/output port.	Primary	Positive
UART				
TXD0	O	UART data output pin. This pin is used as the secondary function of the P43 pin.	Secondary	Positive
RXD0	I	UART data input pin. This pin is used as the secondary function of the P42 or the primary function of the P02 pin.	Primary/Secondary	Positive

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
I²C bus interface				
SDA	I/O	I ² C data input/output pin. This pin is used as the secondary function of the P40 pin. This pin has an NMOS open drain output. When using this pin as a function of the I ² C, externally connect a pull-up resistor.	Secondary	Positive
SCL	O	I ² C clock output pin. This pin is used as the secondary function of the P41 pin. This pin has an NMOS open drain output. When using this pin as a function of the I ² C, externally connect a pull-up resistor.	Secondary	Positive
Synchronous serial (SSIO)				
SCK0	I/O	Synchronous serial clock input/output pin. This pin is used as the tertiary function of the P41 or P45 pin.	Tertiary	—
SIN0	I	Synchronous serial data input pin. This pin is used as the tertiary function of the P40 or P44 pin.	Tertiary	Positive
SOUT0	O	Synchronous serial data output pin. This pin is used as the tertiary function of the P42 or P46 pin.	Tertiary	Positive
PWM				
PWM0	O	PWM0 output pin. This pin is used as the tertiary function of the P43 or P34 pin.	Tertiary	Positive
TOP0CK	I	PWM0 external clock input pin. This pin is used as the primary function of the P44 pin.	Primary	—
PWM1	O	PWM1 output pin. This pin is used as the tertiary function of the P47 or P35 pin.	Tertiary	Positive
T1P1CK	I	PWM1 external clock input pin. This pin is used as the primary function of the P45 pin.	Primary	—
PWM2	O	PWM2 output pin. This pin is used as the tertiary function of the P20 or P30 pin.	Tertiary	Positive
P2CK	I	PWM2 external clock input pin. This pin is used as the primary function of the P02 pin.	Primary	—
External interrupt				
NMI	I	External non-maskable interrupt input pin. An interrupt is generated on both edges.	Primary	Positive/negative
EXIO-7	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P00-P07 pins.	Primary	Positive/negative
Capture				
CAP0	I	Capture trigger input pins. The value of the time base counter is captured in the register synchronously with the interrupt edge selected by software.	Primary	Positive/negative
CAP1	I	These pins are used as the primary functions of the P00 pin(CAP0) and P01 pin(CAP1).	Primary	Positive/negative
Timer				
TOP0CK	I	External clock input pin used for Timer 0. This pin is used as the primary function of the P44 pin.	Primary	—
T1P1CK	I	External clock input pin used for Timer 1. This pin is used as the primary function of the P45 pin.	Primary	—
Melody				
MD0	O	Melody/buzzer signal output pin. This pin is used as the secondary function of the P22 pin.	Secondary	Positive/negative
LED drive				
LED0-2	O	Nch open drain output pins to drive LED.	Primary	Positive/negative

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V _{DD}	Ta = 25°C	−0.3 to +4.6	V
Power supply voltage 2	AV _{DD}	Ta = 25°C	−0.3 to +4.6	V
Power supply voltage 3	V _{PP}	Ta = 25°C	−0.3 to +9.5	V
Power supply voltage 4	V _{DDL}	Ta = 25°C	−0.3 to +3.6	V
Power supply voltage 5	V _{DDX}	Ta = 25°C	−0.3 to +3.6	V
Power supply voltage 6	V _{L1}	Ta = 25°C	−0.3 to +1.75	V
Power supply voltage 7	V _{L2}	Ta = 25°C	−0.3 to +3.5	V
Power supply voltage 8	V _{L3}	Ta = 25°C	−0.3 to +5.25	V
Power supply voltage 9	V _{L4}	Ta = 25°C	−0.3 to +7.0	V
Input voltage	V _{IN}	Ta = 25°C	−0.3 to V _{DD} +0.3	V
Output voltage	V _{OUT}	Ta = 25°C	−0.3 to V _{DD} +0.3	V
Output current 1	I _{OUT1}	Port3−A, Ta = 25°C	−12 to +11	mA
Output current 2	I _{OUT2}	Port2, Ta = 25°C	−12 to +20	mA
Power dissipation	PD	Ta = 25°C	122	mW
Storage temperature	T _{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T _{OP}	ML610Q438/Q439	−20 to +70	°C
		ML610Q438P/Q439P		
Operating voltage	V _{DD}	—	1.1 to 3.6	V
	AV _{DD}	—	2.2 to 3.6	AV _{DD}
Operating frequency (CPU)	f _{OP}	V _{DD} = 1.1 to 3.6V	30k to 36k	Hz
		V _{DD} = 1.3 to 3.6V	30k to 650k	
		V _{DD} = 1.8 to 3.6V	30k to 4.2M	
Low-speed crystal oscillation frequency	f _{XTL}	—	32.768k	Hz
Low-speed crystal oscillation external capacitor	C _{DL}	—	0 to 12	pF
	C _{GL}	—	0 to 12	
High-speed crystal/ceramic oscillation frequency	f _{XTH}	—	4.0M / 4.096M	Hz
High-speed crystal oscillation external capacitor	C _{DH}	—	24	pF
	C _{GH}	—	24	
Capacitor externally connected to V _{DDL} pin	C _{L0}	—	1.0±30%	μF
	C _{L1}	—	0.1±30%	
Capacitor externally connected to V _{DDX} pin	C _X	—	0.1±30%	μF
Capacitors externally connected to V _{L1} , 2, 3, 4 pins	C _{a, b, c, d}	—	1.0±30%	μF
Capacitors externally connected across C1 and C2 pins and across C3 and C4 pins	C ₁₂ , C ₃₄	—	1.0±30%	μF

DC CHARACTERISTICS (3/5)

($V_{DD} = 1.1$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^{\circ}C$, $T_a = -40$ to $+85^{\circ}C$ for P version, unless otherwise specified) (3/5)

Parameter	Symbol	Condition		Rating			Unit	Measuring circuit
				Min.	Typ.	Max.		
BLD threshold voltage	V_{BLD}	$V_{DD} = 1.35$ to $3.6V$	LD2-0 = 0H	Typ. -2%	1.35	Typ. +2%	V	1
			LD2-0 = 1H		1.4			
			LD2-0 = 2H		1.45			
			LD2-0 = 3H		1.5			
			LD2-0 = 4H		1.6			
			LD2-0 = 5H		1.7			
			LD2-0 = 6H		1.8			
			LD2-0 = 7H		1.9			
			LD2-0 = 8H		2.0			
			LD2-0 = 9H		2.1			
			LD2-0 = 0AH		2.2			
			LD2-0 = 0BH		2.3			
			LD2-0 = 0CH		2.4			
			LD2-0 = 0DH		2.5			
			LD2-0 = 0EH		2.7			
			LD2-0 = 0FH		2.9			
BLD threshold voltage temperature deviation	ΔV_{BLD}	$V_{DD} = 1.35$ to $3.6V$		—	~0	—	%/ $^{\circ}C$	1
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed oscillation: stopped.	$T_a = 25^{\circ}C$	—	0.15	0.50	μA	1
			$T_a = -20$ to $+70^{\circ}C$	—	—	2.50		
Supply current 2	IDD2	CPU: In HALT state (LTBC, RTC: Operating ^{*3*5}). High-speed oscillation: Stopped. LCD/BIAS circuits: Stopped.	$T_a = 25^{\circ}C$	—	0.5	1.3	μA	1
			$T_a = -20$ to $+70^{\circ}C$	—	—	3.5		
Supply current 3	IDD3	CPU: In 32.768kHz operating state. ^{*1*3} High-speed oscillation: Stopped. LCD/BIAS circuits: Operating. ^{*2}	$T_a = 25^{\circ}C$	—	5	7	μA	1
			$T_a = -20$ to $+70^{\circ}C$	—	—	12		
Supply current 4	IDD4	CPU: In 500kHz CR operating state. LCD/BIAS circuits: Operating. ^{*2*3}	$T_a = 25^{\circ}C$	—	70	85	μA	1
			$T_a = -20$ to $+70^{\circ}C$	—	—	100		
Supply current 5	IDD5	CPU: In 4.096MHz operating state. PLL: In oscillating state. LCD/BIAS circuits: Operating. ^{*2*3} $V_{DD} = 1.8$ to $3.6V$	$T_a = 25^{\circ}C$	—	0.8	1.0	mA	1
			$T_a = -20$ to $+70^{\circ}C$	—	—	1.2		

^{*1}: CPU operating rate is 100% (No HALT state).

^{*2}: All SEGs: off waveform, No LCD panel load, 1/3 bias, 1/3 duty, Frame frequency: Approx. 64 Hz, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)

^{*3}: Use 32.768KHz Crystal Resonator DT-26 (Load capacitance 6pF) (KDS: DAISHINKU CORP.)

^{*4}: Use 4.096MHz Crystal Oscillator CHC49SFWB (Kyocera).

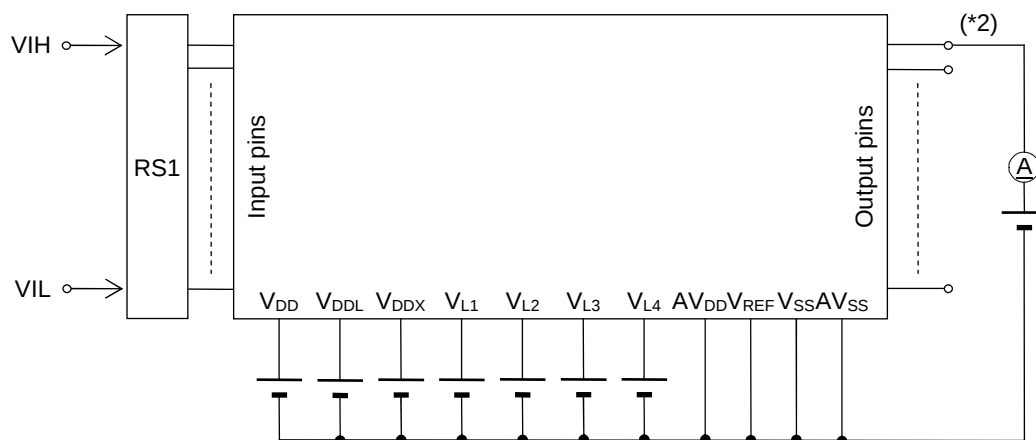
^{*5}: Significant bits of BLKCON0~BLKCON4 registers are all "1".

DC CHARACTERISTICS (4/5)

($V_{DD} = 1.1$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^\circ C$, $T_a = -40$ to $+85^\circ C$ for P version, unless otherwise specified) (4/5)

Parameter	Symbol	Condition		Rating			Unit	Measuring circuit
				Min.	Typ.	Max.		
Output voltage 1 (P20–P22/2 nd function is selected) (P30–P36) (P40–P47) (PA0–PA5)	VOH1	IOH1 = $-0.5mA$, $V_{DD} = 1.8$ to $3.6V$		$V_{DD} - 0.5$	—	—	V	2
		IOH1 = $-0.1mA$, $V_{DD} = 1.3$ to $3.6V$		$V_{DD} - 0.3$	—	—		
		IOH1 = $-0.03mA$, $V_{DD} = 1.1$ to $3.6V$		$V_{DD} - 0.3$	—	—		
	VOL1	IOL1 = $+0.5mA$, $V_{DD} = 1.8$ to $3.6V$		—	—	0.5		
		IOL1 = $+0.1mA$, $V_{DD} = 1.3$ to $3.6V$		—	—	0.5		
		IOL1 = $+0.03mA$, $V_{DD} = 1.1$ to $3.6V$		—	—	0.3		
Output voltage 2 (P20–P22/2 nd function is Not selected)	VOH2	IOH1 = $-0.5mA$, $V_{DD} = 1.8$ to $3.6V$		$V_{DD} - 0.5$	—	—		
		IOH1 = $-0.1mA$, $V_{DD} = 1.3$ to $3.6V$		$V_{DD} - 0.3$	—	—		
		IOH1 = $-0.03mA$, $V_{DD} = 1.1$ to $3.6V$		$V_{DD} - 0.3$	—	—		
	VOL2	IOL2 = $+5mA$, $V_{DD} = 1.8$ to $3.6V$		—	—	0.5		
Output voltage 3 (P40–P41)	VOL3	IOL3 = $+3mA$, $V_{DD} = 2.0$ to $3.6V$ (when I ² C mode is selected)		—	—	0.4		
Output voltage 4 (COM0–23) (SEG0–63)	VOH4	IOH4 = $-0.2mA$, $V_{L1} = 1.2V$		$V_{L4} - 0.2$	—	—		
	VOMH4	IOMH4 = $+0.2mA$, $V_{L1} = 1.2V$		—	—	$V_{L3} + 0.2$		
	VOMH4S	IOMH4S = $-0.2mA$, $V_{L1} = 1.2V$		$V_{L3} - 0.2$	—	—		
	VOM4	IOM4 = $+0.2mA$, $V_{L1} = 1.2V$		—	—	$V_{L2} + 0.2$		
	VOM4S	IOM4S = $-0.2mA$, $V_{L1} = 1.2V$		$V_{L2} - 0.2$	—	—		
	VOML4	IOML4 = $+0.2mA$, $V_{L1} = 1.2V$		—	—	$V_{L1} + 0.2$		
	VOML4S	IOML4S = $-0.2mA$, $V_{L1} = 1.2V$		$V_{L1} - 0.2$	—	—		
	VOL4	IOL4 = $+0.2mA$, $V_{L1} = 1.2V$		—	—	0.2		
Output leakage (P20–P22) (P30–P35) (P40–P47) (PA0–PA5)	IOOH	VOH = V_{DD} (in high-impedance state)		—	—	1	μA	3
	IOOL	VOL = V_{SS} (in high-impedance state)		-1	—	—		
Input current 1 (RESET_N)	IIH1	$V_{IH1} = V_{DD}$		0	—	1	μA	4
	IIL1	$V_{IL1} = V_{SS}$	$V_{DD} = 1.8$ to $3.6V$	-600	-300	-20		
			$V_{DD} = 1.3$ to $3.6V$	-600	-300	-10		
			$V_{DD} = 1.1$ to $3.6V$	-600	-300	-2		
Input current 1 (TEST)	IIH1	$V_{IH1} = V_{DD}$	$V_{DD} = 1.8$ to $3.6V$	20	300	600		
			$V_{DD} = 1.3$ to $3.6V$	10	300	600		
			$V_{DD} = 1.1$ to $3.6V$	2	300	600		
	IIL1	$V_{IL1} = V_{SS}$		-1	—	—		
Input current 2 (NMI) (P00–P03) (P04–P07)	IIH2	$V_{IH2} = V_{DD}$ (when pulled-down)	$V_{DD} = 1.8$ to $3.6V$	2	30	200		
			$V_{DD} = 1.3$ to $3.6V$	0.2	30	200		
			$V_{DD} = 1.1$ to $3.6V$	0.01	30	200		
	IIL2	$V_{IL2} = V_{SS}$		-200	-30	-2		

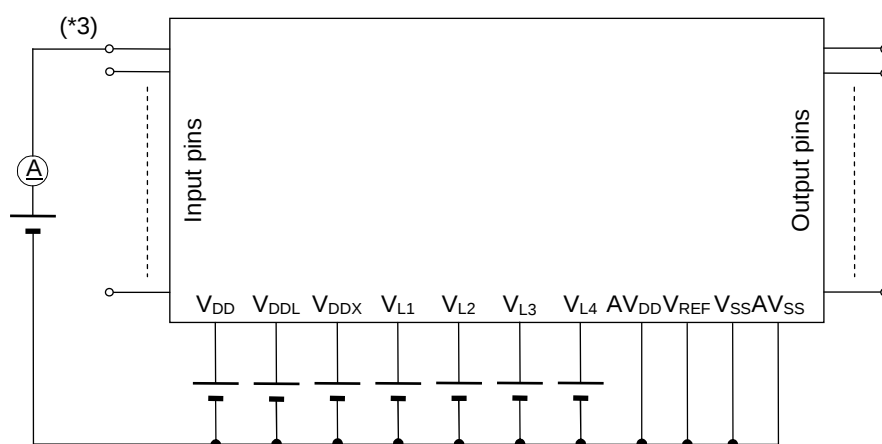
MEASURING CIRCUIT 3



*1: Input logic circuit to determine the specified measuring conditions.

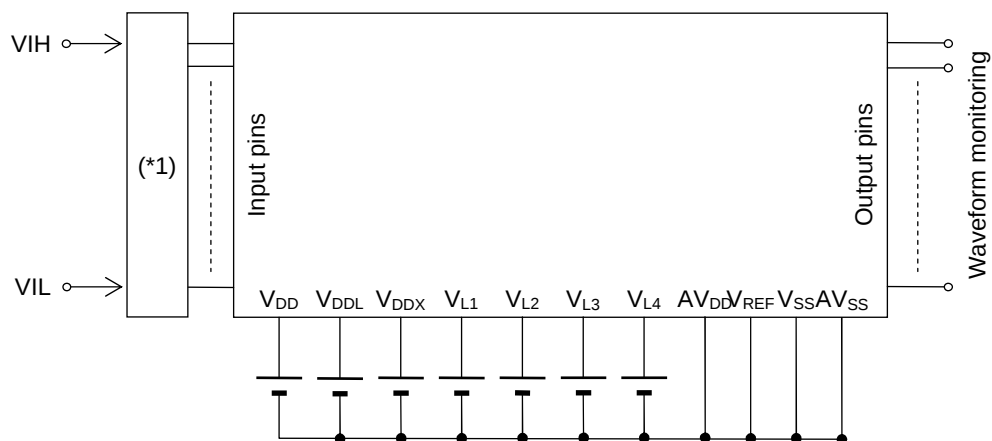
*2: Measured at the specified output pins.

MEASURING CIRCUIT 4



*3: Measured at the specified output pins.

MEASURING CIRCUIT 5

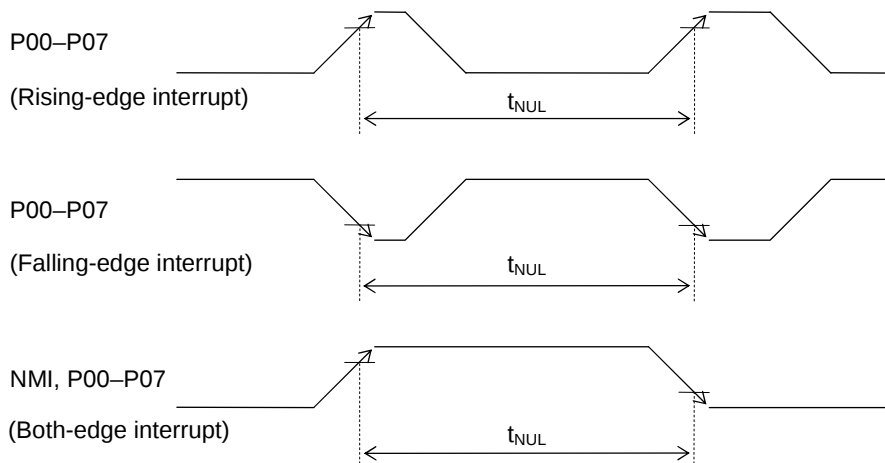


*1: Input logic circuit to determine the specified measuring conditions.

AC CHARACTERISTICS (External Interrupt)

($V_{DD} = 1.1$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^{\circ}C$, $T_a = -40$ to $+85^{\circ}C$ for P version, unless otherwise specified)

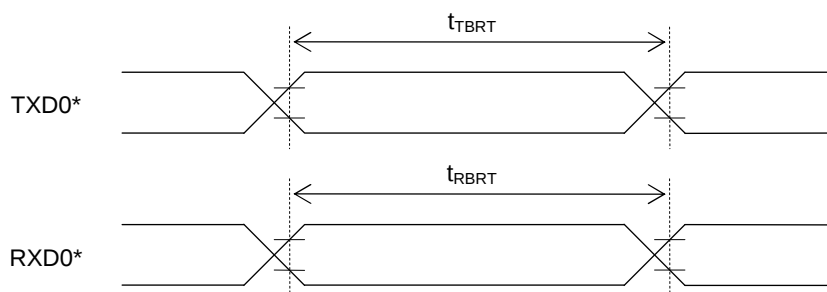
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation System clock: 32.768kHz	76.8	—	106.8	μs

**AC CHARACTERISTICS (UART)**

($V_{DD} = 1.1$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^{\circ}C$, $T_a = -40$ to $+85^{\circ}C$ for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Transmit baud rate	t_{TBRT}	—	—	BRT^{*1}	—	s
Receive baud rate	t_{RBRT}	—	BRT^{*1} –3%	BRT^{*1}	BRT^{*1} +3%	s

*1: Baud rate period (including the error of the clock frequency selected) set with the UART baud rate register (UA0BRTL,H) and the UART mode register 0 (UA0MOD0).



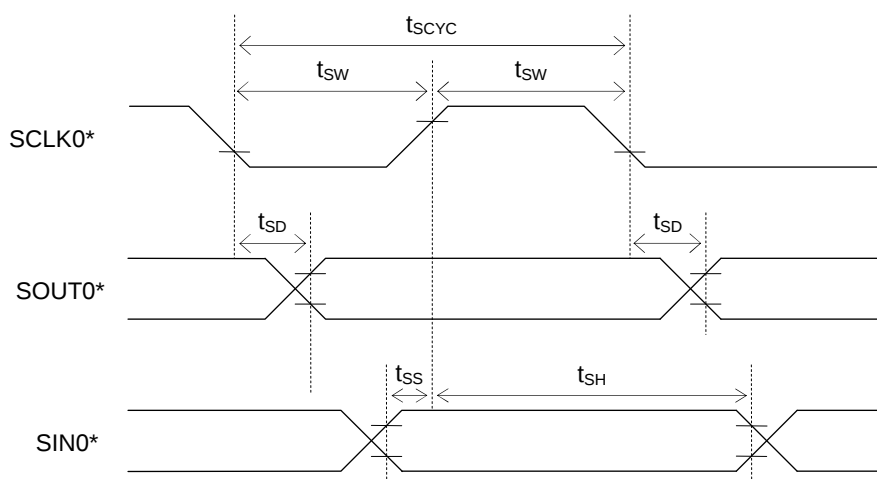
*: Indicates the secondary function of the port.

AC CHARACTERISTICS (Synchronous Serial Port)

($V_{DD} = 1.1$ to $3.6V$, $AV_{DD} = 2.2$ to $3.6V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $+70^{\circ}C$, $T_a = -40$ to $+85^{\circ}C$ for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCLK input cycle (slave mode)	t_{SCYC}	When high-speed oscillation is not active	10	—	—	μs
		When high-speed oscillation is active ($V_{DD} = 1.8$ to $3.6V$)	1	—	—	μs
SCLK output cycle (master mode)	t_{SCYC}	—	—	$SCLK^{*1}$	—	s
SCLK input pulse width (slave mode)	t_{SW}	When high-speed oscillation is not active	4	—	—	μs
		When high-speed oscillation is active ($V_{DD} = 1.8$ to $3.6V$)	0.4	—	—	μs
SCLK output pulse width (master mode)	t_{SW}	—	$SCLK^{*1} \times 0.4$	$SCLK^{*1} \times 0.5$	$SCLK^{*1} \times 0.6$	s
SOUT output delay time (slave mode)	t_{SD}	—	—	—	180	ns
SOUT output delay time (master mode)	t_{SD}	—	—	—	80	ns
SIN input setup time (slave mode)	t_{SS}	—	80	—	—	ns
SIN input setup time (master mode)	t_{SS}	—	180	—	—	ns
SIN input hold time	t_{SH}	—	80	—	—	ns

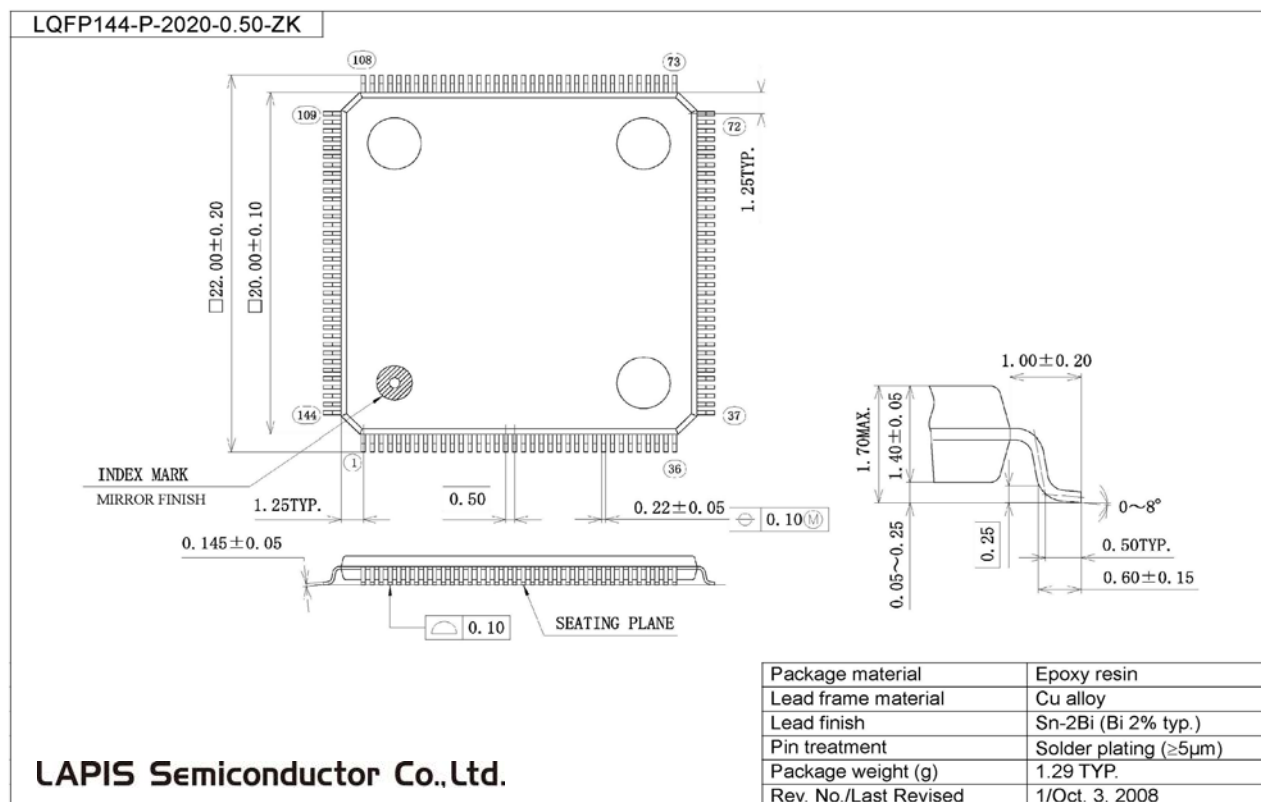
*1: Clock period selected with S0CK3–0 of the serial port 0 mode register (SIO0MOD1)



*: Indicates the secondary function of the port.

Package Dimensions

(Unit: mm)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact our responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Revision History

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610Q439-01	Aug. 24,2010	—	—	Formally edition 1.0
FEDL610Q439-02	Feb. 2,2011	34	34	Change of a Package Dimensions
FEDL610Q439-03	Jun. 7,2011	3	3	Add the P persion

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