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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	eZ80
Core Size	8-Bit
Speed	50MHz
Connectivity	Ethernet, I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	32
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/ez80f91aza50eg

List of Tables

Figure 2 shows the pin layout of the eZ80F91 device in the 144-pin LQFP package.

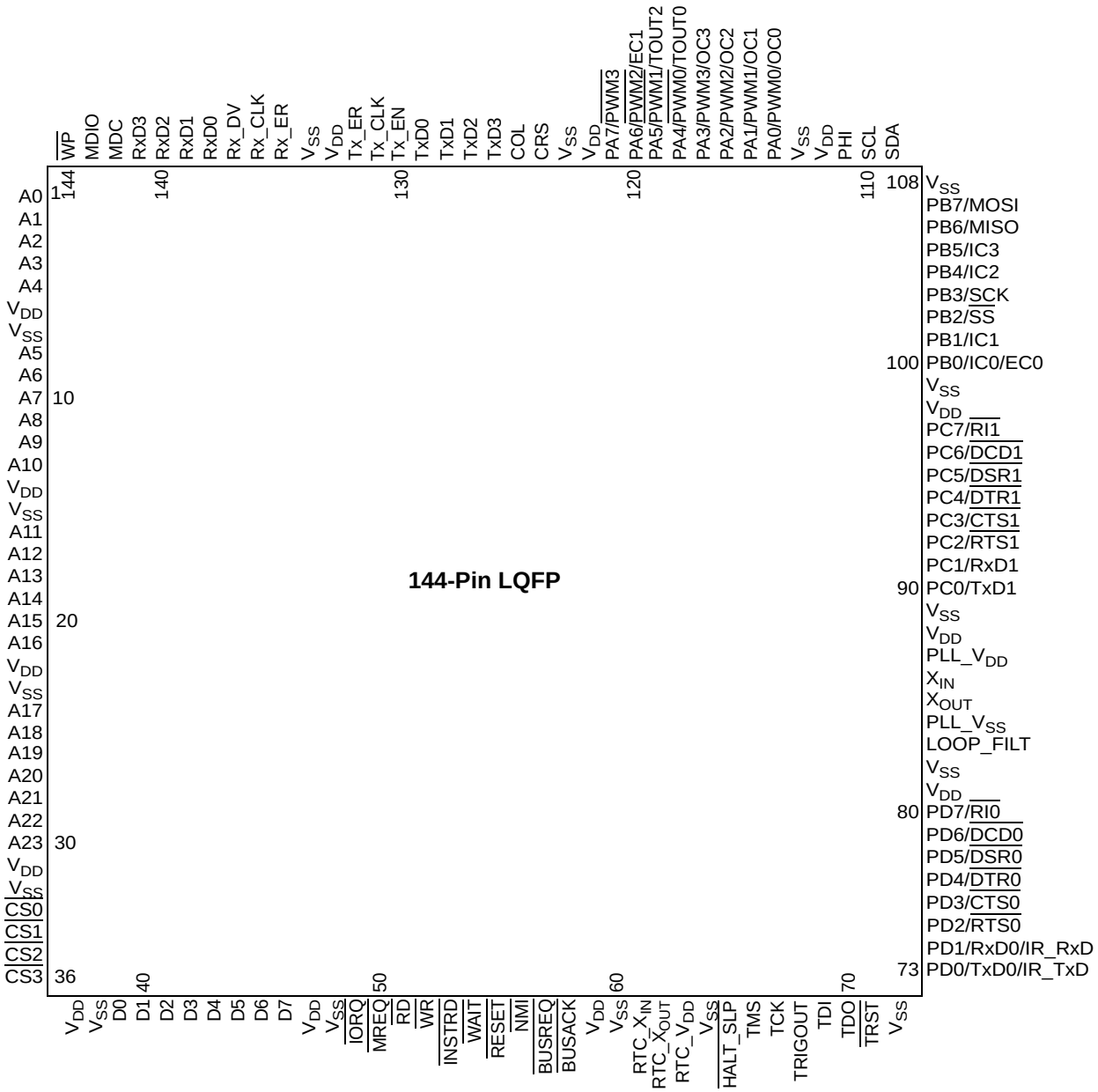


Figure 2. 144-Pin LQFP Configuration of the eZ80F91

Table 2. Pin Identification on the eZ80F91 ASSP Device (Continued)

LQFP Pin No	BGA Pin No	Symbol	Function	Signal Direction	Description
95	F10	PC5	GPIO Port C	Bidirectional with Schmitt Trigger input	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port C pin, when programmed as output is selected to be an open-drain or open-source output. Port C is multiplexed with one UART.
		DSR1	Data Set Ready	Schmitt Trigger input, Active Low	Modem status signal to the UART. This signal is multiplexed with PC5.
96	G8	PC6	GPIO Port C	Bidirectional with Schmitt Trigger input	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port C pin, when programmed as output is selected to be an open-drain or open-source output. Port C is multiplexed with one UART.
		DCD1	Data Carrier Detect	Schmitt Trigger input, Active Low	Modem status signal to the UART. This signal is multiplexed with PC6.
97	E12	PC7	GPIO Port C	Bidirectional with Schmitt Trigger input	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port C pin, when programmed as output is selected to be an open-drain or open-source output. Port C is multiplexed with one UART.
		RI1	Ring Indicator	Schmitt Trigger input, Active Low	Modem status signal to the UART. This signal is multiplexed with PC7.
98	E11	V_{DD}	Power Supply		Power Supply.
99	F9	V_{SS}	Ground		Ground.

Table 2. Pin Identification on the eZ80F91 ASSP Device (Continued)

LQFP Pin No	BGA Pin No	Symbol	Function	Signal Direction	Description
103	D11	PB3	GPIO Port B	Bidirectional with Schmitt Trigger input	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port B pin, when programmed as output is selected to be an open-drain or open-source output.
		SCK	SPI Serial Clock	Bidirectional with Schmitt Trigger input	SPI serial clock. This signal is multiplexed with PB3.
104	E9	PB4	GPIO Port B	Bidirectional with Schmitt Trigger input	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port B pin, when programmed as output is selected to be an open-drain or open-source output.
		IC2	Input Capture	Schmitt Trigger input	Input Capture A Signal to Timer 3. This signal is multiplexed with PB4.
105	D10	PB5	GPIO Port B	Bidirectional with Schmitt Trigger input	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port B pin, when programmed as output is selected to be an open-drain or open-source output.
		IC3	Input Capture	Schmitt Trigger input	Input Capture B Signal to Timer 3. This signal is multiplexed with PB5.

System Clock Source Options

The following section describes five system clock source options.

System Clock

The eZ80F91 ASSP device's internal clock, SCLK, is responsible for clocking all internal logic. The SCLK source can be an external crystal oscillator, an internal PLL, or an internal 32 kHz RTC oscillator. The SCLK source is selected by PLL Control Register 0. RESET default is provided by the external crystal oscillator. For more details about CLK_MUX values in the PLL Control Register 0, see Table 155 on page 270.

PHI

PHI is a device output driven by SCLK that is used for system synchronization to the eZ80F91 ASSP device. PHI is used as the reference clock for all AC characteristics; for details, see the AC Characteristics chapter on page 343.

External Crystal Oscillator

An externally-driven oscillator operates in two modes. In one mode, the X_{IN} pin is driven by a oscillator from DC up to 50 MHz when the X_{OUT} pin is not connected. In the other mode, the X_{IN} and X_{OUT} pins are driven by a crystal circuit.

Crystals recommended by Zilog are defined to be a 50 MHz–3 overtone circuit or 1–10 MHz range fundamental for PLL operation. For details, see the On-Chip Oscillators chapter on page 332.

Real Time Clock

An internal 32 kHz real-time clock crystal oscillator driven by either the on-chip 32768 Hz crystal oscillator or a 50/60 Hz power-line frequency input. While intended for time-keeping, the RTC 32 kHz oscillator is selected as an SCLK. RTC_V_{DD} and RTC_V_{SS} provides an isolated power supply to ensure RTC operation in the event of loss of line power when a battery is provided. For more details, see the Real-Time Clock chapter on page 155.

PLL Clock

The eZ80F91 MCU's internal PLL is driven by external crystals or external crystal oscillators in the range of 1 MHz to 10 MHz, and generates an SCLK up to 50 MHz. For more details, see the Phase-Locked Loop chapter on page 265.

SCLK Source Selection Example

For additional SCLK source selection examples, refer to the Crystal Oscillator/Resonator Guidelines for eZ80 and eZ80Acclaim! Devices Technical Note (TN0013), which is available free for download from the Zilog website.

Bit	Description (Continued)
[6] INT_PX	**Pin 6 Interrupt Priority** 1: Level One Interrupt Priority 0: Default Interrupt Priority
[5] INT_PX	**Pin 5 Interrupt Priority** 1: Level One Interrupt Priority 0: Default Interrupt Priority
[4] INT_PX	**Pin 4 Interrupt Priority** 1: Level One Interrupt Priority 0: Default Interrupt Priority
[3] INT_PX	**Pin 3 Interrupt Priority** 1: Level One Interrupt Priority 0: Default Interrupt Priority
[2] INT_PX	**Pin 2 Interrupt Priority** 1: Level One Interrupt Priority 0: Default Interrupt Priority
[1] INT_PX	**Pin 1 Interrupt Priority** 1: Level One Interrupt Priority 0: Default Interrupt Priority
[0] INT_PX	**Pin 0 Interrupt Priority** 1: Level One Interrupt Priority 0: Default Interrupt Priority

The Interrupt Vector Priority Control bits are listed in Table 15.

Table 15. Interrupt Vector Priority Control Bits

Priority Control Bit	Vector	Source	Priority Control Bit	Vector	Source
INT_P0[0]	040h	EMAC Rx	INT_P3[0]	0A0h	Port B 0
INT_P0[1]	044h	EMAC Tx	INT_P3[1]	0A4h	Port B 1
INT_P0[2]	048h	EMAC SYS	INT_P3[2]	0A8h	Port B 2
INT_P0[3]	04Ch	PLL	INT_P3[3]	0ACh	Port B 3
INT_P0[4]	050h	Flash	INT_P3[4]	0B0h	Port B 4
INT_P0[5]	054h	Timer 0	INT_P3[5]	0B4h	Port B 5
INT_P0[6]	058h	Timer 1	INT_P3[6]	0B8h	Port B 6
INT_P0[7]	05Ch	Timer 2	INT_P3[7]	0BCh	Port B 7
INT_P1[0]	060h	Timer 3	INT_P4[0]	0C0h	Port C 0
INT_P1[1]	064h	Unused*	INT_P4[1]	0C4h	Port C 1

Note: *The vector addresses 064h and 068h are left unused to avoid conflict with the NMI vector address 066h.

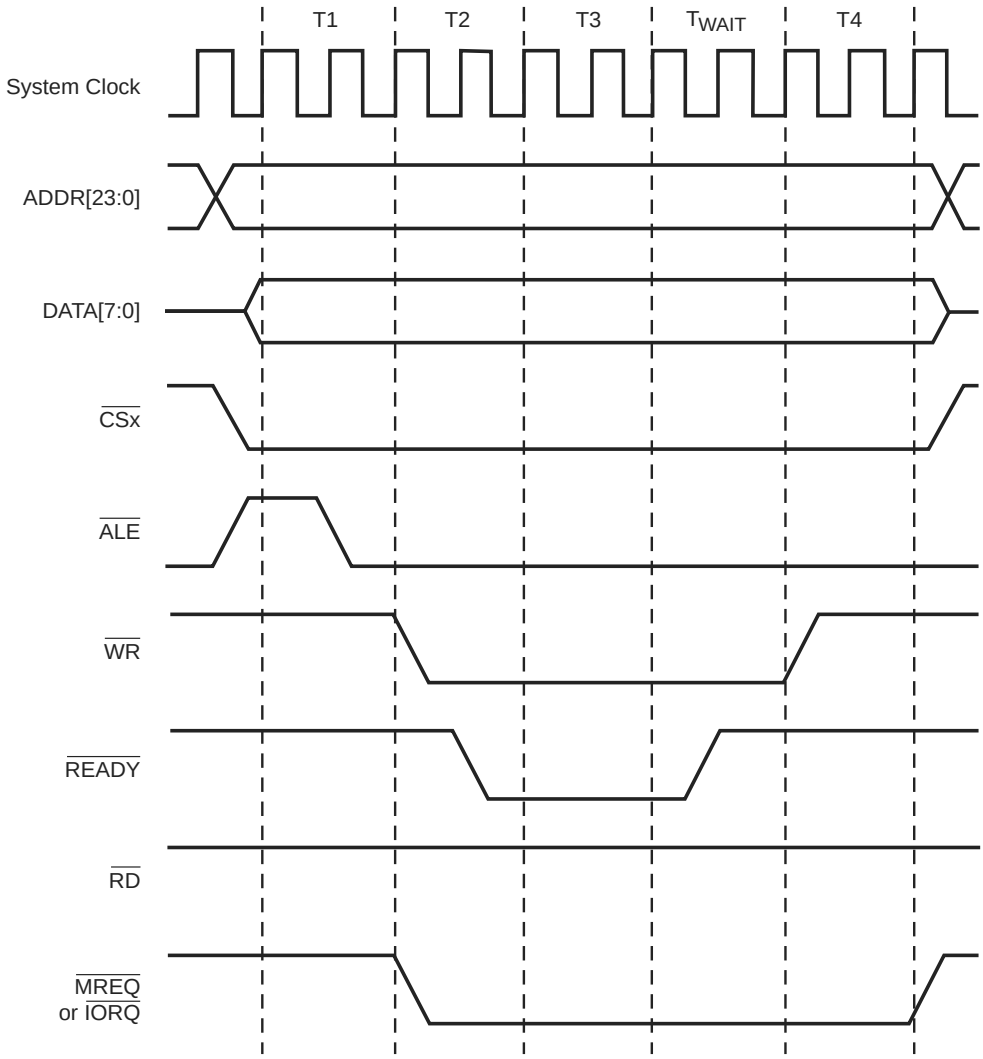


Figure 14. Example: Intel Bus Mode Write Timing: Separate Address and Data Buses

Basic Timer Operation

Basic timer operation is controlled by a timer control register and a programmable reload value. The CPU uses the control register to setup the prescaling, the input clock source, the end-of-count behavior, and to start the timer. The 16-bit reload value is used to determine the duration of the timer's count before either halting or reloading.

After choosing a timer period and writing the appropriate values to the reload registers, the CPU must set the timer enable bit (TMR*x*_CTL[TIM_EN]) by allowing the count to begin. The reload bit (TMR*x*_CTL[RLD]) must also be asserted so that the timer counts down from the reload value rather than from 0000h. On the system clock cycle, after the assertion of the reload bit, the timer loads with the 16-bit reload value and begins counting down. The reload bit is automatically cleared after the loading operation. The timer is enabled and reloaded on the same cycle; however, the timer does not require disabling to reload and reloading is performed at any time. It is also possible to halt the timer by deasserting the timer enable bit and resuming the count at a later time from the same point by reasserting the bit.

Reading the Current Count Value

The CPU reads the current count value when the timer is running. Because the count is a 16-bit value, the hardware latches the value of the upper byte into temporary storage when the lower byte is read. This value in temporary storage is the value returned when the upper byte is read. Therefore, the software must read the lower byte first. If it attempts to read the upper byte first, it does not obtain the current upper byte of the count. Instead, it obtains the last latched value. This read operation does not affect timer operation.

Setting Timer Duration

There are three factors to consider while determining Programmable Reload Timer duration: clock frequency, clock divider ratio, and initial count value. Minimum duration of the timer is achieved by loading 0001h. Maximum duration is achieved by loading 0000h, because the timer first rolls over to FFFFh and then continues counting down to 0000h before the end-of-count is signaled. Depending on the TMR*x*_CTL[CLK_SEL] bits of the control register, the clock is either the system clock, or an on-chip RC oscillator output or an input from a pin.

The time-out period of the timer is returned by the following equation:

$$\text{Time-Out Period} = \frac{\text{Clock Divider Ratio x Reload Value}}{\text{System Clock Frequency}}$$

To calculate the time-out period with the above equation while using an initial value of 0000h, enter a reload value of 65536 (FFFFh + 1).

Timer Interrupt Enable Register

The Timer *x* Interrupt Enable Register, shown in Table 55, is used to control timer interrupt operations. Only bits related to functions present in a given timer are active.

Table 55. Timer Interrupt Enable (TMR*x*_IER)

Bit	7	6	5	4	3	2	1	0
Field	Reserved	IRQ_OC*x*_EN				IRQ_ ICB_EN	IRQ_ ICA_EN	IRQ_ EOC_EN
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	TMR0_IER = 0061h, TMR1_IER = 0066h, TMR2_IER = 0070h, TMR3_IER = 0075h							

Note: R = read only; R/W = read/write.

Bit	Description
[7]	**Reserved** This bit is unused and must be programmed to 0.
[6] IRQ_OC3_EN	**Interrupt Request Output Compare 3 Enable** 0: Interrupt requests for OC3 are disabled (valid only in OUTPUT COMPARE Mode). OC operations occur in Timer 3. 1: Interrupt requests for OC3 are enabled (valid only in OUTPUT COMPARE Mode). OC operations occur in Timer 3.
[5] IRQ_OC2_EN	**Interrupt Request Output Compare 2 Enable** 0: Interrupt requests for OC2 are disabled (valid only in OUTPUT COMPARE Mode). OC operations occur in Timer 3. 1: Interrupt requests for OC2 are enabled (valid only in OUTPUT COMPARE Mode). OC operations occur in Timer 3.
[4] IRQ_OC1_EN	**Interrupt Request Output Compare 1 Enable** 0: Interrupt requests for OC1 are disabled (valid only in OUTPUT COMPARE Mode). OC operations occur in Timer 3. 1: Interrupt requests for OC1 are enabled (valid only in OUTPUT COMPARE Mode). OC operations occur in Timer 3.
[3] IRQ_OC0_EN	**Interrupt Request Output Compare 0 Enable** 0: Interrupt requests for OC0 are disabled (valid only in OUTPUT COMPARE Mode). OC operations occur in Timer 3. 1: Interrupt requests for OC0 are enabled (valid only in OUTPUT COMPARE Mode). OC operations occur in Timer 3.

Table 60. Timer Reload High Byte Register (TMR*x*_RR_H)

Bit	7	6	5	4	3	2	1	0
Field	TMR_RR_H							
Reset	0	0	0	0	0	0	0	0
R/W	W	W	W	W	W	W	W	W
Address	TMR0_RR_H = 0064h, TMR1_RR_H = 0069h, TMR2_RR_H = 0073h, TMR3_RR_H = 0078h							

Note: W = write only.

Bit	Description
[7:0] TMR_RR_H	**Timer Reload High Byte** 00h–FFh: These bits represent the high byte of the 2-byte timer reload value, {TMR*x*_RR_H[7:0], TMR*x*_RR_L[7:0]}. Bit 7 is bit 15 (msb) of the 16-bit timer reload value. Bit 0 is bit 8 of the 16-bit timer reload value.

Timer Input Capture Control Register

The Timer *x* Input Capture Control Register, shown in Table 61, is used to select the edge or edges to be captured. For Timer 1, CAP_EDGE_B is used for IC1 and CAP_EDGE_A is for IC0. For Timer 3, CAP_EDGE_B is for IC3, and CAP_EDGE_A is for IC2.

Table 61. Timer Input Capture Control Register (TMR1_CAP_CTL, TMR3_CAP_CTL)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				CAP_EDGE_B		CAP_EDGE_A	
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	TMR1_CAP_CTL = 006Ah, TMR3_CAP_CTL = 007Bh							

Note: R = read only; R/W = read/write.

Bit	Description
[7:4]	**Reserved** These bits are reserved and must be programmed to 0000.
[3:2] CAP_EDGE_B	**Capture Edge Enable B** 00: Disable capture on ICB. 01: Enable capture only on the falling edge of ICB. 10: Enable capture only on the rising edge of ICB. 11: Enable capture on both edges of ICB.

Bit	Description (Continued)
[4] TCIE	**Transmission Complete Interrupt** 0: Transmission complete interrupt is disabled 1: Transmission complete interrupt is generated when both the transmit hold register and the transmit shift register are empty
[3] MIIE	**Modem Interrupt Input Enable** 0: Modem interrupt on edge detect of status inputs is disabled. 1: Modem interrupt on edge detect of status inputs is enabled.
[2] LSIE	**Line Status Interrupt Input Enable** 0: Line status interrupt is disabled. 1: Line status interrupt is enabled for receive data errors: incorrect parity bit received, framing error, overrun error, or break detection.
[1] TIE	**Transmit Interrupt Input Enable** 0: Transmit interrupt is disabled. 1: Transmit interrupt is enabled. Interrupt is generated when the transmit FIFO/buffer is empty indicating no more bytes available for transmission.
[0] RIE	**Receive Interrupt Input Enable** 0: Receive interrupt is disabled. 1: Receive interrupt and receiver time-out interrupt are enabled. Interrupt is generated if the FIFO/buffer contains data ready to be read or if the receiver times out.

UART Interrupt Identification Register

The read-only UARTx_IIR Register allows you to check whether the FIFO is enabled and the status of interrupts. These registers share the same I/O addresses as the UARTx_FCTL registers. See Tables 99 and 100.

Table 99. UART Interrupt Identification Registers (UART*x*_IIR)

Bit	7	6	5	4	3	2	1	0
Field	FSTS	Reserved			INSTS			INTBIT
Reset	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R
Address	UART0_IIR = 00C2h, UART1_IIR = 00D2h							

Note: *x* indicates UART[1:0]; R = read only.

Bit	Description
[7] FSTS	**FIFO Enable** 0: FIFO is disabled. 1: FIFO is enabled.
[6:4]	**Reserved** These bits are reserved and must be programmed to 000.

Phase Frequency Detector

The Phase Frequency Detector (PFD) is a digital block. The two inputs are the reference clock (XTAL oscillator; see the On-Chip Oscillators chapter on page 332) and the PLL divider output. The two outputs drive the internal charge pump and represent the error (or difference) between the falling edges of the PFD inputs.

Charge Pump

The Charge Pump is an analog block that is driven by two digital inputs from the PFD that control its programmable current sources. The internal current source contains four programmable values: 1.5 mA, 1 mA, 500 µA, and 100 µA. These values are selected by PLL_CTRL1[7:6]. The selected current drive is sinked/sourced onto the loop-filter node according to the error (or difference) between the falling edges of the PFD inputs. Ideally, when the PLL is locked, there are no errors (error = 0) and no current is sourced/sinked onto the loop-filter node.

Voltage-Controlled Oscillator

The Voltage-Controlled Oscillator (VCO) is an analog block that exhibits an output frequency proportional to its input voltage. The VCO input is driven from the charge pump and filtered via the off-chip loop filter.

Loop Filter

The Loop Filter comprises off-chip passive components (usually 1 resistor and 2 capacitors) that filter/integrate charge from the internal charge pump. The filtered node also drives the VCO input, which creates a proportional frequency output. When PLL is not used, the Loop Filter pin must not be connected.

Divider

The Divider is a digital, programmable downcounter. The divider input is driven by the VCO. The divider output drives the PFD. The function of the Divider is to divide the frequency of its input signal by a programmable factor *N* and supply the result in its output.

MUX/CLK Sync

The MUX/CLK Sync is a digital, software-controllable multiplexer that selects between PLL or the XTAL oscillator as the system clock (SCLK). A PLL source is selected only after the PLL is *locked* (via the lock detect block) to allow glitch-free clock switching.

Table 155. PLL Control Register 0 (PLL_CTL0)

Bit	7	6	5	4	3	2	1	0
Field	CHRP_CTL1		Reserved		LDS_CTL1		CLK_MUX	
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W
Address	005Eh							

Note: R = read only; R/W = read/write.

Bit	Description
[7:6] CHRP_CTL1	**Charge Pump** 00: Charge pump current = 100µA. 01: Charge pump current = 500µA. 10: Charge pump current = 1.0mA. 11: Charge pump current = 1.5mA.
[5:4]	**Reserved** These bits are reserved and must be programmed to 00.
[3:2] LDS_CTL1	**Lock Control** 00: Lock criteria: 8 consecutive cycles of 20ns. 01: Lock criteria: 16 consecutive cycles of 20 ns. 10: Lock criteria: 8 consecutive cycles of 400 ns. 11: Lock criteria: 16 consecutive cycles of 400 ns.
[1:0] CLK_MUX	**Clock Source** 00: System clock source is the external crystal oscillator. 01: System clock source is the PLL[2]. 10: System clock source is the Real-Time Clock crystal oscillator. 11: Reserved (previous select is preserved).

Notes:
1. Bits are programmed only when the PLL is disabled. The PLL is disabled when PLL_CTL1 bit 0 is equal to 0.
2. PLL cannot be selected when disabled or *out of lock*.

PLL Control Register 1

The PLL is enabled using this register. PLL lock-detect status, the PLL interrupt signals and the PLL interrupt enables are accessed via this register. A brief description of each of these PLL Control Register 1 attributes is listed below, and further described in Table 156.

Lock Status (LCK_STATUS)

The current lock bit out of the PLL is synchronized and read via this bit.

Bit	Description (Continued)
[2] INT_LOCK_EN	**PLL Lock Interrupt Enable** 0: Interrupt generation for PLL locked condition (Bit 4) is disabled. 1: Interrupt generation for PLL locked condition is enabled.
[1] INT_UNLOCK_EN	**PLL Unlock Interrupt Enable** 0: Interrupt generation for PLL unlocked condition (Bit 3) is disabled. 1: Interrupt generation for PLL unlocked condition is enabled.
[0] PLL_ENABLE	**PLL Enable** 0: PLL is disabled.* 1: PLL is enabled.

Note: *PLL cannot be disabled if the CLK_MUX bit of PLL_CTL0[1:0] is set to 01, because the PLL is selected as the clock source.

PLL Characteristics

The operating and testing characteristics for the PLL are described in Table 157.

Table 157. PLL Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
I_{OHCP_OUT}	High level output current for CP_OUT pin (programmed value ±42%)	$3.0 < V_{DD} < 3.6$ $0.6 < PD\_OUT < V_{DD} – 0.6$ PLL_CTL0[7:6] = 11	–0.86	–1.50	–2.13	mA
I_{OLCP_OUT}	Low level output current for CP_OUT pin (programmed value ±42%)	$3.0 < V_{DD} < 3.6$ $0.6 < PD\_OUT < V_{DD} – 0.6$ PLL_CTL0[7:6] = 11	0.86	1.50	2.13	mA
I_{OHCP_OUT}	High level output current for CP_OUT pin (programmed value ±42%)	$3.0 < V_{DD} < 3.6$ $0.6 < PD\_OUT < V_{DD} – 0.6$ PLL_CTL0[7:6] = 10	–0.42	–1.0	–1.42	mA
I_{OLCP_OUT}	Low level output current for CP_OUT pin (programmed value ±42%)	$3.0 < V_{DD} < 3.6$ $0.6 < PD\_OUT < V_{DD} – 0.6$ PLL_CTL0[7:6] = 10	0.42	1.0	1.42	mA
I_{OHCP_OUT}	High level output current for CP_OUT pin (programmed value ±42%)	$3.0 < V_{DD} < 3.6$ $0.6 < PD\_OUT < V_{DD} – 0.6$ PLL_CTL0[7:6] = 01	–210	–500	–710	µA
I_{OLCP_OUT}	Low level output current for CP_OUT pin (programmed value ±42%)	$3.0 < V_{DD} < 3.6$ $0.6 < PD\_OUT < V_{DD} – 0.6$ PLL_CTL0[7:6] = 01	210	500	710	µA
I_{OHCP_OUT}	High level output current for CP_OUT pin (programmed value ±42%)	$3.0 < V_{DD} < 3.6$ $0.6 < PD\_OUT < V_{DD} – 0.6$ PLL_CTL0[7:6] = 00	–42	–100	–142	µA

Table 161. Exchange Instructions

Mnemonic	Instruction
EX	Exchange registers
EXX	Exchange CPU multibyte register banks

Table 162. Input/Output Instructions

Mnemonic	Instruction
IN	Input from I/O
IN0	Input from I/O on Page 0
IND (INDR)	Input from I/O and Decrement (with Repeat)
INDRX	Input from I/O and Decrement Memory Address with Stationary I/O Address
IND2 (IND2R)	Input from I/O and Decrement (with Repeat)
INDM (INDMR)	Input from I/O and Decrement (with Repeat)
INI (INIR)	Input from I/O and Increment (with Repeat)
INIRX	Input from I/O and Increment Memory Address with Stationary I/O Address
INI2 (INI2R)	Input from I/O and Increment (with Repeat)
INIM (INIMR)	Input from I/O and Increment (with Repeat)
OTDM (OTDMR)	Output to I/O and Decrement (with Repeat)
OTDRX	Output to I/O and Decrement Memory Address with Stationary I/O Address
OTIM (OTIMR)	Output to I/O and Increment (with Repeat)
OTIRX	Output to I/O and Increment Memory Address with Stationary I/O Address
OUT	Output to I/O
OUT0	Output to I/0 on Page 0
OUTD (OTDR)	Output to I/O and Decrement (with Repeat)
OUTD2 (OTD2R)	Output to I/O and Decrement (with Repeat)
OUTI (OTIR)	Output to I/O and Increment (with Repeat)
OUTI2 (OTI2R)	Output to I/O and Increment (with Repeat)
TSTIO	Test I/O

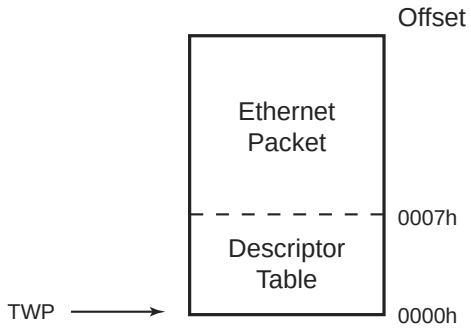


Figure 61. Descriptor Table

Note: For an official description of an Ethernet packet, refer to the IEEE 802.3 specification, Figure 3-1.

The descriptor table contains three entries: the next pointer (NP), the packet size (Pkt_Size) and the packet status (Stat), as shown in Figure 62.

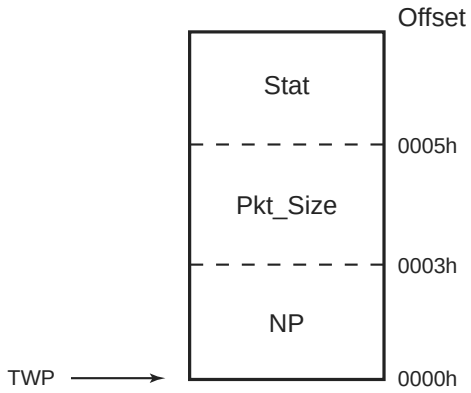


Figure 62. Descriptor Table Entries

NP is a 24-bit pointer to the start of the next packet. Pkt_Size contains the number of bytes of data in the Ethernet packet, including the four CRC bytes, but does not contain the seven descriptor table bytes. Stat contains the status of the packet. Stat differs for Transmit and Receive packets. See Table 179 and 180.

EMAC Configuration Register 4

The EMAC Configuration Register 4, shown in Table 186, controls pause control frame behavior, back pressure, and receive frame acceptance.

Table 186. EMAC Configuration Register 4 (EMAC_CFG4)

Bit	7	6	5	4	3	2	1	0
Field	Reserved	TPCF	THDF	PARF	RxFC	TxFC	TPAUSE	RxEN
Reset	0	0	0	0	0	0	0	0
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	0024h							

Note: R = read only; R/W = read/write.

Bit	Description
[7]	**Reserved** This bit is reserved and must be programmed to 0.
[6] TPCF	**Transmit Pause Control Frame** 0: Do not transmit a pause control frame. 1: Transmit pause control frame (FULL-DUPLEX Mode). TPCF continually sends pause control frames until negated.
[5] THDF	**Transmit Half-Duplex Frame** 0: Disable back pressure. 1: EMAC asserts back pressure on the link. Back pressure causes the preamble to be transmitted, raising the carrier sense (HALF-DUPLEX Mode).
[4] PARF	**Frame Receive** 0: Only accept frames that meet preset criteria (that is, address, CRC, length, etc.). 1: All frames are received regardless of address, CRC, length, etc.
[3] RxFC	**Receive Pause Control Frames** 0: EMAC ignores received pause control frames. 1: EMAC acts upon pause control frames received.
[2] TxFC	**Transmit Pause Control Frames** 0: Pause control frames are not allowed to be transmitted. 1: Pause control frames are allowed to be transmitted.
[1] TPAUSE	**Pause Condition** 0: Do not force a pause condition. 1: Force a pause condition while this bit is asserted.
[0] RxEN	**Pause Control Frames** 0: EMAC receiver disabled. 1: EMAC receiver enabled.

Table 198. EMAC Hash Table Register (EMAC_HTBL_*x*)

Bit	7	6	5	4	3	2	1	0
Field	EMAC_HTBL_*x*							
EMAC_HTBL_0 Reset	0	0	0	0	0	0	0	0
EMAC_HTBL_1 Reset	0	0	0	0	0	0	0	0
EMAC_HTBL_2 Reset	0	0	0	0	0	0	0	0
EMAC_HTBL_3 Reset	0	0	0	0	0	0	0	0
EMAC_HTBL_4 Reset	0	0	0	0	0	0	0	0
EMAC_HTBL_5 Reset	0	0	0	0	0	0	0	0
EMAC_HTBL_6 Reset	0	0	0	0	0	0	0	0
EMAC_HTBL_7 Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	EMAC_HTBL_0 = 0033h, EMAC_HTBL_1 = 0034h, EMAC_HTBL_2 = 0035h, EMAC_HTBL_3 = 0036h, EMAC_HTBL_4 = 0037h, EMAC_HTBL_5 = 0038h, EMAC_HTBL_6 = 0039h, EMAC_HTBL_7 = 003Ah							

Note: R/W = read/write; x indicates reset bits in the range [7:0].

Bit	Description
[7:0] EMAC_HTBL_*x*	00h–FFh: This field is the hash table. The 64 bit hash table is {EMAC_HTBL_7, EMAC_HTBL_6, EMAC_HTBL_5, EMAC_HTBL_4, EMAC_HTBL_3, EMAC_HTBL_2, EMAC_HTBL_1, EMAC_HTBL_0}.

EMAC MII Management Register

The EMAC MII Management Register, shown in Table 199, is used to control the external PHY attached to the MII.

Table 199. EMAC MII Management Register (EMAC_MIIMGT)

Bit	7	6	5	4	3	2	1	0
Field	LCTLD	RSTAT	SCINC	SCAN	SPRE	CLKS		
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	003Bh							

Note: R/W = read/write.

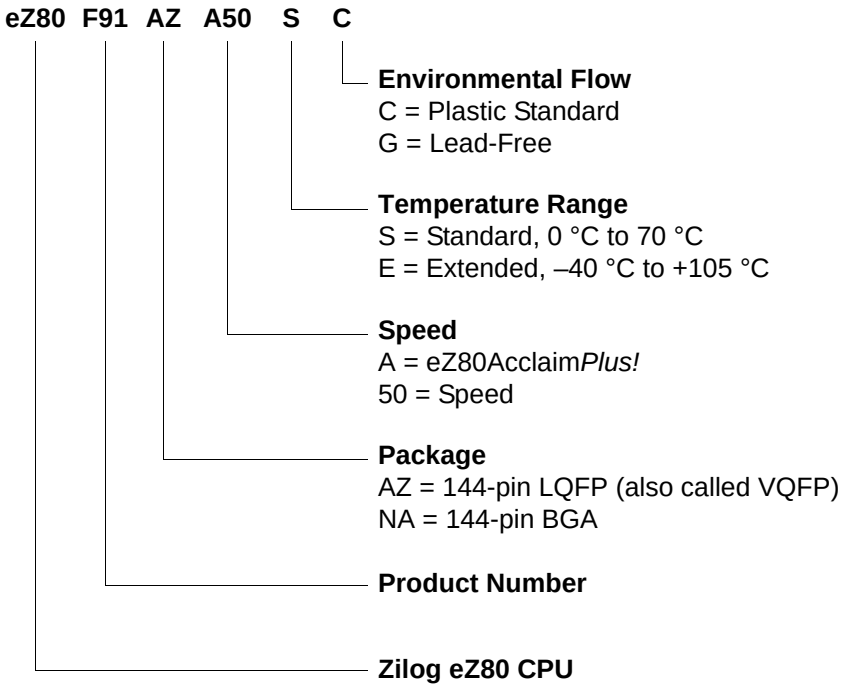
Bit	Description
[7] LCTLD	**Configuration Data** 0: No operation. 1: A rising edge causes the CTLD control data to be transmitted to external PHY if MII is not busy. This bit is self-clearing.
[6] RSTAT	**Read Status** 0: No operation. 1: A rising edge causes status to be read from external PHY via PRSD[15:0] bus if MII is not busy. This bit is self-clearing.
[5] SCINC	**Scan Address Increments** 0: Normal operation. 1: Scan PHY address increments upon SCAN cycle. The SCAN bit must also be set for the PHY address to increment after each scan. The scanning starts at the EMAC_FIAD and increments up to 1Fh. It then returns to the EMAC_FIAD address.
[4] SCAN	**Scan Mode Read** 0: Normal operation. 1: Perform continuous read cycles via MII management. While in SCAN Mode, the EMAC_ISTAT[MGTDONE] bit is set when the current PHY read has completed. At this time, the EMAC_PRSD Register holds the read data and the EMAC_MIISTAT[4:0] holds the address of the PHY for which the EMAC_PRSD data pertains.
[3] SPRE	**Suppress Preamble** 0: Normal preamble. 1: Suppress the MDO preamble. MDO is management data output, an internal signal driven from the MDIO pin.
[2:0] CLKS	**Serial Clock Divisor** Programmable divisor that produces MDC from SCLK. MDC is the management data clock pin, which clocks MDIO data to and from the PHY. its frequency is SCLK divided by the MDC clock divider. 000: MDC = SCLK ÷ 4. 001: MDC = SCLK ÷ 4. 010: MDC = SCLK ÷ 6. 011: MDC = SCLK ÷ 8. 100: MDC = SCLK ÷ 10. 101: MDC = SCLK ÷ 14. 110: MDC = SCLK ÷ 20. 111: MDC = SCLK ÷ 28.

EMAC PHY Configuration Data Register, Low and High Byte

The low and high bytes of the EMAC PHY Configuration Data Register, shown in Tables 200 and 201, represent the configuration data written to the external PHY. The EMAC_CTLD_H and EMAC_CTLD_L registers form a 16-bit register. These registers are loaded with data to be sent via the MDIO pin to the PHY. The PHY is selected by setting the EMAC_FIAD. The register inside the PHY is selected by setting EMAC_RGAD.

Part Number Description

Zilog part numbers consists of number of components as described below:



Example. Part number eZ80F91AZA50SC is an eZ80Acclaim*Plus!* product in a 144-pin LQFP package operating with a 50MHz external clock frequency over a 0ºC to +70ºC temperature range and built using the Plastic Standard environmental flow.