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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	Ethernet, I²C, SPI, SSC, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	69
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at32uc3a1128-aut

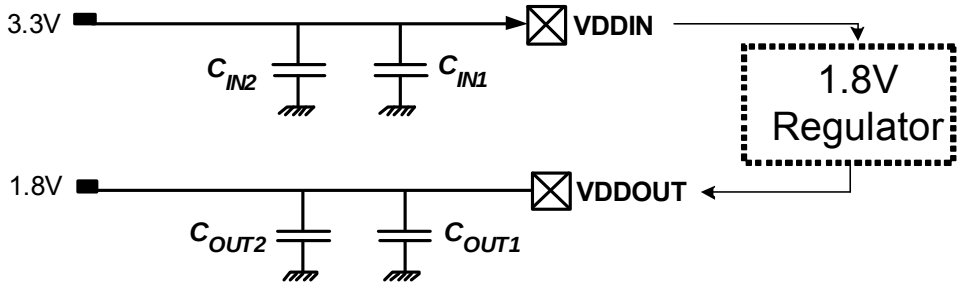
6.2 Voltage Regulator

6.2.1 Single Power Supply

The AT32UC3A embeds a voltage regulator that converts from 3.3V to 1.8V. The regulator takes its input voltage from VDDIN, and supplies the output voltage on VDDOUT. VDDOUT should be externally connected to the 1.8V domains.

Adequate input supply decoupling is mandatory for VDDIN in order to improve startup stability and reduce source voltage drop. Two input decoupling capacitors must be placed close to the chip.

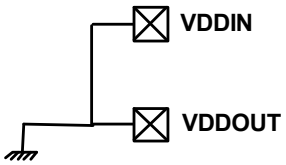
Adequate output supply decoupling is mandatory for VDDOUT to reduce ripple and avoid oscillations. The best way to achieve this is to use two capacitors in parallel between VDDOUT and GND as close to the chip as possible



Refer to Section 38.3 on page 765 for decoupling capacitors values and regulator characteristics

6.2.2 Dual Power Supply

In case of dual power supply, VDDIN and VDDOUT should be connected to ground to prevent from leakage current.



The following GPIO registers are mapped on the local bus:

Table 12-2. Local bus mapped GPIO registers

Port	Register	Mode	Local Bus Address	Access
0	Output Driver Enable Register (ODER)	WRITE	0x4000_0040	Write-only
		SET	0x4000_0044	Write-only
		CLEAR	0x4000_0048	Write-only
		TOGGLE	0x4000_004C	Write-only
	Output Value Register (OVR)	WRITE	0x4000_0050	Write-only
		SET	0x4000_0054	Write-only
		CLEAR	0x4000_0058	Write-only
		TOGGLE	0x4000_005C	Write-only
	Pin Value Register (PVR)	-	0x4000_0060	Read-only
1	Output Driver Enable Register (ODER)	WRITE	0x4000_0140	Write-only
		SET	0x4000_0144	Write-only
		CLEAR	0x4000_0148	Write-only
		TOGGLE	0x4000_014C	Write-only
	Output Value Register (OVR)	WRITE	0x4000_0150	Write-only
		SET	0x4000_0154	Write-only
		CLEAR	0x4000_0158	Write-only
		TOGGLE	0x4000_015C	Write-only
	Pin Value Register (PVR)	-	0x4000_0160	Read-only
2	Output Driver Enable Register (ODER)	WRITE	0x4000_0240	Write-only
		SET	0x4000_0244	Write-only
		CLEAR	0x4000_0248	Write-only
		TOGGLE	0x4000_024C	Write-only
	Output Value Register (OVR)	WRITE	0x4000_0250	Write-only
		SET	0x4000_0254	Write-only
		CLEAR	0x4000_0258	Write-only
		TOGGLE	0x4000_025C	Write-only
	Pin Value Register (PVR)	-	0x4000_0260	Read-only

  - Optional Manchester Encoding
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit
- IrDA modulation and demodulation
  - Communication at up to 115.2 Kbps
- Test Modes
  - Remote Loopback, Local Loopback, Automatic Echo
- SPI Mode
  - Master or Slave
  - Serial Clock Programmable Phase and Polarity
  - SPI Serial Clock (SCK) Frequency up to Internal Clock Frequency PBA/4
- Supports Connection of Two Peripheral DMA Controller Channels (PDC)
  - Offers Buffer Transfer without Processor Intervention

12.11.8 Serial Synchronous Controller

- Provides serial synchronous communication links used in audio and telecom applications (with CODECs in Master or Slave Modes, I2S, TDM Buses, Magnetic Card Reader, etc.)
- Contains an independent receiver and transmitter and a common clock divider
- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

12.11.9 Timer Counter

- Three 16-bit Timer Counter Channels
- Wide range of functions including:
  - Frequency Measurement
  - Event Counting
  - Interval Measurement
  - Pulse Generation
  - Delay Timing
  - Pulse Width Modulation
  - Up/down Capabilities
- Each channel is user-configurable and contains:
  - Three external clock inputs
  - Five internal clock inputs
  - Two multi-purpose input/output signals
- Two global registers that act on all three TC Channels

12.11.10 Pulse Width Modulation Controller

- 7 channels, one 20-bit counter per channel
- Common clock generator, providing Thirteen Different Clocks
  - A Modulo n counter providing eleven clocks
  - Two independent Linear Dividers working on modulo n counter outputs
- Independent channel programming
  - Independent Enable Disable Commands
  - Independent Clock
  - Independent Period and Duty Cycle, with Double Bufferization
  - Programmable selection of the output waveform polarity
  - Programmable center or left aligned output waveform

PAGEN: Page number

The PAGEN field is used to address a page or fuse bit for certain operations. In order to simplify programming, the PAGEN field is automatically updated every time the page buffer is written to. For every page buffer write, the PAGEN field is updated with the page number of the address being written to. Hardware automatically masks writes to the PAGEN field so that only bits representing valid page numbers can be written, all other bits in PAGEN are always 0. As an example, in a flash with 1024 pages (page 0 - page 1023), bits 15:10 will always be 0.

Table 18-6. Semantic of PAGEN field in different commands

Command	PAGEN description
No operation	Not used
Write Page	The number of the page to write
Clear Page Buffer	Not used
Lock region containing given Page	Page number whose region should be locked
Unlock region containing given Page	Page number whose region should be unlocked
Erase All	Not used
Write General-Purpose Fuse Bit	GPFUSE #
Erase General-Purpose Fuse Bit	GPFUSE #
Set Security Bit	Not used
Program GP Fuse Byte	WriteData[7:0], ByteAddress[2:0]
Erase All GP Fuses	Not used
Quick Page Read	Page number
Write User Page	Not used
Erase User Page	Not used
Quick Page Read User Page	Not used

KEY: Write protection key

This field should be written with the value 0xA5 to enable the command defined by the bits of the register. If the field is written with a different value, the write is not performed and no action is started.

This field always reads as 0.

19.7.5 Bus Matrix Master Remap Control Register

Register Name: MRCR

Access Type: Read/Write

Reset: 0x0000_0000

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
RCB15	RCB14	RCB13	RCB12	RCB11	RCB10	RCB9	RCB8
7	6	5	4	3	2	1	0
RCB7	RCB6	RCB5	RCB4	RCB3	RCB2	RCB1	RCB0

- **RCB: Remap Command Bit for Master x**

0: Disable remapped address decoding for the selected Master

1: Enable remapped address decoding for the selected Master

19.7.6 Bus Matrix Special Function Registers

Register Name: SFR0...SFR15

Access Type: Read/Write

Reset:

31	30	29	28	27	26	25	24
SFR							

23	22	21	20	19	18	17	16
SFR							

15	14	13	12	11	10	9	8
SFR							

7	6	5	4	3	2	1	0
SFR							

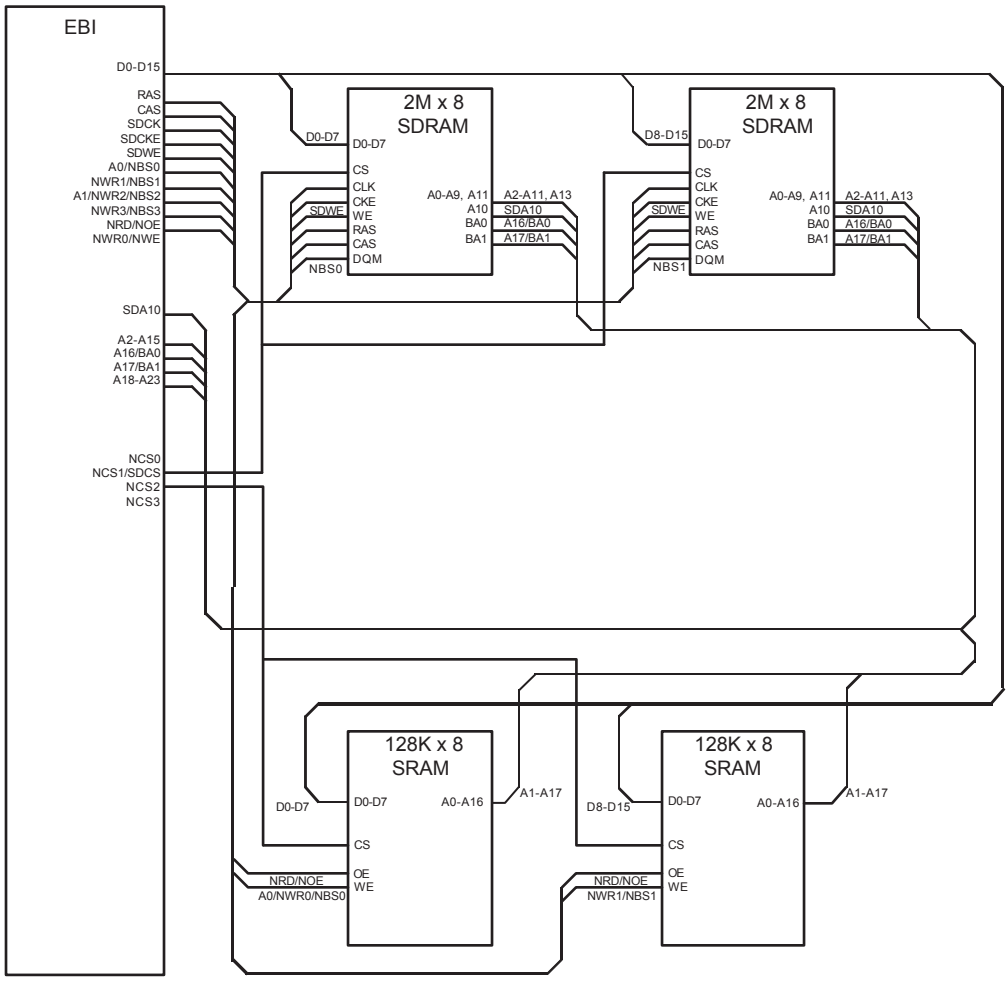
- **SFR: Special Function Register Fields**

The bitfields of these registers are described in the Peripherals chapter.

20.5.2 Connection Examples

Figure 20-2 shows an example of connections between the EBI and external devices.

Figure 20-2. EBI Connections to Memory Devices



transfer. The address will be increased by either 1, 2 or 4 depending on the size of the DMA transfer (Byte, Half-Word or Word). The Memory Address Register can be read at any time during transfer.

21.4.3 Transfer Counter

Each channel has a 16-bit Transfer Counter Register (TCR). This register must be programmed with the number of transferred to be performed. TCR should contain the number of data items to be transferred independently of the transfer size. The Transfer Counter Register can be read at any time during transfer to see the number of remaining transfers.

21.4.4 Reload Registers

Both the Memory Address Register and the Transfer Counter Register have a reload register, respectively Memory Address Reload Register (MARR) and Transfer Counter Reload Register (TCRR). These registers provide the possibility for the PDCA to work on two memory buffers for each channel. When one buffer has completed, MAR and TCR will be reloaded with the values in MARR and TCRR. The reload logic is always enabled and will trigger if the TCR reaches zero while TCRR holds a non-zero value.

21.4.5 Peripheral Selection

The Peripheral Select Register decides which peripheral should be connected to the PDCA channel. Configuring PSR will both select the direction of the transfer (memory to peripheral or peripheral to memory), which handshake interface to use, and the address of the peripheral holding register.

21.4.6 Transfer Size

The transfer size can be set individually for each channel to be either Byte, Half-Word or Word (8-bit, 16-bit or 32-bit respectively). Transfer size is set by programming the SIZE bit-field in the Mode Register (MR).

21.4.7 Enabling and Disabling

Each DMA channel is enabled by writing ‘1’ to the Transfer Enable bit (TEN) in the Control Register (CR) and disabled by writing ‘1’ to the Transfer Disable bit (TDIS). The current status can be read from the Status Register (SR).

21.4.8 Interrupts

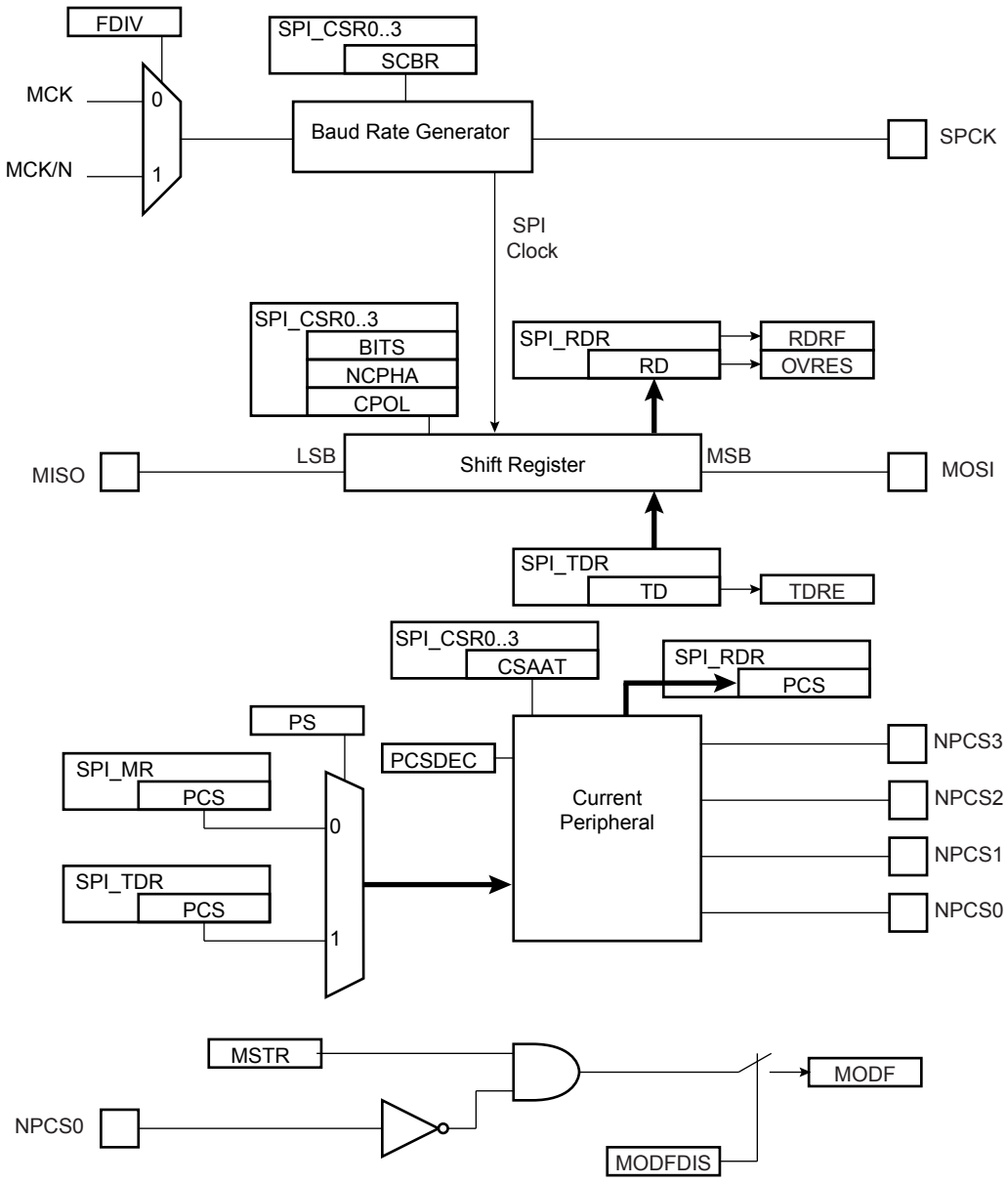
Interrupts can be enabled by writing to the Interrupt Enable Register (IER) and disabled by writing to Interrupt Disable Register (IDR). The Interrupt Mask Register (IMR) can be read to see whether an interrupt is enabled or not. The current status of an interrupt source can be read through the Interrupt Status Register (ISR).

The PDCA has three interrupt sources:

- Reload Counter Zero - The Transfer Counter Reload Register is zero.
- Transfer Finished - Both the Transfer Counter Register and Transfer Counter Reload Register are zero.
- Transfer Error - An error has occurred in accessing memory.

23.7.3.1 Master Mode Block Diagram

Figure 23-5. Master Mode Block Diagram



Access: Read-only

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
RXDATA							

- **RXDATA: Master or Slave Receive Holding Data**

24.14.12 TWI Transmit Holding Register

Name: THR

Access: Read-write

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
TXDATA							

- **TXDATA: Master or Slave Transmit Holding Data**

After initialization, as soon as DS field is modified and self-refresh mode is activated, the Extended Mode Register is accessed automatically and DS bits are updated before entry in self-refresh mode.

- **TIMEOUT: Time to define when low-power mode is enabled**

00	The SDRAM controller activates the SDRAM low-power mode immediately after the end of the last transfer.
01	The SDRAM controller activates the SDRAM low-power mode 64 clock cycles after the end of the last transfer.
10	The SDRAM controller activates the SDRAM low-power mode 128 clock cycles after the end of the last transfer.
11	Reserved.

29.7.28 MACB Statistic Registers

These registers reset to zero on a read and stick at all ones when they count to their maximum value. They should be read frequently enough to prevent loss of data. The receive statistics registers are only incremented when the receive enable bit is set in the network control register. To write to these registers, bit 7, WESTAT, in the network control register, NCR, must be set. The statistics register block contains the following registers.

29.7.28.1 Pause Frames Received Register

Register Name: PFR

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
FROK							
7	6	5	4	3	2	1	0
FROK							

- **FROK: Pause Frames received OK**

A 16-bit register counting the number of good pause frames received. A good frame has a length of 64 to 1518 (1536 if bit 8, BIG, in network configuration register, NCFGR, is set, 10240 if bit 3, JFRAME in network configuration register, NCFGR, is set) and has no FCS, alignment or receive symbol errors.

29.7.28.2 Frames Transmitted OK Register

Register Name: FTO

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
FTOK							
15	14	13	12	11	10	9	8
FTOK							
7	6	5	4	3	2	1	0
FTOK							

- **FTOK: Frames Transmitted OK**

A 24-bit register counting the number of frames successfully transmitted, i.e., no underrun and not too many retries.

30.8.2.19 USB Device DMA Channel X Control Register (UDDMAX_CONTROL)

Offset: 0x0318 + (X - 1) . 0x10

Register Name: *UDDMAX_CONTROL*, X in [1..6]

Access Type: Read/Write

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
CH_BYTE_LENGTH							
rwu							
0	0	0	0	0	0	0	0
23	22	21	20	19	18	17	16
CH_BYTE_LENGTH							
rwu							
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
BURST_LOCK_EN	DESC_LD_IRQ_EN	EOBUFF_IRQ_EN	EOT_IRQ_EN	DMAEND_EN	BUFF_CLOSE_IN_EN	LD_NXT_CH_DESC_EN	CH_EN
rwu	rwu	rwu	rwu	rwu	rwu	rwu	rwu
0	0	0	0	0	0	0	0

- **CH_EN: Channel Enable**

Set this bit to enable this channel data transfer.

Clear this bit to disable the channel data transfer.

This may be used to start or resume any requested transfer.

This bit is cleared by hardware when the HSB source channel is disabled at end of dma buffer.

- **LD_NXT_CH_DESC_EN: Load Next Channel Descriptor Enable**

Set this bit to allow automatic next descriptor loading at the end of the channel transfer.

Clear this bit to disable this feature.

If set, the dma channel controller loads the next descriptor when the UDDMAX_STATUS.CH_EN bit is reset due to software of hardware event (for example at the end of the current transfer).

- **BUFF_CLOSE_IN_EN: Buffer Close Input Enable**

Set this bit to automatically closed the current dma transfer at the end of the usb OUT data transfer (received short packet).

Clear this bit to disable this feature.

- **DMAEND_EN: End of DMA Buffer Output Enable**

Set this bit to properly complete the usb transfer at the end of the dma transfer.

For IN endpoint, it means that a short packet (or a Zero Length Packet) will be sent to the usb line to properly closed the usb transfer at the end of the dma transfer.

For OUT endpoint, it means that all the banks will be properly released. (NBUSYBK=0) at the end of the dma transfer.

- **ACPA: RA Compare Effect on TIOA**

ACPA		Effect
0	0	none
0	1	set
1	0	clear
1	1	toggle

- **ACPC: RC Compare Effect on TIOA**

ACPC		Effect
0	0	none
0	1	set
1	0	clear
1	1	toggle

- **AEEVT: External Event Effect on TIOA**

AEEVT		Effect
0	0	none
0	1	set
1	0	clear
1	1	toggle

- **ASWTRG: Software Trigger Effect on TIOA**

ASWTRG		Effect
0	0	none
0	1	set
1	0	clear
1	1	toggle

- **BCPB: RB Compare Effect on TIOB**

BCPB		Effect
0	0	none

32.7.7 PWM Interrupt Disable Register

Register Name: IDR

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	CHID6	CHID5	CHID4	CHID3	CHID2	CHID1	CHID0

- **CHIDx: Channel ID.**

0 = No effect.

1 = Disable interrupt for PWM channel x.

33.7.2 Mode Register

Name: MR

Access Type: Read/Write

Offset: 0x04

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
–	–	–	–	SHTIM			
23	22	21	20	19	18	17	16
–	–	–	STARTUP				
15	14	13	12	11	10	9	8
–	–	PRESCAL					
7	6	5	4	3	2	1	0
–	–	SLEEP	LOWRES	TRGSEL			TRGEN

- **SHTIM: Sample & Hold Time**
  Sample & Hold Time = (SHTIM+1) / ADCClock
- **STARTUP: Start Up Time**
  Startup Time = (STARTUP+1) * 8 / ADCClock
- **PRESCAL: Prescaler Rate Selection**
  ADCClock = CLK_ADC / ((PRESCAL+1) * 2)
- **SLEEP: Sleep Mode**

SLEEP	Selected Mode
0	Normal Mode
1	Sleep Mode

- **LOWRES: Resolution**

LOWRES	Selected Resolution
0	10-bit resolution
1	8-bit resolution

- **TRGSEL: Trigger Selection**

TRGSEL			Selected TRGSEL
0	0	0	Internal Trigger 0, depending of chip integration
0	0	1	Internal Trigger 1, depending of chip integration
0	1	0	Internal Trigger 2, depending of chip integration
0	1	1	Internal Trigger 3, depending of chip integration
1	0	0	Internal Trigger 4, depending of chip integration

34.7.3 Audio Bitstream DAC Interrupt Mask Register

Name: IMR

Access Type: Read-only

31	30	29	28	27	26	25	24
-	-	TX_READY	UNDERRUN	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

- **UNDERRUN: Underrun Interrupt Mask**

0: The Audio Bitstream DAC Underrun interrupt is disabled.

1: The Audio Bitstream DAC Underrun interrupt is enabled.

- **TX_READY: TX Ready Interrupt Mask**

0: The Audio Bitstream DAC TX Ready interrupt is disabled.

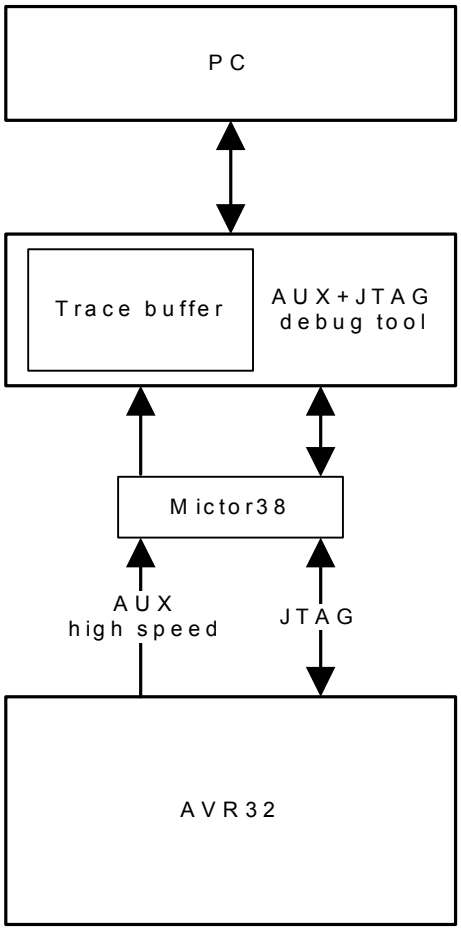
1: The Audio Bitstream DAC TX Ready interrupt is enabled.

Debug tools utilizing the AUX port should connect to the device through a Nexus-compliant Mictor-38 connector, as described in the AVR32UC Technical Reference manual. This connector includes the JTAG signals and the RESET_N pin, giving full access to the programming and debug features in the device.

Table 35-1. Auxiliary port signals

Signal	Direction	Description
MCKO	Output	Trace data output clock
MDO[5:0]	Output	Trace data output
MSEO[1:0]	Output	Trace frame control
EVTI_N	Input	Event In
EVTO_N	Output	Event Out

Figure 35-3. AUX+JTAG based debugger



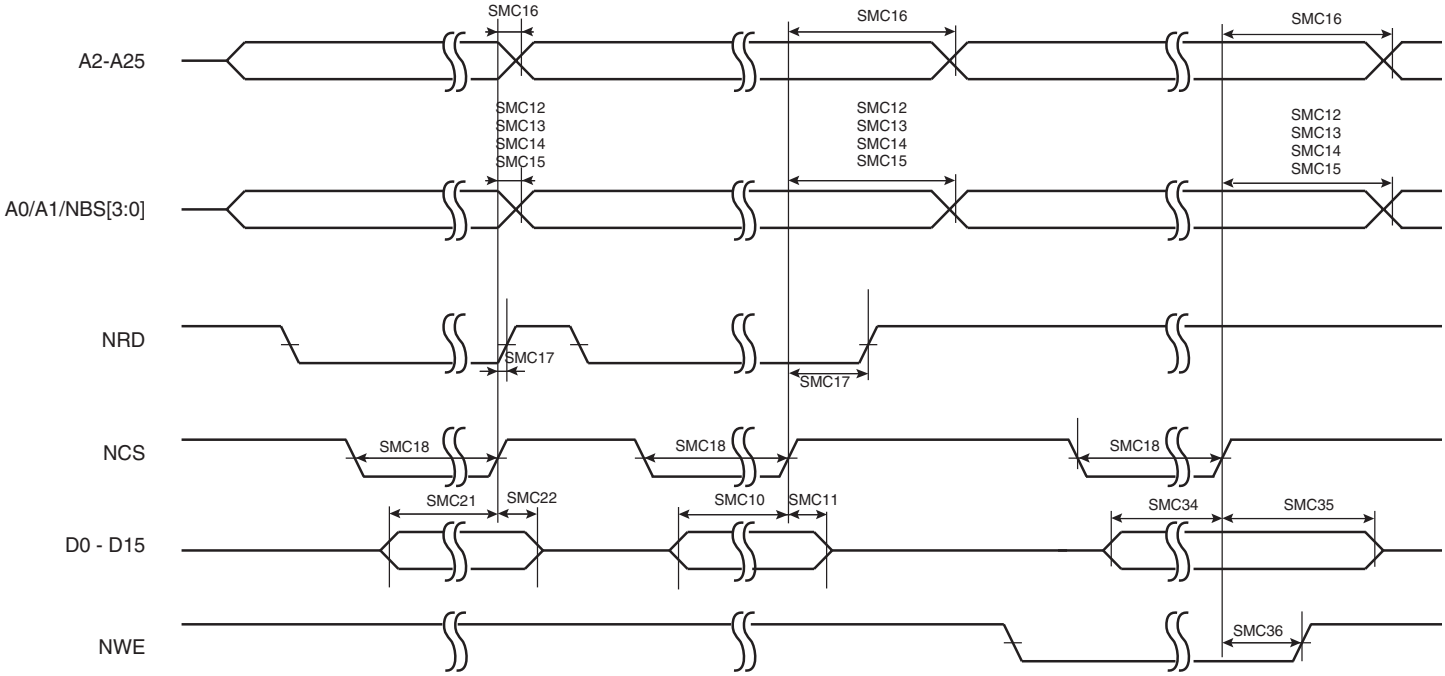
35.4.3.1 Trace operation

Trace features are enabled by writing OCD registers by JTAG. The OCD extracts the trace information from the CPU, compresses this information and formats it into variable-length messages according to the Nexus standard. The messages are buffered in a 16-frame transmit queue, and are output on the AUX port one frame at a time.

Table 38-26. SMC Write Signals with No Hold Settings (NWE Controlled only).

Symbol	Parameter	Min	Units
SMC_{37}	NWE Rising to A2-A25 Valid	5.4	ns
SMC_{38}	NWE Rising to NBS0/A0 Valid	5	
SMC_{39}	NWE Rising to NBS1 Change	5	
SMC_{40}	NWE Rising to A1/NBS2 Change	5	
SMC_{41}	NWE Rising to NBS3 Change	5	
SMC_{42}	NWE Rising to NCS Rising	5.1	
SMC_{43}	Data Out Valid before NWE Rising	(nwe pulse length - 1) * t_{CPSMC} - 1.2	
SMC_{44}	Data Out Valid after NWE Rising	5	
SMC_{45}	NWE Pulse Width	nwe pulse length * t_{CPSMC} - 0.9	

Figure 38-2. SMC Signals for NCS Controlled Accesses.



If the ADC sleep mode is activated when the ADC is idle the ADC will not enter sleep mode before after the next AD conversion.

Fix/Workaround

Activate the sleep mode in the mode register and then perform an AD conversion.

41.5.11 ABDAC

1. **Audio Bitstream DAC is not functional.**
   Fix/Workaround
   Do not use the ABDAC on revE.

41.5.12 FLASHC

1. **The address of Flash General Purpose Fuse Register Low (FGPFRLO) is 0xFFFE140C on revE instead of 0xFFFE1410.**
   Fix/Workaround
   None.

2. **The command Quick Page Read User Page(QPRUP) is not functional.**
   Fix/Workaround
   None.

3. **PAGEN Semantic Field for Program GP Fuse Byte is WriteData[7:0], ByteAddress[1:0] on revision E instead of WriteData[7:0], ByteAddress[2:0].**
   Fix/Workaround
   None.

4. **On AT32UC3A0512 and AT32UC3A1512, corrupted read in flash after FLASHC WP, EP, EA, WUP, EUP commands may happen**
   - After a FLASHC Write Page (WP) or Erase Page (EP) command applied to a page in a given half of the flash (first or last 256 kB of flash), reading (data read or code fetch) the other half of the flash may fail. This may lead to an exception or to other errors derived from this corrupted read access.
   - After a FLASHC Erase All (EA) command, reading (data read or code fetch) the flash may fail. This may lead to an exception or to other errors derived from this corrupted read access.
   - After a FLASHC Write User Page (WUP) or Erase User Page (EUP) command, reading (data read or code fetch) the second half (last 256 kB) of the flash may fail. This may lead to an exception or to other errors derived from this corrupted read access.

   Fix/Workaround
   Flashc WP, EP, EA, WUP, EUP commands: these commands must be issued from RAM or through the EBI. After these commands, read twice one flash page initialized to 00h in each half part of the flash.

41.5.13 RTC

1. **Writes to control (CTRL), top (TOP) and value (VAL) in the RTC are discarded if the RTC peripheral bus clock (PBA) is divided by a factor of four or more relative to the HSB clock.**
   Fix/Workaround
   Do not write to the RTC registers using the peripheral bus clock (PBA) divided by a factor of four or more relative to the HSB clock.