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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LED, LVD, POR, PWM
Number of I/O	23
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 13x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SO
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc68hc908jl8cdw

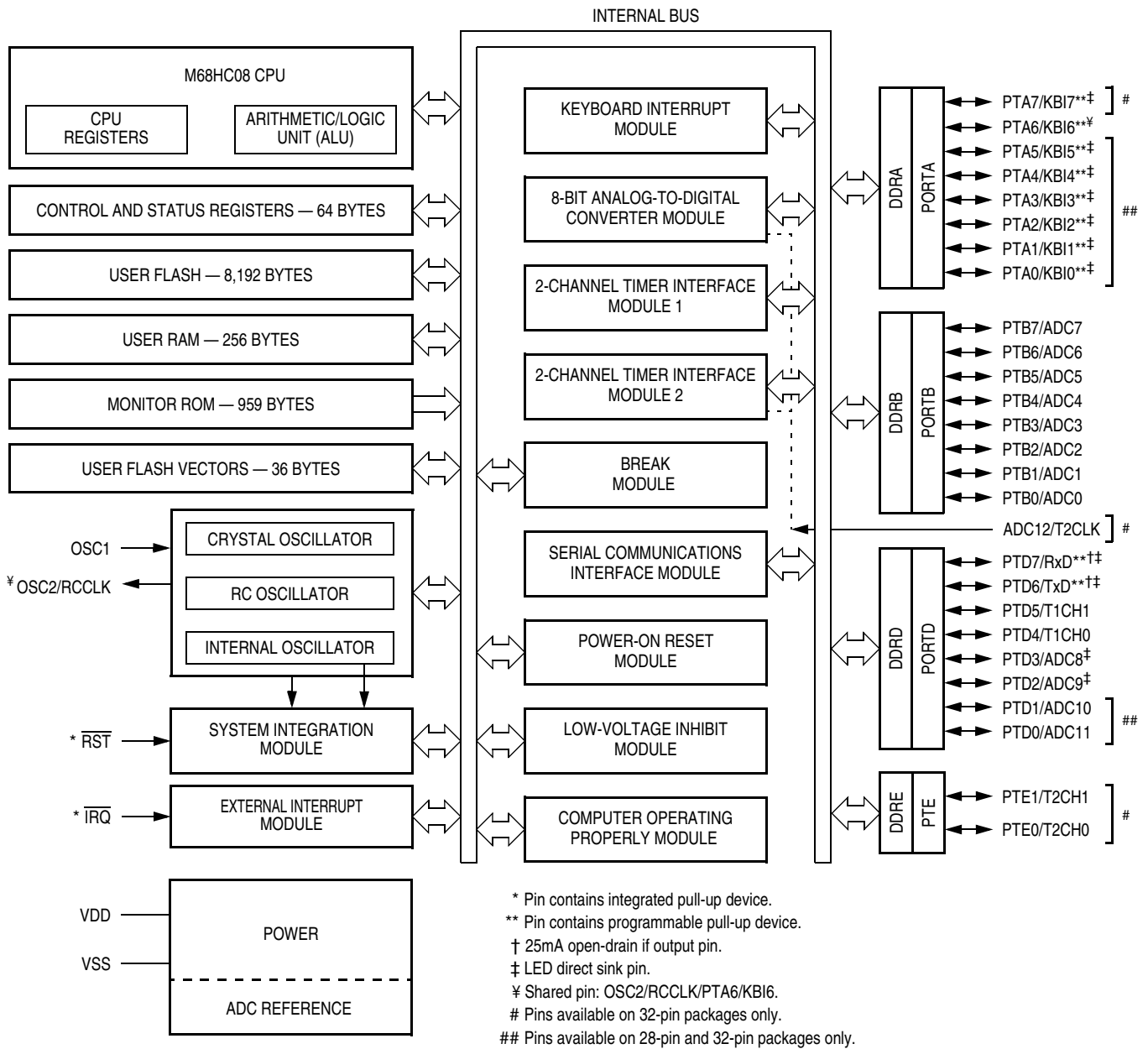


Figure 1-1. MC68HC908JL8 Block Diagram

\$0000 ↓ \$003F	I/O REGISTERS 64 BYTES
\$0040 ↓ \$005F	RESERVED 32 BYTES
\$0060 ↓ \$015F	RAM 256 BYTES
\$0160 ↓ \$DBFF	UNIMPLEMENTED 55,968 BYTES
\$DC00 ↓ \$FBFF	FLASH MEMORY 8,192 BYTES
\$FC00 ↓ \$FDFF	MONITOR ROM 512 BYTES
\$FE00	BREAK STATUS REGISTER (BSR)
\$FE01	RESET STATUS REGISTER (RSR)
\$FE02	RESERVED
\$FE03	BREAK FLAG CONTROL REGISTER (BFCR)
\$FE04	INTERRUPT STATUS REGISTER 1 (INT1)
\$FE05	INTERRUPT STATUS REGISTER 2 (INT2)
\$FE06	INTERRUPT STATUS REGISTER 3 (INT3)
\$FE07	RESERVED
\$FE08	FLASH CONTROL REGISTER (FLCR)
\$FE09 ↓ \$FF0B	RESERVED
\$FE0C	BREAK ADDRESS HIGH REGISTER (BRKH)
\$FE0D	BREAK ADDRESS LOW REGISTER (BRKL)
\$FE0E	BREAK STATUS AND CONTROL REGISTER (BRKSCR)
\$FE0F	RESERVED
\$FE10 ↓ \$FFCE	MONITOR ROM 447 BYTES
\$FFCF	FLASH BLOCK PROTECT REGISTER (FLBPR)
\$FFD0	MASK OPTION REGISTER (MOR)
\$FFD1 ↓ \$FFDB	RESERVED 11 BYTES
\$FFDC ↓ \$FFFF	USER FLASH VECTORS 36 BYTES

Figure 2-1. Memory Map

Memory

8. Wait for time, t_{prog} (30 μ s).
9. Repeat steps 7 and 8 until all bytes within the row are programmed.
10. Clear the PGM bit.
11. Wait for time, t_{nvh} (5 μ s).
12. Clear the HVEN bit.
13. After time, t_{rcv} (1 μ s), the memory can be accessed in read mode again.

This program sequence is repeated throughout the memory until all data is programmed.

NOTE

The time between each FLASH address change (step 7 to step 7), or the time between the last FLASH addressed programmed to clearing the PGM bit (step 7 to step 10), must not exceed the maximum programming time, $t_{prog max}$.

NOTE

Programming and erasing of FLASH locations cannot be performed by code being executed from the FLASH memory. While these operations must be performed in the order shown, other unrelated operations may occur between the steps.

At the beginning of an interrupt, the CPU saves the CPU register contents on the stack and sets the interrupt mask (I bit) to prevent additional interrupts. At the end of an interrupt, the RTI instruction recovers the CPU register contents from the stack so that normal processing can resume. [Figure 5-9](#) shows interrupt entry timing.

[Figure 5-10](#) shows interrupt recovery timing.

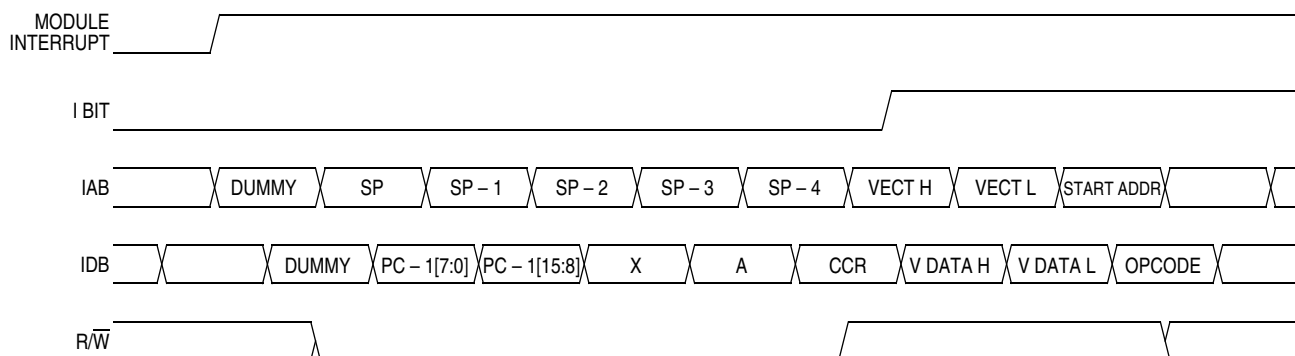


Figure 5-9. Interrupt Entry

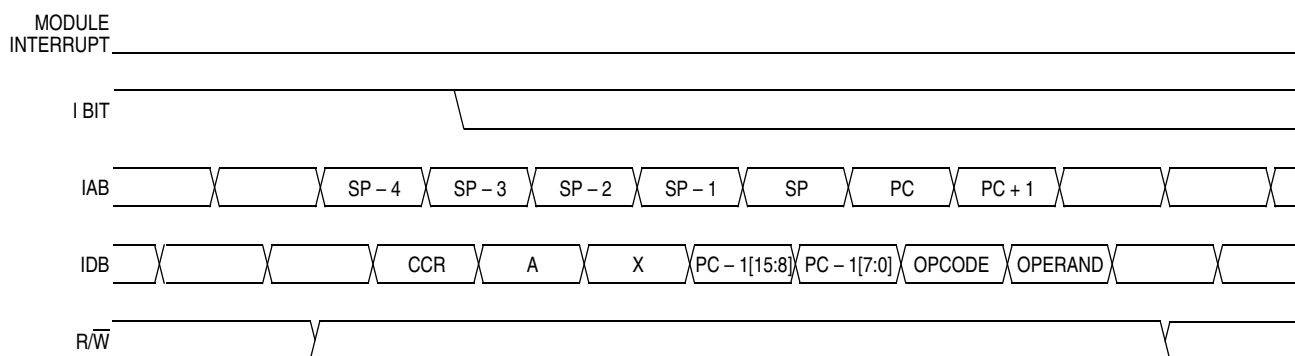


Figure 5-10. Interrupt Recovery

5.5.1.1 Hardware Interrupts

A hardware interrupt does not stop the current instruction. Processing of a hardware interrupt begins after completion of the current instruction. When the current instruction is complete, the SIM checks all pending hardware interrupts. If interrupts are not masked (I bit clear in the condition code register), and if the corresponding interrupt enable bit is set, the SIM proceeds with interrupt processing; otherwise, the next instruction is fetched and executed.

If more than one interrupt is pending at the end of an instruction execution, the highest priority interrupt is serviced first. [Figure 5-11](#) demonstrates what happens when two interrupts are pending. If an interrupt is pending upon exit from the original interrupt service routine, the pending interrupt is serviced before the LDA instruction is executed.

NOTE

The internal oscillator is a free running oscillator and is available after each POR or reset. It is turned-off in stop mode by setting the STOP_ICLKDIS bit in CONFIG2 (see 3.4 Configuration Register 2 (CONFIG2)).

6.4 I/O Signals

The following paragraphs describe the oscillator I/O signals.

6.4.1 Crystal Amplifier Input Pin (OSC1)

OSC1 pin is an input to the crystal oscillator amplifier or the input to the RC oscillator circuit.

6.4.2 Crystal Amplifier Output Pin (OSC2/RCCLK/PTA6/KBI6)

For the XTAL oscillator, OSC2 pin is the output of the crystal oscillator inverting amplifier.

For the RC oscillator, OSC2 pin can be configured as a general purpose I/O pin PTA6, or the output of the RC oscillator, RCCLK.

Oscillator	OSC2 pin function
XTAL	Inverting OSC1
RC	Controlled by PTA6EN bit in PTAPUE (\$000D) PTA6EN = 0: RCCLK output PTA6EN = 1: PTA6/KBI6

6.4.3 Oscillator Enable Signal (SIMOSCEN)

The SIMOSCEN signal comes from the system integration module (SIM) and enables/disables the XTAL oscillator circuit or the RC-oscillator.

6.4.4 XTAL Oscillator Clock (XTALCLK)

XTALCLK is the XTAL oscillator output signal. It runs at the full speed of the crystal (f_{XCLK}) and comes directly from the crystal oscillator circuit. Figure 6-2 shows only the logical relation of XTALCLK to OSC1 and OSC2 and may not represent the actual circuitry. The duty cycle of XTALCLK is unknown and may depend on the crystal and other external factors. Also, the frequency and amplitude of XTALCLK can be unstable at start-up.

6.4.5 RC Oscillator Clock (RCCLK)

RCCLK is the RC oscillator output signal. Its frequency is directly proportional to the time constant of the external R and C. Figure 6-3 shows only the logical relation of RCCLK to OSC1 and may not represent the actual circuitry.

6.4.6 Oscillator Out 2 (2OSCOU2)

2OSCOU2 is same as the input clock (XTALCLK or RCCLK). This signal is driven to the SIM module.

7.3.1 Entering Monitor Mode

Table 7-1 shows the pin conditions for entering monitor mode. As specified in the table, monitor mode may be entered after a POR.

Communication at 9600 baud will be established provided one of the following sets of conditions is met:

1. If $\overline{\text{IRQ}} = V_{\text{TST}}$:
 - Clock on OSC1 is 4.9125MHz
 - PTB3 = low
2. If $\overline{\text{IRQ}} = V_{\text{TST}}$:
 - Clock on OSC1 is 9.8304MHz
 - PTB3 = high
3. If \$FFFE and \$FFFF are blank (contain \$FF):
 - Clock on OSC1 is 9.8304MHz
 - $\overline{\text{IRQ}} = V_{\text{DD}}$

Table 7-1. Monitor Mode Entry Requirements and Options

$\overline{\text{IRQ}}$	\$FFFE and \$FFFF	PTB3	PTB2	PTB1	PTB0	OSC1 Clock ⁽¹⁾	Bus Frequency	Comments
$V_{\text{TST}}^{(2)}$	X	0	0	1	1	4.9152MHz	2.4576MHz	High voltage entry to monitor mode. 9600 baud communication on PTB0. COP disabled.
$V_{\text{TST}}^{(1)}$	X	1	0	1	1	9.8304MHz	2.4576MHz	
V_{DD}	BLANK (contain \$FF)	X	X	X	1	9.8304MHz	2.4576MHz	Blank reset vector (low-voltage) entry to monitor mode. 9600 baud communication on PTB0. COP disabled.
V_{DD}	NOT BLANK	X	X	X	X	X	OSC1 ÷ 4	Enters User mode.

1. RC oscillator cannot be used for monitor mode; must use either external oscillator or XTAL oscillator circuit.
2. See Table 17-4 for V_{TST} voltage level requirements.

If V_{TST} is applied to $\overline{\text{IRQ}}$ and PTB3 is low upon monitor mode entry (Table 7-1 condition set 1), the bus frequency is a divide-by-two of the clock input to OSC1. If PTB3 is high with V_{TST} applied to $\overline{\text{IRQ}}$ upon monitor mode entry (Table 7-1 condition set 2), the bus frequency is a divide-by-four of the clock input to OSC1. Holding the PTB3 pin low when entering monitor mode causes a bypass of a divide-by-two stage at the oscillator *only if V_{TST} is applied to $\overline{\text{IRQ}}$* . In this event, the OSCOUT frequency is equal to the 2OSCOUT frequency, and OSC1 input directly generates internal bus clocks. In this case, the OSC1 signal must have a 50% duty cycle at maximum bus frequency.

Entering monitor mode with V_{TST} on $\overline{\text{IRQ}}$, the COP is disabled as long as V_{TST} is applied to either $\overline{\text{IRQ}}$ or $\overline{\text{RST}}$. (See Chapter 5 System Integration Module (SIM) for more information on modes of operation.)

If entering monitor mode without high voltage on $\overline{\text{IRQ}}$ and reset vector being blank (\$FFFE and \$FFFF) (Table 7-1 condition set 3, where applied voltage is V_{DD}), then all port B pin requirements and conditions,

Monitor ROM (MON)

The data transmit and receive rate can be anywhere from 4800 baud to 28.8k-baud. Transmit and receive baud rates must be identical.

7.3.4 Echoing

As shown in [Figure 7-5](#), the monitor ROM immediately echoes each received byte back to the PTB0 pin for error checking.

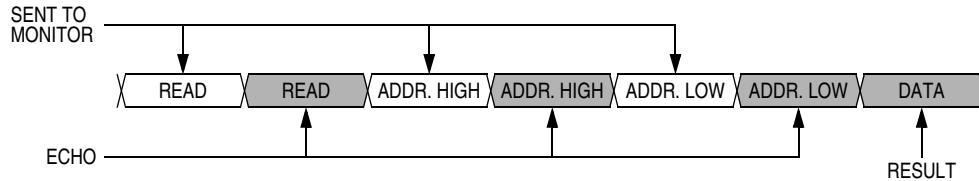


Figure 7-5. Read Transaction

Any result of a command appears after the echo of the last byte of the command.

7.3.5 Break Signal

A start bit followed by nine low bits is a break signal. (See [Figure 7-6](#).) When the monitor receives a break signal, it drives the PTB0 pin high for the duration of two bits before echoing the break signal.

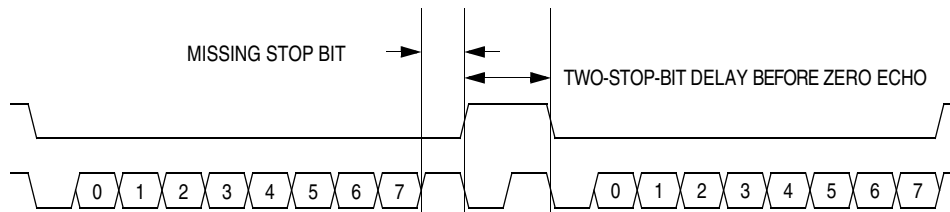


Figure 7-6. Break Transaction

7.3.6 Commands

The monitor ROM uses the following commands:

- READ (read memory)
- WRITE (write memory)
- IREAD (indexed read)
- IWRITE (indexed write)
- READSP (read stack pointer)
- RUN (run user program)

Monitor ROM (MON)

The control and data bytes are described below.

- **Bus speed** — This one byte indicates the operating bus speed of the MCU. The value of this byte should be equal to 4 times the bus speed, and should not be set to less than 4 (i.e. minimum bus speed is 1 MHz).
- **Data size** — This one byte indicates the number of bytes in the data array that are to be manipulated. The maximum data array size is 128. Routines EE_WRITE and EE_READ are restricted to manipulate a data array between 2 to 15 bytes. Whereas routines ERARNGE and MON_ERARNGE do not manipulate a data array, thus, this data size byte has no meaning.
- **Start address** — These two bytes, high byte followed by low byte, indicate the start address of the FLASH memory to be manipulated.
- **Data array** — This data array contains data that are to be manipulated. Data in this array are programmed to FLASH memory by the programming routines: PRGRNGE, MON_PRGRNGE, EE_WRITE. For the read routines: LDRNGE, MON_LDRNGE, and EE_READ, data is read from FLASH and stored in this array.

7.5.1 PRGRNGE

PRGRNGE is used to program a range of FLASH locations with data loaded into the data array.

Table 7-11. PRGRNGE Routine

Routine Name	PRGRNGE
Routine Description	Program a range of locations
Calling Address	\$FC06
Stack Used	15 bytes
Data Block Format	Bus speed (BUS_SPD) Data size (DATASIZE) Start address high (ADDRH) Start address (ADDRL) Data 1 (DATA1) : Data N (DATAN)

The start location of the FLASH to be programmed is specified by the address ADDRH:ADDRL and the number of bytes from this location is specified by DATASIZE. The maximum number of bytes that can be programmed in one routine call is 128 bytes (max. DATASIZE is 128).

ADDRH:ADDRL do not need to be at a page boundary, the routine handles any boundary misalignment during programming. A check to see that all bytes in the specified range are erased is not performed by this routine prior programming. Nor does this routine do a verification after programming, so there is no return confirmation that programming was successful. User must assure that the range specified is first erased.

The coding example below is to program 32 bytes of data starting at FLASH location \$EF00, with a bus speed of 4.9152 MHz. The coding assumes the data block is already loaded in RAM, with the address pointer, FILE_PTR, pointing to the first byte of the data block.

8.9 I/O Registers

NOTE

References to either timer 1 or timer 2 may be made in the following text by omitting the timer number. For example, TSC may generically refer to both T1SC AND T2SC.

These I/O registers control and monitor operation of the TIM:

- TIM status and control register (TSC)
- TIM counter registers (TCNTH:TCNTL)
- TIM counter modulo registers (TMODH:TMODL)
- TIM channel status and control registers (TSC0, TSC1)
- TIM channel registers (TCH0H:TCH0L, TCH1H:TCH1L)

8.9.1 TIM Status and Control Register

The TIM status and control register (TSC):

- Enables TIM overflow interrupts
- Flags TIM overflows
- Stops the TIM counter
- Resets the TIM counter
- Prescales the TIM counter clock

Address: T1SC, \$0020 and T2SC, \$0030

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
Write:	0			TRST				
Reset:	0	0	1	0	0	0	0	0


 = Unimplemented

Figure 8-4. TIM Status and Control Register (TSC)

TOF — TIM Overflow Flag Bit

This read/write flag is set when the TIM counter reaches the modulo value programmed in the TIM counter modulo registers. Clear TOF by reading the TIM status and control register when TOF is set and then writing a logic 0 to TOF. If another TIM overflow occurs before the clearing sequence is complete, then writing logic 0 to TOF has no effect. Therefore, a TOF interrupt request cannot be lost due to inadvertent clearing of TOF. Reset clears the TOF bit. Writing a logic 1 to TOF has no effect.

- 1 = TIM counter has reached modulo value
- 0 = TIM counter has not reached modulo value

TOIE — TIM Overflow Interrupt Enable Bit

This read/write bit enables TIM overflow interrupts when the TOF bit becomes set. Reset clears the TOIE bit.

- 1 = TIM overflow interrupts enabled
- 0 = TIM overflow interrupts disabled

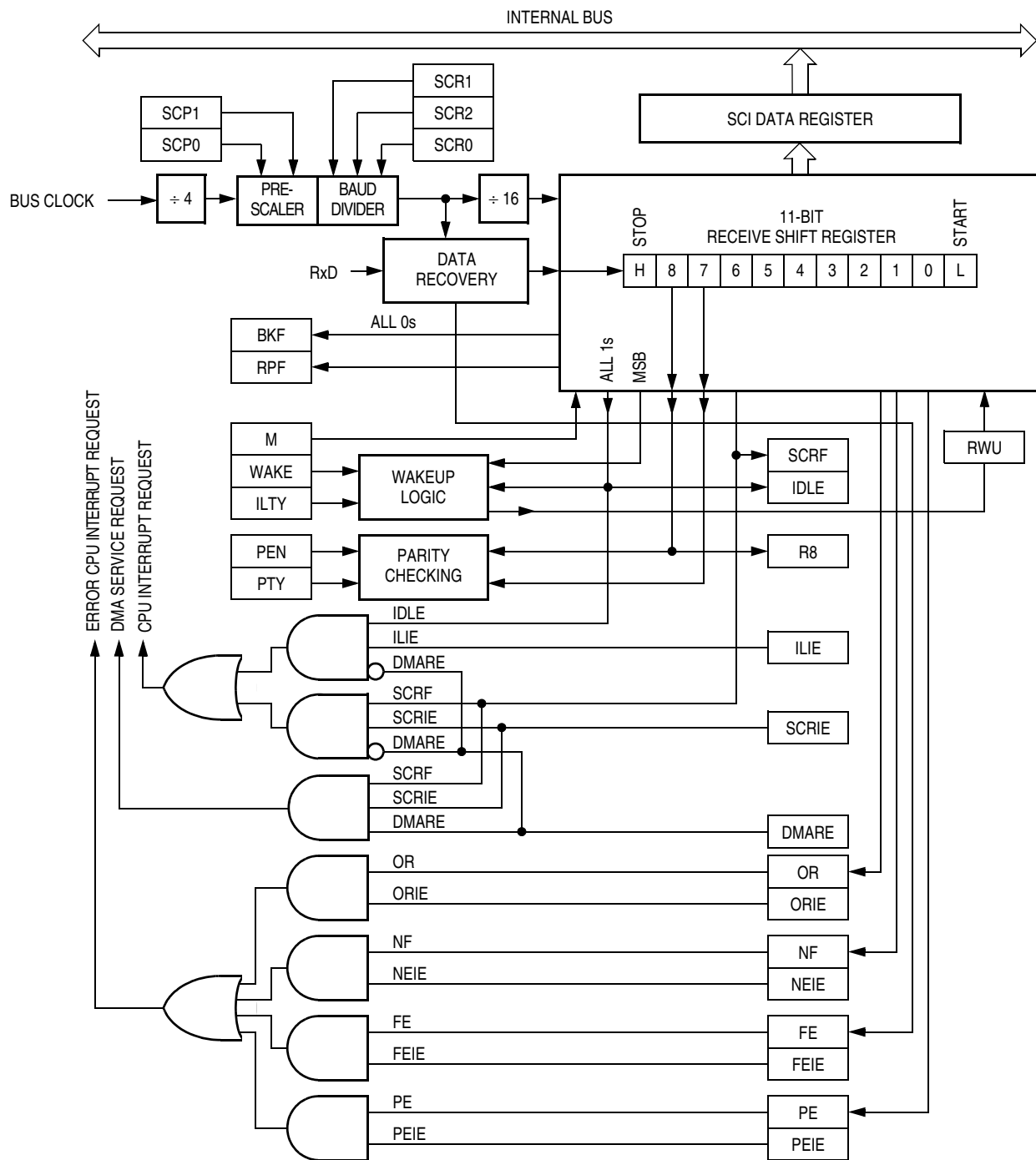


Figure 9-5. SCI Receiver Block Diagram

11.2.3 Port A Input Pull-Up Enable Registers

The port A input pull-up enable registers contain a software configurable pull-up device for each of the eight port A pins. Each bit is individually configurable and requires the corresponding data direction register, DDRAx be configured as input. Each pull-up device is automatically disabled when its corresponding DDRAx bit is configured as output.

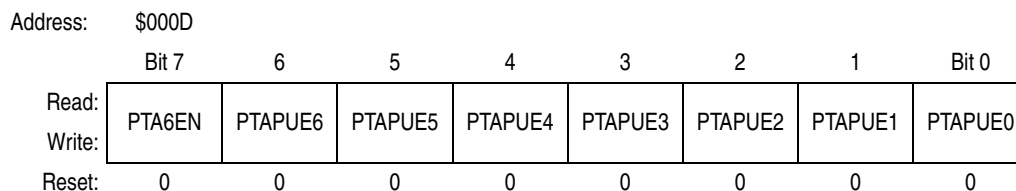


Figure 11-5. Port A Input Pull-up Enable Register (PTAPUE)

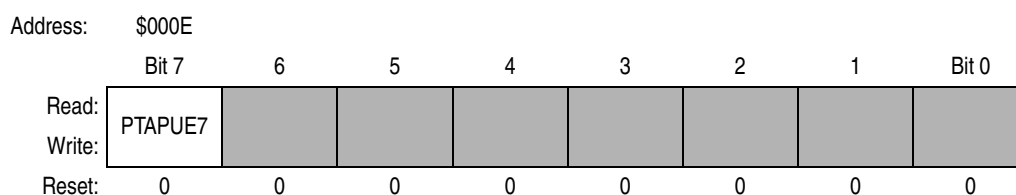


Figure 11-6. PTA7 Input Pull-up Enable Register (PTA7PUE)

PTA6EN — Enable PTA6 on OSC2

This read/write bit configures the OSC2 pin function when RC oscillator option is selected. This bit has no effect for XTAL oscillator option.

- 1 = OSC2 pin configured for PTA6 I/O, and has all the interrupt and pull-up functions
- 0 = OSC2 pin outputs the RC oscillator clock (RCCLK)

PTAPUE[7:0] — Port A Input Pull-up Enable Bits

These read/write bits are software programmable to enable pull-up devices on port A pins.

- 1 = Corresponding port A pin configured to have internal pull-up if its DDRA bit is set to 0
- 0 = Pull-up device is disconnected on the corresponding port A pin regardless of the state of its DDRA bit

Chapter 12

External Interrupt (IRQ)

12.1 Introduction

The external interrupt (IRQ) module provides a maskable interrupt input.

12.2 Features

Features of the IRQ module include the following:

- A dedicated external interrupt pin ($\overline{\text{IRQ}}$)
- IRQ interrupt control bits
- Hysteresis buffer
- Programmable edge-only or edge and level interrupt sensitivity
- Automatic interrupt acknowledge
- Selectable internal pullup resistor

12.3 Functional Description

A logic zero applied to the external interrupt pin can latch a CPU interrupt request. [Figure 12-1](#) shows the structure of the IRQ module.

Interrupt signals on the $\overline{\text{IRQ}}$ pin are latched into the IRQ latch. An interrupt latch remains set until one of the following actions occurs:

- Vector fetch — A vector fetch automatically generates an interrupt acknowledge signal that clears the IRQ latch.
- Software clear — Software can clear the interrupt latch by writing to the acknowledge bit in the interrupt status and control register (INTSCR). Writing a logic one to the ACK bit clears the IRQ latch.
- Reset — A reset automatically clears the interrupt latch.

The external interrupt pin is falling-edge-triggered and is software-configurable to be either falling-edge or falling-edge and low-level-triggered. The MODE bit in the INTSCR controls the triggering sensitivity of the IRQ pin.

When the interrupt pin is edge-triggered only, the CPU interrupt request remains set until a vector fetch, software clear, or reset occurs.

When the interrupt pin is both falling-edge and low-level-triggered, the CPU interrupt request remains set until both of the following occur:

- Vector fetch or software clear
- Return of the interrupt pin to logic one

15.4 LVI Control Register (CONFIG2/CONFIG1)

The LVI module is controlled by three bits in the configuration registers, CONFIG1 and CONFIG2.

Address: \$001E

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	IRQPUD	R	R	LVIT1	LVIT0	R	R	STOP_ICLKDIS
Write:								
Reset:	0	0	0	Cleared by POR only		0	0	0

Figure 15-2. Configuration Register 2 (CONFIG2)

Address: \$001F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	COPRS	R	R	LVID	R	SSREC	STOP	COPD
Write:								
Reset:	0	0	0	0	0	0	0	0

Figure 15-3. Configuration Register 1 (CONFIG1)

LVID — Low Voltage Inhibit Disable Bit

LVID disables the LVI module. Reset clears LVID.

1 = Low voltage inhibit disabled

0 = Low voltage inhibit enabled

LVIT1, LVIT0 — LVI Trip Voltage Selection Bits

These two bits determine at which level of V_{DD} the LVI module will come into action. LVIT1 and LVIT0 are cleared by a power-on reset only.

Table 15-1. Trip Voltage Selection

LVIT1	LVIT0	Trip Voltage ⁽¹⁾	Comments
0	0	V_{LVR3} (2.49V)	For $V_{DD}=3V$ operation
0	1	V_{LVR3} (2.49V)	For $V_{DD}=3V$ operation
1	0	V_{LVR5} (4.25V)	For $V_{DD}=5V$ operation
1	1	Reserved	

1. See [Chapter 17 Electrical Specifications](#) for full parameters.

15.5 Low-Power Modes

The STOP and WAIT instructions put the MCU in low-power-consumption standby modes.

15.5.1 Wait Mode

The LVI module, when enabled, will continue to operate in wait mode.

15.5.2 Stop Mode

The LVI module, when enabled, will continue to operate in stop mode.

16.4 Break Module Registers

These registers control and monitor operation of the break module:

- Break status and control register (BRKSCR)
- Break address register high (BRKH)
- Break address register low (BRKL)
- Break status register (BSR)
- Break flag control register (BFCR)

16.4.1 Break Status and Control Register (BRKSCR)

The break status and control register contains break module enable and status bits.

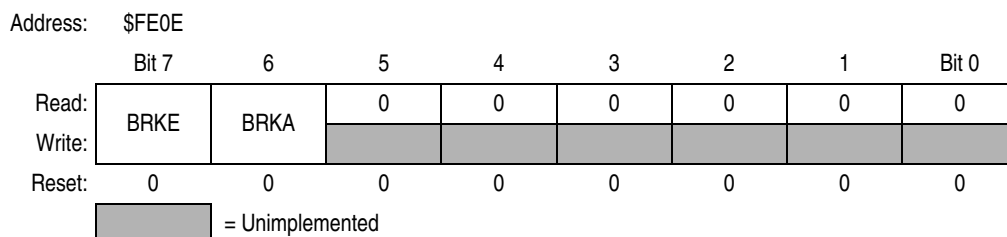


Figure 16-3. Break Status and Control Register (BRKSCR)

BRKE — Break Enable Bit

This read/write bit enables breaks on break address register matches. Clear BRKE by writing a logic zero to bit 7. Reset clears the BRKE bit.

- 1 = Breaks enabled on 16-bit address match
- 0 = Breaks disabled

BRKA — Break Active Bit

This read/write status and control bit is set when a break address match occurs. Writing a logic one to BRKA generates a break interrupt. Clear BRKA by writing a logic zero to it before exiting the break routine. Reset clears the BRKA bit.

- 1 = Break address match
- 0 = No break address match

16.4.2 Break Address Registers

The break address registers contain the high and low bytes of the desired breakpoint address. Reset clears the break address registers.

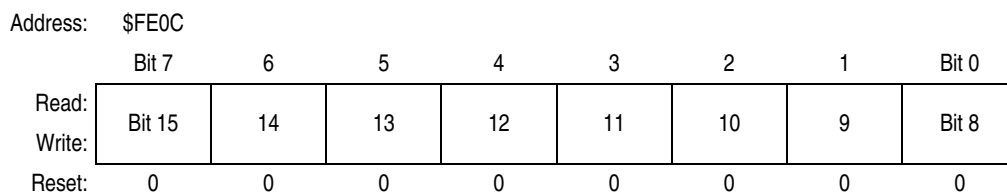


Figure 16-4. Break Address Register High (BRKH)

17.6 5V Control Timing

Table 17-5. Control Timing (5V)

Characteristic ⁽¹⁾	Symbol	Min	Max	Unit
Internal operating frequency	f_{OP}	—	8	MHz
\overline{RST} input pulse width low ⁽²⁾	t_{RL}	750	—	ns
TIM2 external clock input	f_{T2CLK}	—	4	MHz
\overline{IRQ} interrupt pulse width low (edge-triggered) ⁽³⁾	t_{LIH}	100	—	ns
\overline{IRQ} interrupt pulse period ⁽³⁾	t_{LIL}	Note ⁽⁴⁾	—	t_{CYC}

- $V_{DD} = 4.5$ to 5.5 Vdc, $V_{SS} = 0$ Vdc, $T_A = T_L$ to T_H ; timing shown with respect to 20% V_{DD} and 70% V_{SS} , unless otherwise noted.
- Minimum pulse width reset is guaranteed to be recognized. It is possible for a smaller pulse width to cause a reset.
- Values are based on characterization results, not tested in production.
- The minimum period is the number of cycles it takes to execute the interrupt service routine plus 1 t_{CYC} .

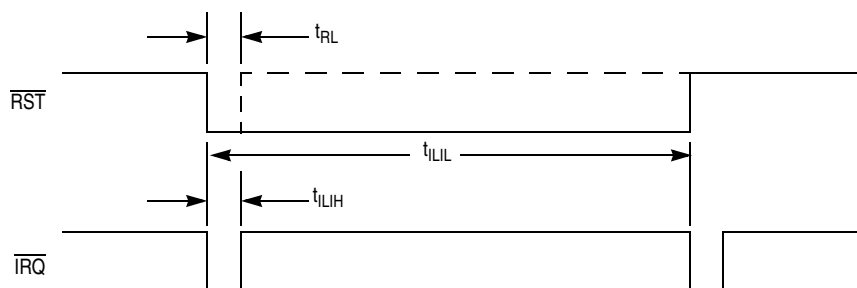


Figure 17-1. \overline{RST} and \overline{IRQ} Timing

17.7 5V Oscillator Characteristics

Table 17-6. Oscillator Specifications (5V)

Characteristic	Symbol	Min	Typ	Max	Unit
Internal oscillator clock frequency	f_{ICLK}		50k ⁽¹⁾		Hz
External reference clock to OSC1 ⁽²⁾	f_{OSC}	dc	—	32M	Hz
Crystal reference frequency ⁽³⁾	$f_{XTALCLK}$		—	32M	Hz
Crystal load capacitance ⁽⁴⁾	C_L	—	—	—	
Crystal fixed capacitance ⁽³⁾	C_1	—	$2 \times C_L$	—	
Crystal tuning capacitance ⁽³⁾	C_2	—	$2 \times C_L$	—	
Feedback bias resistor	R_B	—	10 M Ω	—	
Series resistor ^{(3), (5)}	R_S	—	—	—	
External RC clock frequency	f_{RCCLK}	2M	—	12M	Hz
RC oscillator external R	R_{EXT}	See Figure 17-2			Ω
RC oscillator external C	C_{EXT}	—	10	—	pF

- Typical value reflect average measurements at midpoint of voltage range, 25 °C only. See Figure 17-5 for plot.
- No more than 10% duty cycle deviation from 50%.
- Fundamental mode crystals only.
- Consult crystal vendor data sheet.
- Not required for high frequency crystals.

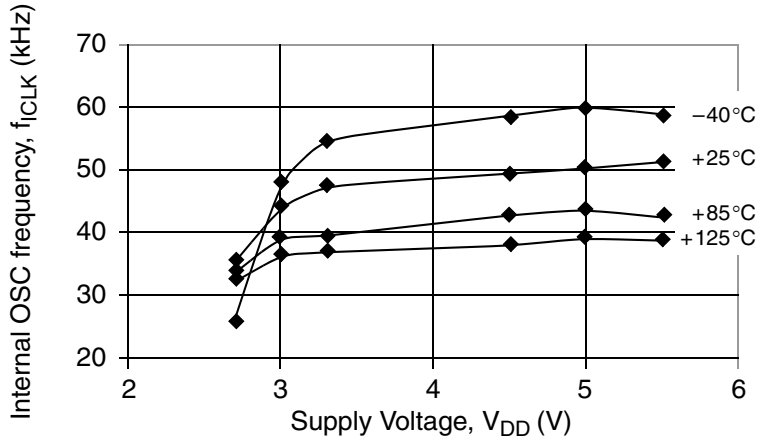


Figure 17-5. Internal Oscillator Frequency

17.11 Typical Supply Currents

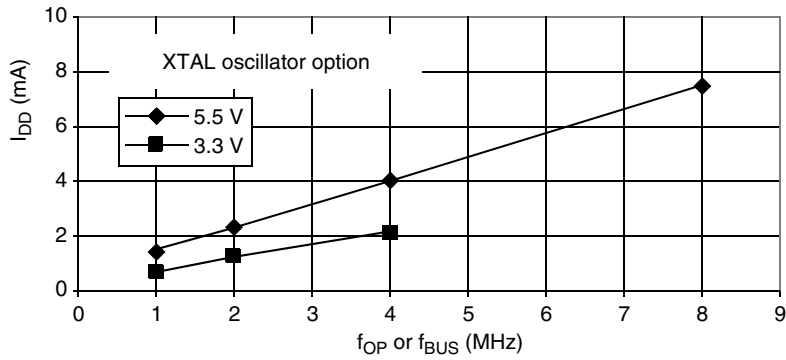


Figure 17-6. Typical Operating I_{DD} (XTAL osc), with All Modules Turned On (25 °C)

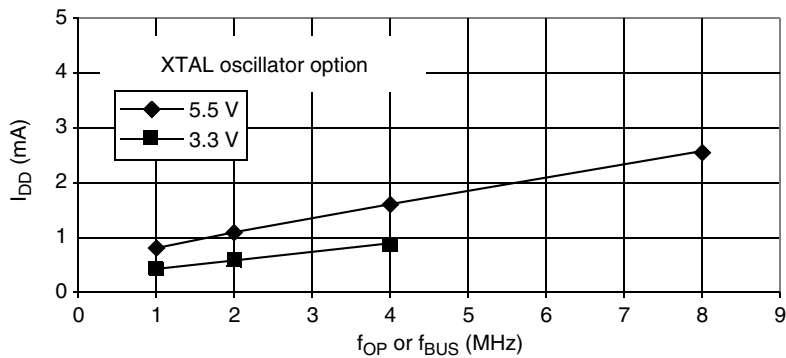


Figure 17-7. Typical Wait Mode I_{DD} (XTAL osc), with All Modules Turned Off (25 °C)

Chapter 18

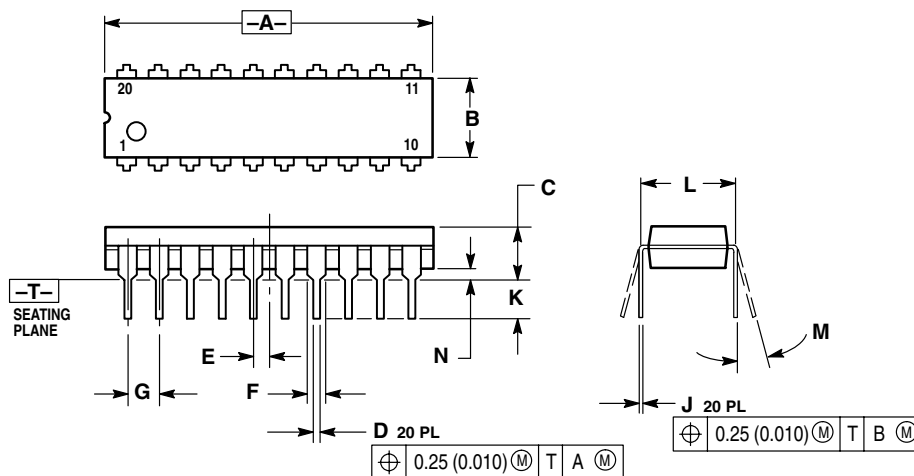
Mechanical Specifications

18.1 Introduction

This section gives the dimensions for:

- 20-pin plastic dual in-line package (case #738)
- 20-pin small outline integrated circuit package (case #751D)
- 28-pin plastic dual in-line package (case #710)
- 28-pin small outline integrated circuit package (case #751F)
- 32-pin shrink dual in-line package (case #1376)
- 32-pin low-profile quad flat pack (case #873A)

18.2 20-Pin Plastic Dual In-Line Package (PDIP)



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

Figure 18-1. 20-Pin PDIP (Case #738)

