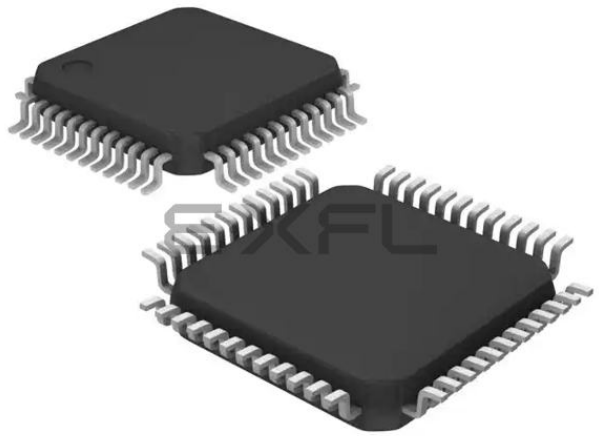

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 72MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | DMA, I²S, POR, PWM, WDT |
| Number of I/O | 19 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 3.6V |
| Data Converters | A/D 11x12b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f318c8t6 |

## 3.8 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allows I/O toggling up to 36 MHz.

## 3.9 Direct memory access (DMA)

The flexible general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each of the 7 DMA channels is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, $I^2C$, USART, timers, DAC and ADC.

## 3.10 Interrupts and events

### 3.10.1 Nested vectored interrupt controller (NVIC)

The STM32F318x8 devices embed a nested vectored interrupt controller (NVIC) able to handle up to 60 maskable interrupt channels and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

## 3.21 Infrared transmitter

The STM32F318x8 devices provide an infrared transmitter solution. The solution is based on internal connections between TIM16 and TIM17 as shown in the figure below.

TIM17 is used to provide the carrier frequency and TIM16 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate the infrared remote control signals, TIM16 channel 1 and TIM17 channel 1 must be properly configured to generate correct waveforms. All standard IR pulse modulation modes can be obtained by programming the two timers output compare channels.

**Figure 3. Infrared transmitter**

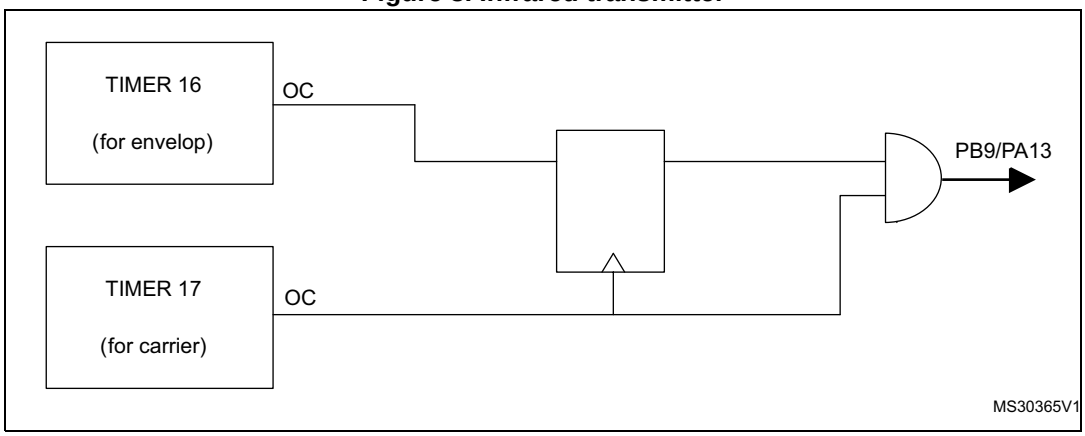


Table 14. Alternate functions for Port B (continued)

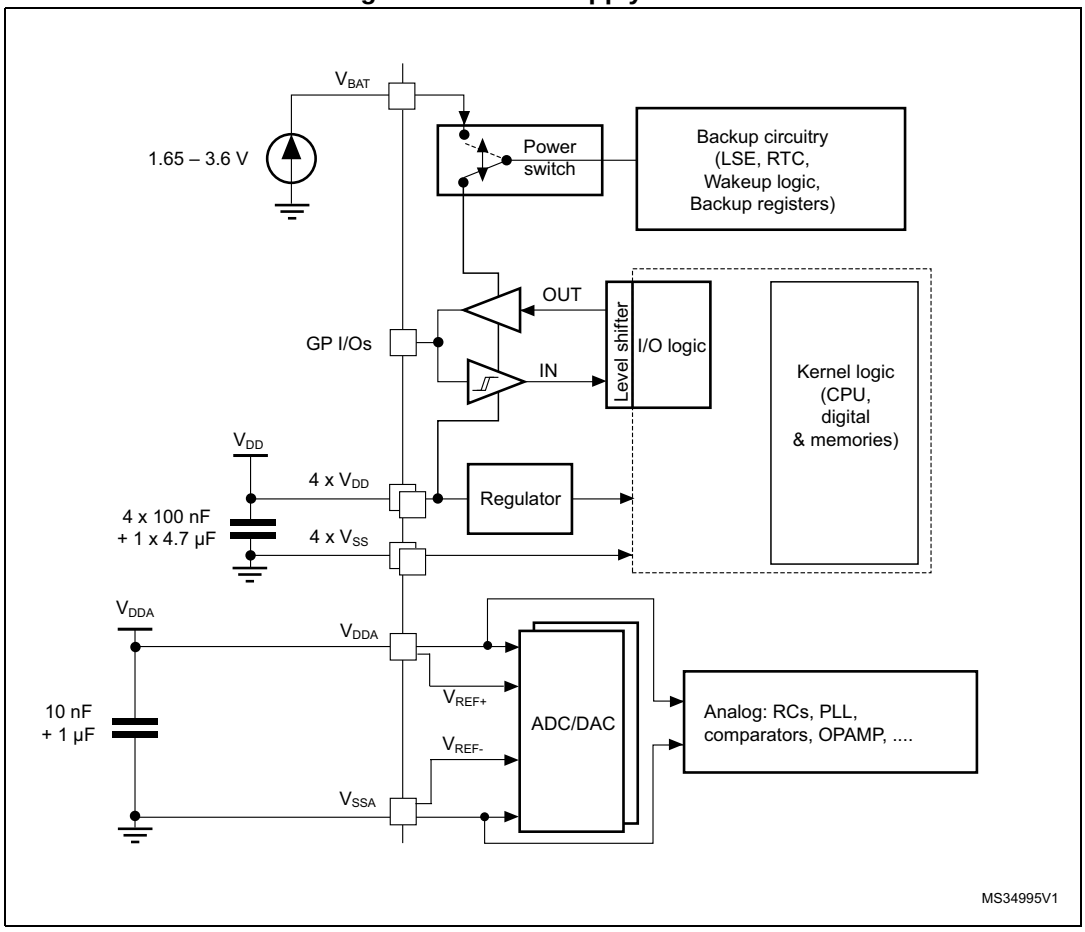
| Port & pin name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | SYS_AF | TIM2/TIM15/TIM16 /TIM17/EVENT | I2C3/TIM1/TIM2/TIM15 | I2C3/TIM15/TSC | I2C1/I2C2/TIM1/ TIM16/TIM17 | SPI2/I2S2/ SPI3/I2S3/Infrared | SPI2/I2S2/SPI3/ I2S3/TIM1/Infrared | USART1/USART2/USART3/ GPCOMP6 | I2C3/GPCOMP2 /GPCOMP4/GPCOMP6 | TIM1/TIM15 | TIM2/TIM17 | TIM1 | TIM1 | - | - | EVENT |
| PB10 | - | TIM2 _CH3 | - | TSC _SYNC | - | - | - | USART3 _TX | - | - | - | - | - | - | - | EVENT OUT |
| PB11 | - | TIM2 _CH4 | - | TSC _G6_IO1 | - | - | - | USART3 _RX | - | - | - | - | - | - | - | EVENT OUT |
| PB12 | - | - | - | TSC _G6_IO2 | I2C2 _SMBAL | SPI2_NSS/I2S2_ WS | TIM1 _BKIN | USART3 _CK | - | - | - | - | - | - | - | EVENT OUT |
| PB13 | - | - | - | TSC _G6_IO3 | - | SPI2_SCK/ I2S2_CK | TIM1 _CH1N | USART3 _CTS | - | - | - | - | - | - | - | EVENT OUT |
| PB14 | - | TIM15 _CH1 | - | TSC _G6_IO4 | - | SPI2_MISO/I2S2 ext_SD | TIM1 _CH2N | USART3 _RTS _DE | - | - | - | - | - | - | - | EVENT OUT |
| PB15 | RTC _REFIN | TIM15 _CH2 | TIM15 _CH1N | - | TIM1 _CH3N | SPI2_MOSI/ I2S2_SD | - | - | - | - | - | - | - | - | - | EVENT OUT |

Table 15. Alternate functions for Port F

| Port & pin name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|---|
| | SYS_AF | TIM2/TIM15/ TIM16/TIM17/ EVENT | I2C3/TIM1/TIM2/ TIM15 | I2C3/TIM15/TSC | I2C1/I2C2/TIM1/ TIM16/TIM17 | SPI2/I2S2/ SPI3/I2S3/ Infrared | SPI2/I2S2/SPI3/ I2S3/TIM1/ Infrared | USART1/USART2/USART3/ GPCOMP6 |
| PF0 | - | - | - | - | I2C2_SDA | SPI2_NSS/ I2S2_WS | TIM1_CH3N | - |
| PF1 | - | - | - | - | I2C2_SCL | SPI2_SCK/ I2S2_CK | - | - |

### 6.1.6 Power supply scheme

**Figure 10. Power supply scheme**




**Caution:** Each power supply pair (for example $V_{DD}/V_{SS}$, $V_{DDA}/V_{SSA}$) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

## 6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 17: Voltage characteristics*, *Table 18: Current characteristics*, and *Table 19: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 17. Voltage characteristics(1)**

| Symbol | Ratings | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$–$V_{SS}$ | External main supply voltage (including $V_{DD}$ and $V_{BAT}$) | -0.3 | 1.95 | V |
| $V_{DDA}$–$V_{SS}$ | External main supply voltage | -0.3 | 4.0 | V |
| $V_{DD}$–$V_{DDA}$ | Allowed voltage difference for $V_{DD} > V_{DDA}$ | - | 0.4 | V |
| $V_{IN}$(2) | Input voltage on FT and FTf pins | $V_{SS}$ – 0.3 | $V_{DD}$ + 4.0 | V |
| | Input voltage on TTa and TT pins | $V_{SS}$ – 0.3 | 4.0 | |
| | Input voltage on POR pin | $V_{SS}$ – 0.3 | $V_{DDA}$ + 4.0 | |
| | Input voltage on any other pin | $V_{SS}$ – 0.3 | 4.0 | |
| | Input voltage on Boot0 pin | 0 | 9 | |
| $\lvert\Delta V_{DDx}\rvert$ | Variations between different $V_{DD}$ power pins | - | 50 | mV |
| $\lvert V_{SSX} - V_{SS}\rvert$ | Variations between all the different ground pins | - | 50 | |
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | see *Section 6.3.11: Electrical sensitivity characteristics* | | V |

1. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range. The following relationship must be respected between $V_{DDA}$ and $V_{DD}$:
$V_{DDA}$ must power on before or at the same time as $V_{DD}$ in the power up sequence.
$V_{DDA}$ must be greater than or equal to $V_{DD}$.
2. $V_{IN}$ maximum must always be respected. Refer to *Table 18: Current characteristics* for the maximum allowed injected current values.

**Table 18. Current characteristics**

| Symbol | Ratings | Max. | Unit |
|---|---|---|---|
| $\Sigma I_{VDD}$ | Total current into sum of all VDD_x power lines (source) | 130 | mA |
| $\Sigma I_{VSS}$ | Total current out of sum of all VSS_x ground lines (sink) | -130 | |
| $I_{VDD}$ | Maximum current into each $V_{DD\_x}$ power line (source)(1) | 100 | |
| $I_{VSS}$ | Maximum current out of each $V_{SS\_x}$ ground line (sink)(1) | -100 | |
| $I_{IO(PIN)}$ | Output current sunk by any I/O and control pin | 25 | |
| | Output current sourced by any I/O and control pin | -25 | |
| $\Sigma I_{IO(PIN)}$ | Total output current sunk by sum of all IOs and control pins(2) | 80 | |
| | Total output current sourced by sum of all IOs and control pins(2) | -80 | |
| $I_{INJ(PIN)}$ | Injected current on TT, FT, FTf and B pins(3) | -5/+0 | |
| | Injected current on TC and RST pin(4) | +/-5 | |
| | Injected current on TTa pins(5) | +/-5 | |
| $\Sigma I_{INJ(PIN)}$ | Total injected current (sum of all I/O and control pins)(6) | +/-25 | |

1. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$ and $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins.The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 17: Voltage characteristics* for the maximum allowed input voltage values.
5. A positive injection is induced by $V_{IN} > V_{DDA}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ}$(PIN) must never be exceeded. Refer also to *Table 17: Voltage characteristics* for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note (2) below *Table 61*.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

**Table 19. Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $T_J$ | Maximum junction temperature | 150 | °C |

**Table 25. Typical and maximum current consumption from the $V_{DDA}$ supply**

| Symbol | Parameter | Conditions (1) | $f_{HCLK}$ | $V_{DDA}$ = 2.4 V | | | | $V_{DDA}$ = 3.6 V | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Typ | Max @ $T_A$(2) | | | Typ | Max @ $T_A$(2) | | | |
| | | | | | 25 °C | 85 °C | 105 °C | | 25 °C | 85 °C | 105 °C | |
| $I_{DDA}$ | Supply current in Run mode, code executing from Flash or RAM | HSE bypass | 72 MHz | 225 | 248(3) | 261 | 266(3) | 248 | 270(3) | 290 | 296(3) | µA |
| | | | 64 MHz | 198 | 221 | 234 | 239 | 219 | 241 | 258 | 263 | |
| | | | 48 MHz | 149 | 169 | 178 | 182 | 163 | 182 | 196 | 200 | |
| | | | 32 MHz | 102 | 120 | 128 | 131 | 112 | 131 | 139 | 142 | |
| | | | 24 MHz | 79 | 96 | 101 | 104 | 87 | 104 | 110 | 112 | |
| | | | 8 MHz | 3.1 | 4.1 | 4.1 | 5.1 | 3.1 | 4.1 | 4.1 | 5.1 | |
| | | | 1 MHz | 3.1 | 4.1 | 4.1 | 5.1 | 3.1 | 4.1 | 4.1 | 5.1 | |
| | | HSI clock | 64 MHz | 263 | 287 | 301 | 306 | 292 | 317 | 333 | 339 | |
| | | | 48 MHz | 214 | 236 | 248 | 252 | 237 | 260 | 272 | 277 | |
| | | | 32 MHz | 167 | 187 | 196 | 199 | 185 | 206 | 216 | 219 | |
| | | | 24 MHz | 144 | 164 | 171 | 173 | 161 | 179 | 188 | 191 | |
| | | | 8 MHz | 67 | 81 | 85 | 86 | 77 | 91 | 93 | 95 | |

1. Current consumption from the $V_{DDA}$ supply is independent of whether the peripherals are on or off. Furthermore when the PLL is off, $I_{DDA}$ is independent from the frequency.
2. Data based on characterization results, not tested in production.
3. Data based on characterization results and tested in production with code executing from RAM.

**Table 26. Typical and maximum $V_{DD}$ consumption in Stop mode**

| Symbol | Parameter | Conditions | Typ @$V_{DD}$ ($V_{DD}$= 1.8 V $V_{DDA}$ = 3.3 V) | Max | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | 1.8 V | $T_A$ = 25°C | $T_A$ = 85°C | $T_A$ = 105°C | |
| $I_{DD}$ | Supply current in Stop mode | All oscillators off | 3.11 | 7.3 | 160 | 359 | µA |

**Table 27. Typical and maximum $V_{DDA}$ consumption in Stop mode**

| Symbol | Parameter | Conditions | Typ @$V_{DD}$ ($V_{DD}$ = 1.8 V) | | | | | | | Max | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.8 V | 2.0 V | 2.4 V | 2.7 V | 3.0 V | 3.3 V | 3.6 V | $T_A$ = 25°C | $T_A$ = 85°C | $T_A$ = 105°C | |
| $I_{DDA}$ | Supply current in Stop mode | All oscillators off | 0.70 | 0.71 | 0.73 | 0.76 | 0.81 | 0.87 | 0.94 | 1.6 | 2.1 | 2.7 | µA |

**Table 30. Typical current consumption in Sleep mode, code running from Flash or RAM**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Typ | | Unit |
|---|---|---|---|---|---|---|
| | | | | Peripherals enabled | Peripherals disabled | |
| $I_{DD}$ | Supply current in Sleep mode from $V_{DD}$ supply | Running from HSE crystal clock 8 MHz, code executing from Flash or RAM | 72 MHz | 27.5 | 5.6 | mA |
| | | | 64 MHz | 24.5 | 5.0 | |
| | | | 48 MHz | 18.5 | 3.82 | |
| | | | 32 MHz | 12.5 | 2.62 | |
| | | | 24 MHz | 9.4 | 2.02 | |
| | | | 16 MHz | 6.3 | 1.42 | |
| | | | 8 MHz | 3.08 | 0.65 | |
| | | | 4 MHz | 1.93 | 0.55 | |
| | | | 2 MHz | 1.24 | 0.48 | |
| | | | 1 MHz | 0.90 | 0.44 | |
| | | | 500 kHz | 0.73 | 0.42 | |
| | | | 125 kHz | 0.59 | 0.41 | |
| $I_{DDA}$ (1) | Supply current in Sleep mode from $V_{DDA}$ supply | | 72 MHz | 237.3 | | µA |
| | | | 64 MHz | 208.7 | | |
| | | | 48 MHz | 154.6 | | |
| | | | 32 MHz | 105.1 | | |
| | | | 24 MHz | 81.3 | | |
| | | | 16 MHz | 57.7 | | |
| | | | 8 MHz | 0.87 | | |
| | | | 4 MHz | 0.87 | | |
| | | | 2 MHz | 0.87 | | |
| | | | 1 MHz | 0.87 | | |
| | | | 500 kHz | 0.87 | | |
| | | | 125 kHz | 0.87 | | |

1. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.

**Table 31. Switching output I/O current consumption**

| Symbol | Parameter | Conditions[1] | I/O toggling frequency ($f_{SW}$) | Typ | Unit |
|---|---|---|---|---|---|
| $I_{SW}$ | I/O current consumption | $V_{DD}$ = 1.8 V<br>$C_{ext}$ = 0 pF<br>$C = C_{INT} + C_{EXT} + C_S$ | 2 MHz | 0.10 | mA |
| | | | 4 MHz | 0.17 | |
| | | | 8 MHz | 0.40 | |
| | | | 18 MHz | 0.78 | |
| | | | 36 MHz | 1.51 | |
| | | | 48 MHz | 2.06 | |
| | | $V_{DD}$ = 1.8 V<br>$C_{ext}$ = 10 pF<br>$C = C_{INT} + C_{EXT} + C_S$ | 2 MHz | 0.14 | |
| | | | 4 MHz | 0.25 | |
| | | | 8 MHz | 0.57 | |
| | | | 18 MHz | 1.16 | |
| | | | 36 MHz | 2.45 | |
| | | | 48 MHz | 3.03 | |
| | | $V_{DD}$ = 1.8 V<br>$C_{ext}$ = 22 pF<br>$C = C_{INT} + C_{EXT} + C_S$ | 2 MHz | 0.19 | |
| | | | 4 MHz | 0.36 | |
| | | | 8 MHz | 0.75 | |
| | | | 18 MHz | 1.59 | |
| | | | 36 MHz | 3.25 | |
| | | $V_{DD}$ = 1.8 V<br>$C_{ext}$ = 33 pF<br>$C = C_{INT} + C_{EXT} + C_S$ | 2 MHz | 0.23 | |
| | | | 4 MHz | 0.45 | |
| | | | 8 MHz | 0.94 | |
| | | | 18 MHz | 1.97 | |
| | | | 36 MHz | 3.62 | |
| | | $V_{DD}$ = 1.8 V<br>$C_{ext}$ = 47 pF<br>$C = C_{INT} + C_{EXT} + C_S$ | 2 MHz | 0.28 | |
| | | | 4 MHz | 0.55 | |
| | | | 8 MHz | 1.15 | |
| | | | 18 MHz | 2.42 | |

1. CS = 5 pF (estimated value).

### Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 37*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

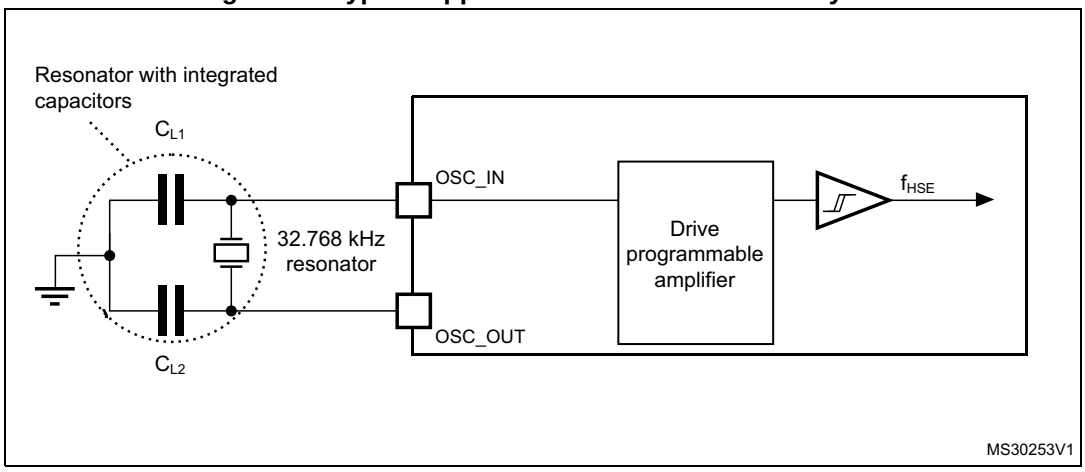
**Table 37. LSE oscillator characteristics ($f_{LSE}$ = 32.768 kHz)**

| Symbol | Parameter | Conditions(1) | Min(2) | Typ | Max(2) | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | LSE current consumption | LSEDRV[1:0]=00 lower driving capability | - | 0.5 | 0.9 | µA |
| | | LSEDRV[1:0]=01 medium low driving capability | - | - | 1 | |
| | | LSEDRV[1:0]=10 medium high driving capability | - | - | 1.3 | |
| | | LSEDRV[1:0]=11 higher driving capability | - | - | 1.6 | |
| $g_m$ | Oscillator transconductance | LSEDRV[1:0]=00 lower driving capability | 5 | - | - | µA/V |
| | | LSEDRV[1:0]=01 medium low driving capability | 8 | - | - | |
| | | LSEDRV[1:0]=10 medium high driving capability | 15 | - | - | |
| | | LSEDRV[1:0]=11 higher driving capability | 25 | - | - | |
| $t_{SU(LSE)}$(3) | Startup time | $V_{DD}$ is stabilized | - | 2 | - | s |

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer.

*Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.*

**Figure 16. Typical application with a 32.768 kHz crystal**




*Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.*

### Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

**Table 46. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class |
|---|---|---|---|
| LU | Static latch-up class | $T_A$ = +105 °C conforming to JESD78A | 2 level A |

## 6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below $V_{SS}$ or above $V_{DD}$ (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

### Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence or oscillator frequency deviation).

The test results are given in *Table 47*

**Table 47. I/O current injection susceptibility**

| Symbol | Description | Functional susceptibility | | Unit |
|---|---|---|---|---|
| | | Negative injection | Positive injection | |
| $I_{INJ}$ | Injected current on BOOT0 | -0 | NA | mA |
| | Injected current on PC0 pin (TTa pin) | -0 | +5 | |
| | Injected current PC0, PC1, PC2, PC3, PA0, PA1, PA2, PA3, PA4, PA6, PA7, PC4, PB0, PB10, PB11, PB13 with induced leakage current on other pins from this group less than -100 µA or more than +100 µA | -5 | +5 | |
| | Injected current on any other TT, FT, FTf and NPOR pins | -5 | NA | |
| | Injected current on all other TC, TTa and RESET pins | -5 | +5 | |

### Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed $V_{OL}/V_{OH}$).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating $\Sigma I_{VDD}$ (see *Table 18*).
- The sum of the currents sunk by all the I/Os on $V_{SS}$ plus the maximum Run consumption of the MCU sunk on $V_{SS}$ cannot exceed the absolute maximum rating $\Sigma I_{VSS}$ (see *Table 18*).

### Output voltage levels

Unless otherwise specified, the parameters given in *Table 49* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 20*. All I/Os (FT, TTa and TC unless otherwise specified) are CMOS and TTL compliant.

**Table 49. Output voltage characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$(1) | Output low level voltage for an I/O pin | $I_{IO}$ = +4 mA<br>1.65 V < $V_{DD}$ < 1.95 V | - | 0.4 | V |
| $V_{OH}$(2) | Output high level voltage for an I/O pin | $I_{IO}$ = -4 mA<br>1.65 V < $V_{DD}$ < 1.95 V | $V_{DD}$–0.4 | - | |
| $V_{OLFM+}$(1)(3) | Output low level voltage for an FTf I/O pin in FM+ mode | $I_{IO}$ = +10 mA<br>$V_{DD}$ = 1.65 V to 1.95 V | - | 0.4 | |

1. The $I_{IO}$ current sunk by the device must always respect the absolute maximum rating specified in *Table 18* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $\Sigma I_{IO(PIN)}$.
2. The $I_{IO}$ current sourced by the device must always respect the absolute maximum rating specified in *Table 18* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $\Sigma I_{IO(PIN)}$.
3. Guaranteed by design, not tested in production.

### 6.3.16 Timer characteristics

The parameters given in *Table 53* are guaranteed by design.

Refer to *Section 6.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

**Table 53. TIMx(1)(2) characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{res(TIM)}$ | Timer resolution time | - | 1 | - | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 72 MHz | 13.9 | - | ns |
| | | $f_{TIMxCLK}$ = 144 MHz, x = 1, 15,16, 17 | 6.95 | - | ns |
| $f_{EXT}$ | Timer external clock frequency on CH1 to CH4 | - | 0 | $f_{TIMxCLK}/2$ | MHz |
| | | $f_{TIMxCLK}$ = 72 MHz | 0 | 36 | MHz |
| $Res_{TIM}$ | Timer resolution | TIMx (except TIM2) | - | 16 | bit |
| | | TIM2 | - | 32 | |
| $t_{COUNTER}$ | 16-bit counter clock period | - | 1 | 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 72 MHz | 0.0139 | 910 | µs |
| | | $f_{TIMxCLK}$ = 144 MHz, x= 1/15/16/17 | 0.0069 | 455 | µs |
| $t_{MAX\_COUNT}$ | Maximum possible count with 32-bit counter | - | - | 65536 × 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 72 MHz | - | 59.65 | s |
| | | $f_{TIMxCLK}$ = 144 MHz, x= 1/15/16/17 | - | 29.825 | s |

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM15, TIM16 and TIM17 timers.
2. Guaranteed by design, not tested in production.

**Table 54. IWDG min/max timeout period at 40 kHz (LSI) (1)**

| Prescaler divider | PR[2:0] bits | Min timeout (ms) RL[11:0]= 0x000 | Max timeout (ms) RL[11:0]= 0xFFF |
|---|---|---|---|
| /4 | 0 | 0.1 | 409.6 |
| /8 | 1 | 0.2 | 819.2 |
| /16 | 2 | 0.4 | 1638.4 |
| /32 | 3 | 0.8 | 3276.8 |
| /64 | 4 | 1.6 | 6553.6 |
| /128 | 5 | 3.2 | 13107.2 |
| /256 | 7 | 6.4 | 26214.4 |

1. These timings are given for a 40 kHz clock but the microcontroller internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

**Table 55. WWDG min-max timeout value @72 MHz (PCLK)(1)**

| Prescaler | WDGTB | Min timeout value | Max timeout value |
|---|---|---|---|
| 1 | 0 | 0.05687 | 3.6409 |
| 2 | 1 | 0.1137 | 7.2817 |
| 4 | 2 | 0.2275 | 14.564 |
| 8 | 3 | 0.4551 | 29.127 |

1. Guaranteed by design, not tested in production.

## 6.3.17 Communications interfaces

### I²C interface characteristics

The I2C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I2C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.13: I/O port characteristics* for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

**Table 56. I2C analog filter characteristics(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{AF}$ | Maximum pulse width of spikes that are suppressed by the analog filter | 50(2) | 260(3) | ns |

1. Guaranteed by design, not tested in production.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

## SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 57* for SPI or in *Table 58* for I²S are derived from tests performed under ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 20*.

Refer to *Section 6.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

**Table 57. SPI characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCK}$ $1/t_{c(SCK)}$ | SPI clock frequency | Master mode | - | - | 18 | MHz |
| | | Slave mode | - | - | 18 | |
| | | Slave mode transmitter/full duplex | - | - | 13(2) | |
| $t_{su(NSS)}$ | NSS setup time | Slave mode, SPI presc = 2 | 4*Tpclk | - | - | ns |
| $t_{h(NSS)}$ | NSS hold time | Slave mode, SPI presc = 2 | 2*Tpclk | - | - | |
| $t_{w(SCKH)}$ $t_{w(SCKL)}$ | SCK high and low time | Master mode, $f_{PCLK}$ = 36 MHz, presc = 4 | Tpclk-2 | Tpclk | Tpclk+2 | |
| $t_{su(MI)}$ $t_{su(SI)}$ | Data input setup time | Master mode | 0 | - | - | |
| | | Slave mode | 1 | - | - | |
| $t_{h(MI)}$ | Data input hold time | Master mode | 6.5 | - | - | |
| $t_{h(SI)}$ | | Slave mode | 2.5 | - | - | |
| $t_{a(SO)}$ | Data output access time | Slave mode | 8 | - | 40 | |
| $t_{dis(SO)}$ | Data output disable time | Slave mode | 8 | - | 14 | |
| $t_{v(SO)}$ | Data output valid time | Slave mode | - | 23 | 38 | |
| $t_{v(MO)}$ | | Master mode | - | 1.5 | 4 | |
| $t_{h(SO)}$ | Data output hold time | Slave mode | 9.5 | - | - | |
| $t_{h(MO)}$ | | Master mode | 0 | - | - | |

1. Data based on characterization results, not tested in production.
2. 2.Maximum frequency in Slave transmitter mode is determined by the sum of tv(SO) and tsu(MI) which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having tsu(MI) = 0 while Duty(SCK) = 50%.

**Table 58. I2S characteristics(1) (continued)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{v(WS)}$ | WS valid time | Master mode | - | 20 | ns |
| $t_{h(WS)}$ | WS hold time | Master mode | 2 | - | |
| $t_{su(WS)}$ | WS setup time | Slave mode | 0 | - | |
| $t_{h(WS)}$ | WS hold time | Slave mode | 4 | - | |
| $t_{su(SD\_MR)}$ | Data input setup time | Master receiver | 1 | - | |
| $t_{su(SD\_SR)}$ | | Slave receiver | 1 | - | |
| $t_{h(SD\_MR)}$ | Data input hold time | Master receiver | 8 | - | |
| $t_{h(SD\_SR)}$ | | Slave receiver | 2.5 | - | |
| $t_{v(SD\_ST)}$ | Data output valid time | Slave transmitter (after enable edge) | - | 50 | |
| $t_{v(SD\_MT)}$ | | Master transmitter (after enable edge) | - | 22 | |
| $t_{h(SD\_ST)}$ | Data output hold time | Slave transmitter (after enable edge) | 8 | - | |
| $t_{h(SD\_MT)}$ | | Master transmitter (after enable edge) | 1 | - | |

1. Data based on characterization results, not tested in production.
2. 256xFs maximum is 36 MHz (APB1 Maximum frequency)

*Note: Refer to RM0366 Reference Manual I2S Section for more details about the sampling frequency (Fs), fMCK, fCK, DCK values reflect only the digital peripheral behavior, source clock precision might slightly change the values DCK depends mainly on ODD bit value. Digital contribution leads to a min of (I2SDIV/(2*I2SDIV+ODD) and a max (I2SDIV+ODD)/(2*I2SDIV+ODD) and Fs max supported for each mode/condition.*