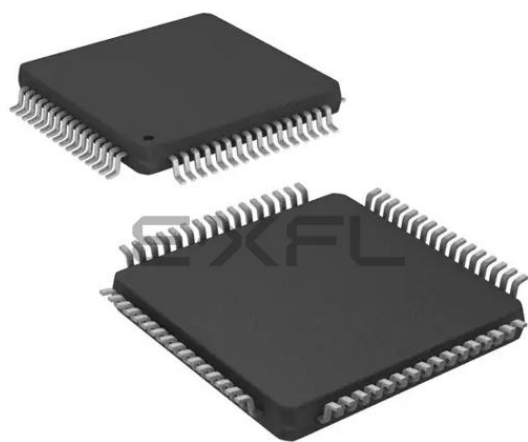




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	51
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256mu806-e-pt

TABLE 4-9: TIMER1 THROUGH TIMER9 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TMR1	0100	Timer1 Register																xxxx
PR1	0102	Period Register 1																FFFF
T1CON	0104	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>	—	TSYNC	TCS	—	—	0000
TMR2	0106	Timer2 Register																xxxx
TMR3HLD	0108	Timer3 Holding Register (for 32-bit timer operations only)																xxxx
TMR3	010A	Timer3 Register																xxxx
PR2	010C	Period Register 2																FFFF
PR3	010E	Period Register 3																FFFF
T2CON	0110	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>	T32	—	TCS	—	—	0000
T3CON	0112	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>	—	—	TCS	—	—	0000
TMR4	0114	Timer4 Register																xxxx
TMR5HLD	0116	Timer5 Holding Register (for 32-bit operations only)																xxxx
TMR5	0118	Timer5 Register																xxxx
PR4	011A	Period Register 4																FFFF
PR5	011C	Period Register 5																FFFF
T4CON	011E	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>	T32	—	TCS	—	—	0000
T5CON	0120	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>	—	—	TCS	—	—	0000
TMR6	0122	Timer6 Register																xxxx
TMR7HLD	0124	Timer7 Holding Register (for 32-bit operations only)																xxxx
TMR7	0126	Timer7 Register																xxxx
PR6	0128	Period Register 6																FFFF
PR7	012A	Period Register 7																FFFF
T6CON	012C	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>	T32	—	TCS	—	—	0000
T7CON	012E	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>	—	—	TCS	—	—	0000
TMR8	0130	Timer8 Register																xxxx
TMR9HLD	0132	Timer9 Holding Register (for 32-bit operations only)																xxxx
TMR9	0134	Timer9 Register																xxxx
PR8	0136	Period Register 8																FFFF
PR9	0138	Period Register 9																FFFF
T8CON	013A	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>	T32	—	TCS	—	—	0000
T9CON	013C	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>	—	—	TCS	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-64: PORTF REGISTER MAP FOR dsPIC33EPXXX(GP/MC)806 AND PIC24EPXXXGP806 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISF	0E50	—	—	—	—	—	—	—	—	—	TRISG6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	003B
PORTF	0E52	—	—	—	—	—	—	—	—	—	RG6	RF5	RF4	RF3	RF2	RF1	RF0	xxxx
LATF	0E54	—	—	—	—	—	—	—	—	—	LATG6	LATF5	LATF4	LATF3	LATF2	LATF1	LATF0	xxxx
ODCF	0E56	—	—	—	—	—	—	—	—	—	ODCF6	ODCF5	ODCF4	ODCF3	ODCF2	ODCF1	ODCF0	0000
CNENF	0E58	—	—	—	—	—	—	—	—	—	CNIEG6	CNIEF5	CNIEF4	CNIEF3	CNIEF2	CNIEF1	CNIEF0	0000
CNPUF	0E5A	—	—	—	—	—	—	—	—	—	CNPUG6	CNPUF5	CNPUF4	CNPUF3	CNPUF2	CNPUF1	CNPUF0	0000
CNPDPF	0E5C	—	—	—	—	—	—	—	—	—	CNPDG6	CNPDPF5	CNPDPF4	CNPDPF3	CNPDPF2	CNPDPF1	CNPDPF0	0000
ANSELF	0E5E	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-65: PORTF REGISTER MAP FOR dsPIC33EPXXXMU806 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISF	0E50	—	—	—	—	—	—	—	—	—	—	TRISF5	TRISF4	TRISF3	—	TRISF1	TRISF0	003B
PORTF	0E52	—	—	—	—	—	—	—	—	—	—	RF5	RF4	RF3	—	RF1	RF0	xxxx
LATF	0E54	—	—	—	—	—	—	—	—	—	—	LATF5	LATF4	LATF3	—	LATF1	LATF0	xxxx
ODCF	0E56	—	—	—	—	—	—	—	—	—	—	ODCF5	ODCF4	ODCF3	—	ODCF1	ODCF0	0000
CNENF	0E58	—	—	—	—	—	—	—	—	—	—	CNIEF5	CNIEF4	CNIEF3	—	CNIEF1	CNIEF0	0000
CNPUF	0E5A	—	—	—	—	—	—	—	—	—	—	CNPUF5	CNPUF4	CNPUF3	—	CNPUF1	CNPUF0	0000
CNPDPF	0E5C	—	—	—	—	—	—	—	—	—	—	CNPDPF5	CNPDPF4	CNPDPF3	—	CNPDPF1	CNPDPF0	0000
ANSELF	0E5E	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-66: PORTG REGISTER MAP FOR dsPIC33EPXXXMU810/814 AND PIC24EPXXXGU810/814 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISG	0E60	TRISG15	TRISG14	TRISG13	TRISG12	—	—	TRISG9	TRISG8	TRISG7	TRISG6	—	—	—	—	TRISG1	TRISG0	F3C3
PORTG	0E62	RG15	RG14	RG13	RG12	—	—	RG9	RG8	RG7	RG6	—	—	RG3 ⁽¹⁾	RG2 ⁽¹⁾	RG1	RG0	xxxx
LATG	0E64	LATG15	LATG14	LATG13	LATG12	—	—	LATG9	LATG8	LATG7	LATG6	—	—	—	—	LATG1	LATG0	xxxx
ODCG	0E66	ODCG15	ODCG14	ODCG13	ODCG12	—	—	—	—	—	—	—	—	—	—	ODCG1	ODCG0	0000
CNENG	0E68	CNIEG15	CNIEG14	CNIEG13	CNIEG12	—	—	CNIEG9	CNIEG8	CNIEG7	CNIEG6	—	—	CNIEG3 ⁽¹⁾	CNIEG2 ⁽¹⁾	CNIEG1	CNIEG0	0000
CNPUG	0E6A	CNPUG15	CNPUG14	CNPUG13	CNPUG12	—	—	CNPUG9	CNPUG8	CNPUG7	CNPUG6	—	—	—	—	CNPUG1	CNPUG0	0000
CNPDPG	0E6C	CNPDPG15	CNPDPG14	CNPDPG13	CNPDPG12	—	—	CNPDPG9	CNPDPG8	CNPDPG7	CNPDPG6	—	—	—	—	CNPDPG1	CNPDPG0	0000
ANSELG	0E6E	—	—	—	—	—	—	ANSG9	ANSG8	ANSG7	ANSG6	—	—	—	—	—	—	03C0

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: If RG2 and RG3 are used as general purpose inputs, the VUSB3V3 pin must be connected to VDD.

REGISTER 6-1: RCON: RESET CONTROL REGISTER⁽¹⁾ (CONTINUED)

bit 3	SLEEP: Wake-up from Sleep Flag bit 1 = Device has been in Sleep mode 0 = Device has not been in Sleep mode
bit 2	IDLE: Wake-up from Idle Flag bit 1 = Device was in Idle mode 0 = Device was not in Idle mode
bit 1	BOR: Brown-out Reset Flag bit 1 = A Brown-out Reset has occurred 0 = A Brown-out Reset has not occurred
bit 0	POR: Power-on Reset Flag bit 1 = A Power-on Reset has occurred 0 = A Power-on Reset has not occurred

- Note 1:** All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.
- 2:** If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

TABLE 11-1: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION) (CONTINUED)

Input Name ⁽¹⁾	Function Name	Register	Configuration Bits
DCI Data Input	CSDI	RPINR24	CSDIR<6:0>
DCI Clock Input	CCKIN	RPINR24	CCKR<6:0>
DCI FSYNC Input	COFSIN	RPINR25	COFSR<6:0>
CAN1 Receive	C1RX	RPINR26	C1RXR<6:0>
CAN2 Receive	C2RX	RPINR26	C2RXR<6:0>
UART3 Receive	U3RX	RPINR27	U3RXR<6:0>
UART3 Clear-to-Send	U3CTS	RPINR27	U3CTSR<6:0>
UART4 Receive	U4RX	RPINR28	U4RXR<6:0>
UART4 Clear-to-Send	U4CTS	RPINR28	U4CTSR<6:0>
SPI3 Data Input	SDI3	RPINR29	SDI3R<6:0>
SPI3 Clock Input	SCK3	RPINR29	SCK3R<6:0>
SPI3 Slave Select	SS3	RPINR30	SS3R<6:0>
SPI4 Data Input	SDI4	RPINR31	SDI4R<6:0>
SPI4 Clock Input	SCK4	RPINR31	SCK4R<6:0>
SPI4 Slave Select	SS4	RPINR32	SS4R<6:0>
Input Capture 9	IC9	RPINR33	IC9R<6:0>
Input Capture 10	IC10	RPINR33	IC10R<6:0>
Input Capture 11	IC11	RPINR34	IC11R<6:0>
Input Capture 12	IC12	RPINR34	IC12R<6:0>
Input Capture 13	IC13	RPINR35	IC13R<6:0>
Input Capture 14	IC14	RPINR35	IC14R<6:0>
Input Capture 15	IC15	RPINR36	IC15R<6:0>
Input Capture 16	IC16	RPINR36	IC16R<6:0>
Output Compare Fault C	OCFC	RPINR37	OCFCR<6:0>
PWM Fault 5 ⁽²⁾	FLT5	RPINR42	FLT5R<6:0>
PWM Fault 6 ⁽²⁾	FLT6	RPINR42	FLT6R<6:0>
PWM Fault 7 ⁽²⁾	FLT7	RPINR43	FLT7R<6:0>
PWM Dead-Time Compensation 1 ⁽²⁾	DTCMP1	RPINR38	DTCMP1R<6:0>
PWM Dead-Time Compensation 2 ⁽²⁾	DTCMP2	RPINR39	DTCMP2R<6:0>
PWM Dead-Time Compensation 3 ⁽²⁾	DTCMP3	RPINR39	DTCMP3R<6:0>
PWM Dead-Time Compensation 4 ⁽²⁾	DTCMP4	RPINR40	DTCMP4R<6:0>
PWM Dead-Time Compensation 5 ⁽²⁾	DTCMP5	RPINR40	DTCMP5R<6:0>
PWM Dead-Time Compensation 6 ⁽²⁾	DTCMP6	RPINR41	DTCMP6R<6:0>
PWM Dead-Time Compensation 7 ⁽²⁾	DTCMP7	RPINR41	DTCMP7R<6:0>
PWM Synch Input 1 ⁽²⁾	SYNCI1	RPINR37	SYNCI1R<6:0>
PWM Synch Input 2 ⁽²⁾	SYNCI2	RPINR38	SYNCI2R<6:0>

Note 1: Unless otherwise noted, all inputs use the Schmitt Trigger input buffers.

2: This input source is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

**REGISTER 11-13: RPINR12: PERIPHERAL PIN SELECT INPUT REGISTER 12
(dsPIC33EPXXXMU806/810/814 DEVICES ONLY)**

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	FLT2R<6:0> ⁽¹⁾						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	FLT1R<6:0> ⁽¹⁾						
bit 7							bit 0

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **FLT2R<6:0>:** Assign PWM Fault 2 ($\overline{\text{FLT2}}$) to the Corresponding RPN/RPIn Pin bits⁽¹⁾
(see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.
.
.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **FLT1R<6:0>:** Assign PWM Fault 1 ($\overline{\text{FLT1}}$) to the Corresponding RPN/RPIn Pin bits⁽¹⁾
(see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.
.
.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

Note 1: These pins are available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

REGISTER 11-31: RPINR31: PERIPHERAL PIN SELECT INPUT REGISTER 31

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SCK4R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SDI4R<6:0>						
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **SCK4R<6:0>:** Assign SPI4 Clock Input (SCK4) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **SDI4R<6:0>:** Assign SPI4 Data Input (SDI4) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

REGISTER 21-10: CxCFG2: ECANx BAUD RATE CONFIGURATION REGISTER 2

U-0	R/W-x	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	WAKFIL	—	—	—	SEG2PH<2:0>		
bit 15						bit 8	

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SEG2PHTS	SAM	SEG1PH<2:0>			PRSEG<2:0>		
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'bit 14 **WAKFIL:** Select CAN Bus Line Filter for Wake-up bit

1 = Uses CAN bus line filter for wake-up

0 = CAN bus line filter is not used for wake-up

bit 13-11 **Unimplemented:** Read as '0'bit 10-8 **SEG2PH<2:0>:** Phase Segment 2 bits

111 = Length is 8 x Tq

•

•

•

000 = Length is 1 x Tq

bit 7 **SEG2PHTS:** Phase Segment 2 Time Select bit

1 = Freely programmable

0 = Maximum of SEG1PH bits or Information Processing Time (IPT), whichever is greater

bit 6 **SAM:** Sample of the CAN Bus Line bit

1 = Bus line is sampled three times at the sample point

0 = Bus line is sampled once at the sample point

bit 5-3 **SEG1PH<2:0>:** Phase Segment 1 bits

111 = Length is 8 x Tq

•

•

•

000 = Length is 1 x Tq

bit 2-0 **PRSEG<2:0>:** Propagation Time Segment bits

111 = Length is 8 x Tq

•

•

•

000 = Length is 1 x Tq

REGISTER 22-3: UxPWRC: USB POWER CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

HS, HC	U-0	U-0	R/W	U-0	U-0	R/W-0, HC	R/W-0
UACTPND	—	—	USLPGRD	—	—	USUSPND	USBPWR ⁽¹⁾
bit 7							bit 0

Legend:	HS = Hardware Settable bit	HC = Hardware Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **UACTPND:** USB Activity Pending bit

- 1 = Module should not be suspended at the moment (requires the USLPGRD bit to be set)
- 0 = Module may be suspended or powered down

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **USLPGRD:** USB Sleep Guard bit

- 1 = Indicates to the USB module that it is about to be suspended or powered down
- 0 = No suspend

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **USUSPND:** USB Suspend Mode Enable bit

- 1 = USB OTG module is in Suspend mode
- 0 = Normal USB OTG operation

bit 0 **USBPWR:** USB Operation Enable bit⁽¹⁾

- 1 = USB OTG module is enabled
- 0 = USB OTG module is disabled

Note 1: Do not clear this bit unless the HOSTEN, USBEN and OTGEN bits (UxCON<3,0> and UxOTGCON<2>) are also cleared.

REGISTER 22-11: UxCNFG2: USB CONFIGURATION REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	UVCMPSEL	PUVBUS	EXTI2CEN	UVBUSDIS ⁽¹⁾	UVCMPDIS ⁽¹⁾	UTRDIS ⁽¹⁾
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'bit 5 **UVCMPSEL:** USB External Comparator Input Mode Select bitWhen UVCMPDIS is Set:

1 = Use 3-pin input for external comparators

0 = Use 2-pin input for external comparators

bit 4 **PUVBUS:** VBUS Pull-up Enable bit

1 = Pull-up on VBUS pin is enabled

0 = Pull-up on VBUS pin is disabled

bit 3 **EXTI2CEN:** I²C™ Interface for External Module Control Enable bit1 = External module(s) controlled via I²C interface

0 = External module(s) controlled via dedicated pins

bit 2 **UVBUSDIS:** USB On-Chip 5V Boost Regulator Builder Disable bit⁽¹⁾

1 = On-chip boost regulator builder is disabled; digital output control interface is enabled

0 = On-chip boost regulator builder is active

bit 1 **UVCMPDIS:** USB On-Chip VBUS Comparator Disable bit⁽¹⁾

1 = On-chip charge VBUS comparator is disabled; digital input status interface is enabled

0 = On-chip charge VBUS comparator is active

bit 0 **UTRDIS:** USB On-Chip Transceiver Disable bit⁽¹⁾

1 = On-chip transceiver is disabled; digital transceiver interface is enabled

0 = On-chip transceiver is active

Note 1: Do not change this bit while the USBPWR bit is set (UxPWRC<0> = 1).

23.4 ADC Control Registers

REGISTER 23-1: ADxCON1: ADCx CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
ADON	—	ADSIDL	ADDMA BM	—	AD12B ⁽¹⁾	FORM<1:0>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0, HSC	R/C-0, HSC
SSRC<2:0>			SSRCG	SIMSAM	ASAM ⁽³⁾	SAMP	DONE ⁽³⁾
bit 7							bit 0

Legend:	C = Clearable bit	HSC = Hardware Settable/Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

- bit 15 **ADON:** ADC Operating Mode bit
 1 = ADC module is operating
 0 = ADC is off
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **ADSIDL:** ADC Stop in Idle Mode bit
 1 = Discontinues module operation when device enters Idle mode
 0 = Continues module operation in Idle mode
- bit 12 **ADDMA BM:** DMA Buffer Build Mode bit
 1 = DMA buffers are written in the order of conversion; the module provides an address to the DMA channel that is the same as the address used for the non-DMA stand-alone buffer
 0 = DMA buffers are written in Scatter/Gather mode; the module provides a Scatter/Gather address to the DMA channel, based on the index of the analog input and the size of the DMA buffer
- bit 11 **Unimplemented:** Read as '0'
- bit 10 **AD12B:** ADC 10-Bit or 12-Bit Operation Mode bit⁽¹⁾
 1 = 12-bit, 1-channel ADC operation
 0 = 10-bit, 4-channel ADC operation
- bit 9-8 **FORM<1:0>:** Data Output Format bits
 For 10-Bit Operation:
 11 = Signed fractional (DOUT = sddd dddd dd00 0000, where s = .NOT.d<9>)
 10 = Fractional (DOUT = dddd dddd dd00 0000)
 01 = Signed integer (DOUT = ssss sssd dddd dddd, where s = .NOT.d<9>)
 00 = Integer (DOUT = 0000 00dd dddd dddd)
 For 12-Bit Operation:
 11 = Signed fractional (DOUT = sddd dddd dddd 0000, where s = .NOT.d<11>)
 10 = Fractional (DOUT = dddd dddd dddd 0000)
 01 = Signed Integer (DOUT = ssss sddd dddd dddd, where s = .NOT.d<11>)
 00 = Integer (DOUT = 0000 dddd dddd dddd)

- Note 1:** This bit is only available in the ADC1 module. In the ADC2 module, this bit is unimplemented and is read as '0'.
- 2:** This setting is available in dsPIC33EPXXX(MC/MU)806/810/814 devices only.
- 3:** Do not clear the DONE bit in software if ADC Sample Auto-Start is enabled (ASAM = 1).

FIGURE 25-2: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM

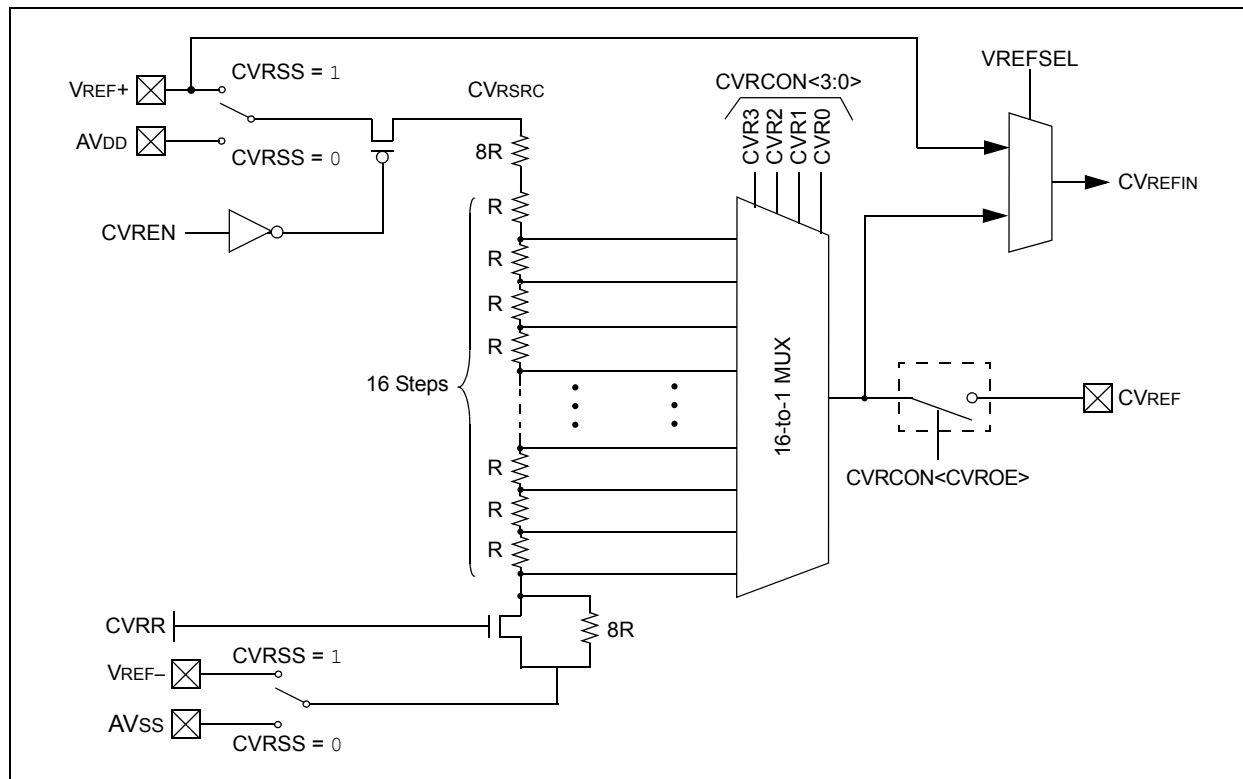
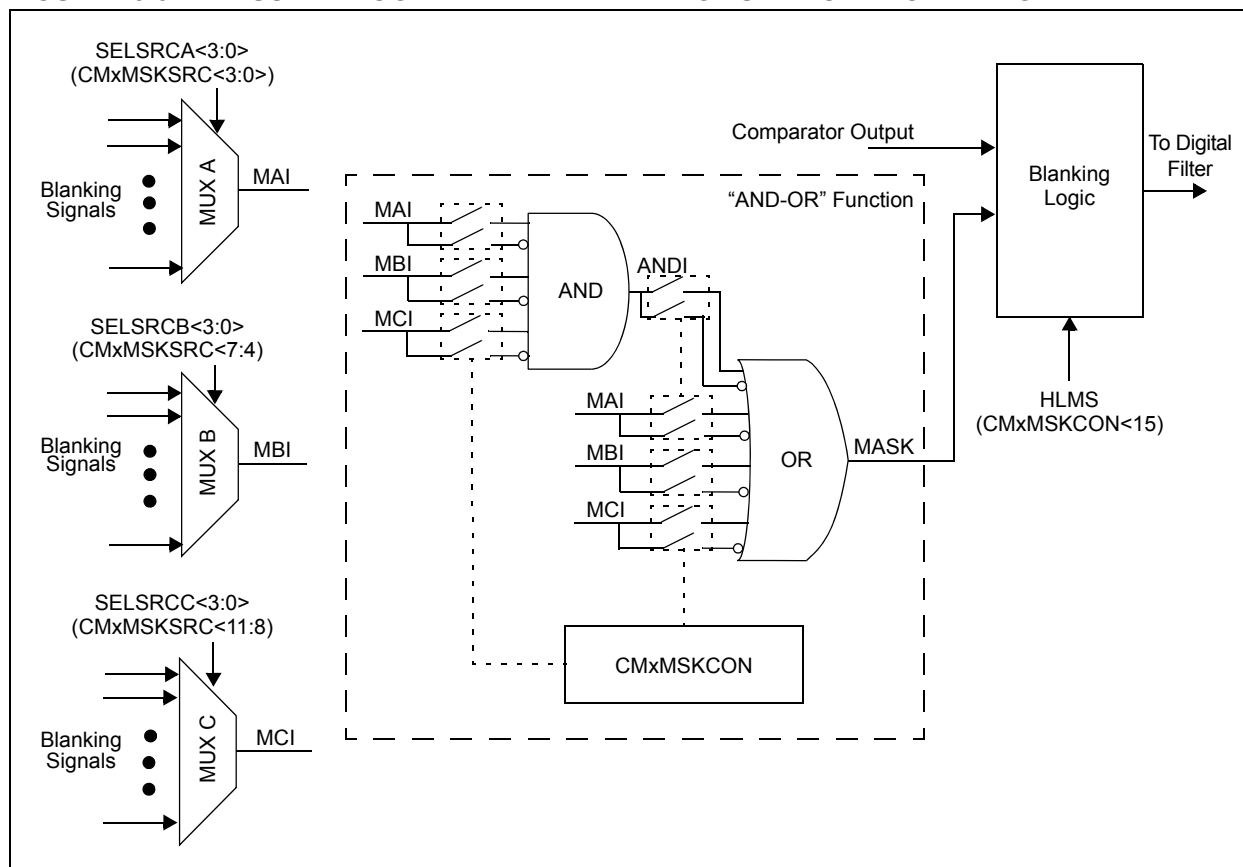


FIGURE 25-3: USER-PROGRAMMABLE BLANKING FUNCTION BLOCK DIAGRAM



REGISTER 28-1: PMCON: PARALLEL MASTER PORT CONTROL REGISTER (CONTINUED)

bit 3	CS1P: Chip Select 0 Polarity bit ⁽¹⁾ 1 = Active-high (<u>PMCS1/PMCS</u>) ⁽²⁾ 0 = Active-low (<u>PMCS1/PMCS</u>)
bit 2	BEP: Byte Enable Polarity bit 1 = Byte enable active-high (<u>PMBE</u>) 0 = Byte enable active-low (<u>PMBE</u>)
bit 1	WRSP: Write Strobe Polarity bit <u>For Slave Modes and Master Mode 2 (PMMODE<9:8> = 00, 01, 10):</u> 1 = Write strobe is active-high (<u>PMWR</u>) 0 = Write strobe is active-low (<u>PMWR</u>) <u>For Master Mode 1 (PMMODE<9:8> = 11):</u> 1 = Enables strobe active-high (<u>PMENB</u>) 0 = Enables strobe active-low (<u>PMENB</u>)
bit 0	RDSP: Read Strobe Polarity bit <u>For Slave Modes and Master Mode 2 (PMMODE<9:8> = 00, 01, 10):</u> 1 = Read strobe is active-high (<u>PMRD</u>) 0 = Read strobe is active-low (<u>PMRD</u>) <u>For Master Mode 1 (PMMODE<9:8> = 11):</u> 1 = Enables strobe active-high (<u>PMRD/PMWR</u>) 0 = Enables strobe active-low (<u>PMRD/PMWR</u>)

Note 1: These bits have no effect when their corresponding pins are used as address lines.

2: PMCS1 applies to Master mode and PMCS applies to Slave mode.

REGISTER 28-4: PMAEN: PARALLEL MASTER PORT ADDRESS ENABLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN15	PTEN14	PTEN13	PTEN12	PTEN11	PTEN10	PTEN9	PTEN8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN7	PTEN6	PTEN5	PTEN4	PTEN3	PTEN2	PTEN1	PTEN0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at Reset

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **PTEN15:** PMCS2 Strobe Enable bit
1 = PMA15 functions as either PMA<15> or PMCS2
0 = PMA15 functions as port I/O
- bit 14 **PTEN14:** PMCS1 Strobe Enable bit
1 = PMA14 functions as either PMA<14> or PMCS1
0 = PMA14 functions as port I/O
- bit 13-2 **PTEN<13:2>:** PMP Address Port Enable bits
1 = PMA<13:2> function as PMP address lines
0 = PMA<13:2> function as port I/O
- bit 1-0 **PTEN<1:0>:** PMALH/PMALL Strobe Enable bits
1 = PMA1 and PMA0 function as either PMA<1:0> or PMALH and PMALL
0 = PMA1 and PMA0 function as port I/O

FIGURE 32-28: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING CHARACTERISTICS

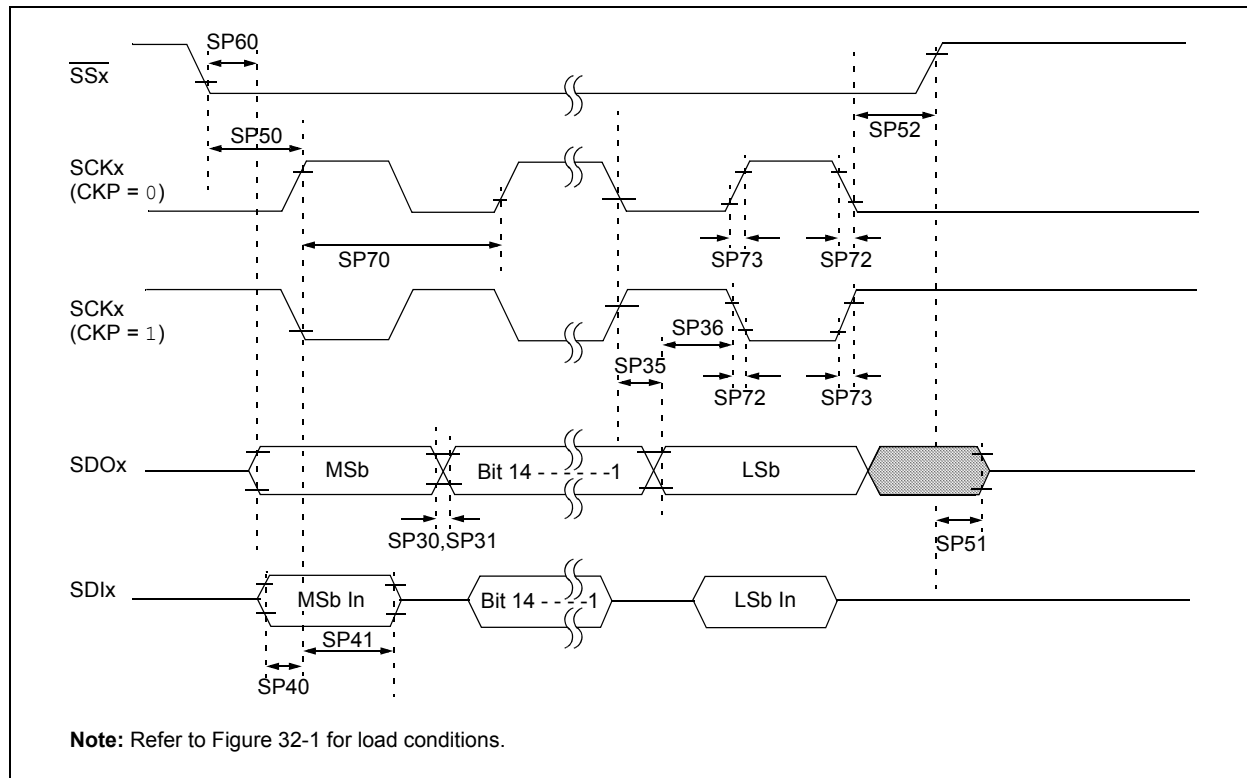


FIGURE 32-29: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS

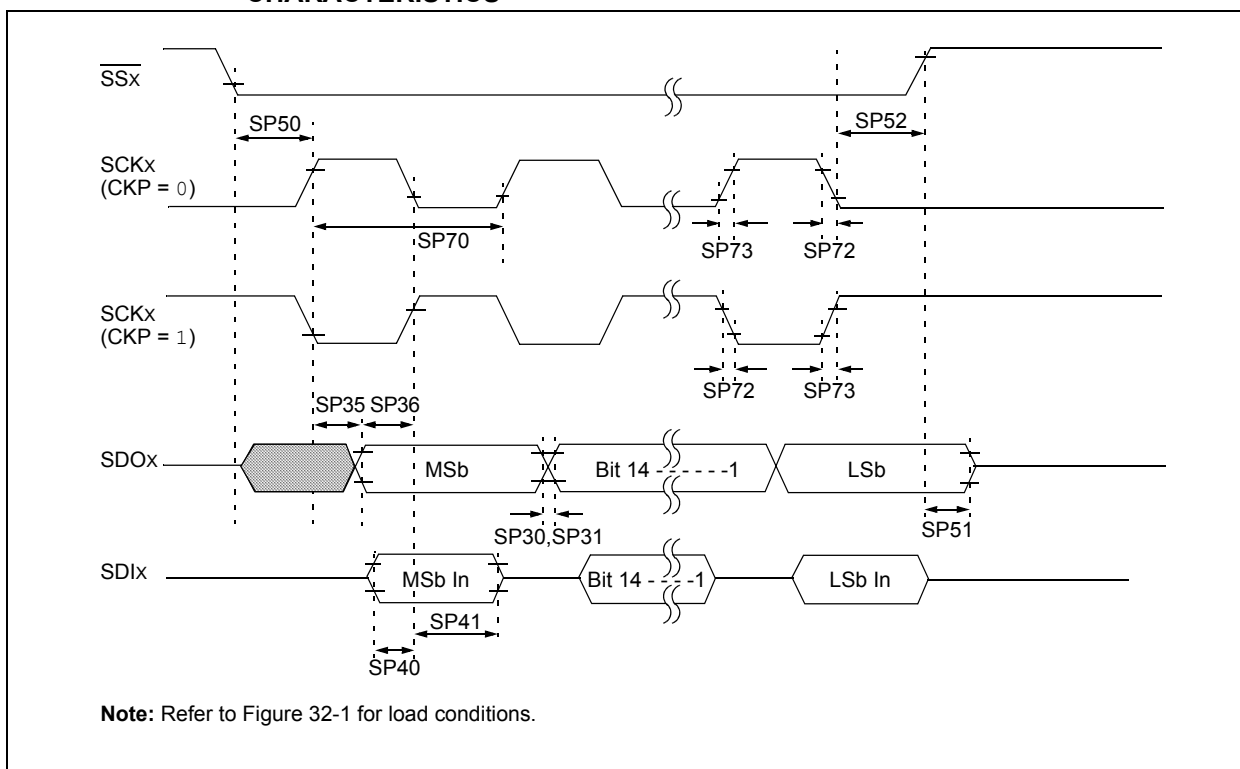


TABLE 32-53: USB OTG MODULE SPECIFICATIONS
(dsPIC33EPXXXMU8XX AND PIC24EPXXXGU8XX DEVICES ONLY)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristics ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
USB313	VUSB3V3 ⁽²⁾	USB Voltage	3.0	—	3.6	V	Voltage on bus must be in this range for proper USB operation
USB315	VILUSB	Input Low Voltage for USB Buffer	—	—	0.8	V	
USB316	VIHUSB	Input High Voltage for USB Buffer	2.0	—	—	V	
USB318	VDIFS	Differential Input Sensitivity	—	—	0.2	V	
USB319	VCM	Differential Common-Mode Range	0.8	—	2.5	V	The difference between D+ and D- must be within this range while VCM is met
USB320	ZOUT	Driver Output Impedance	28.0	—	44.0	Ω	
USB321	VOL	Voltage Output Low	0.0	—	0.3	V	14.25 kΩ load connected to 3.6V
USB322	VOH	Voltage Output High	2.8	—	3.6	V	14.25 kΩ load connected to ground

Note 1: These parameters are characterized but not tested in manufacturing.

2: If the USB module is not being used, this pin must be connected to VDD.

TABLE 32-59: DCI MODULE (MULTI-CHANNEL, I²S MODES) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
CS10	TcSCKL	CCLK Input Low Time (CCLK pin is an input)	$T_{CY}/2 + 20$	—	—	ns	
		CCLK Output Low Time ⁽³⁾ (CCLK pin is an output)	30	—	—	ns	
CS11	TcSCKH	CCLK Input High Time (CCLK pin is an input)	$T_{CY}/2 + 20$	—	—	ns	
		CCLK Output High Time ⁽³⁾ (CCLK pin is an output)	30	—	—	ns	
CS20	TcSCKF	CCLK Output Fall Time (CCLK pin is an output)	—	—	—	ns	See Parameter DO32
CS21	TcSCKR	CCLK Output Rise Time (CCLK pin is an output)	—	—	—	ns	See Parameter DO31
CS30	TcSDOF	CSDO Data Output Fall Time	—	—	—	ns	See Parameter DO32
CS31	TcSDOR	CSDO Data Output Rise Time	—	—	—	ns	See Parameter DO31
CS35	TdV	Clock Edge to CSDO Data Valid	—	—	10	ns	
CS36	TdIV	Clock Edge to CSDO Tri-Stated	10	—	20	ns	
CS40	TcSDI	Setup Time of CSDI Data Input to CCLK Edge (CCLK pin is input or output)	20	—	—	ns	
CS41	THCSDI	Hold Time of CSDI Data Input to CCLK Edge (CCLK pin is input or output)	20	—	—	ns	
CS50	TcOFSF	COFS Fall Time (COFS pin is output)	—	—	—	ns	See Parameter DO32
CS51	TcOFSR	COFS Rise Time (COFS pin is output)	—	—	—	ns	See Parameter DO31
CS55	TsCOFS	Setup Time of COFS Data Input to CCLK Edge (COFS pin is input)	20	—	—	ns	
CS56	THCOFS	Hold Time of COFS Data Input to CCLK Edge (COFS pin is input)	20	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for CCLK is 100 ns. Therefore, the clock generated in Master mode must not violate this specification.

TABLE 32-61: COMPARATOR TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (see Note 3) (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
300	TRESP	Response Time ⁽²⁾	—	150	400	ns	
301	TMC2OV	Comparator Mode Change to Output Valid	—	—	10	μs	

Note 1: Parameters are characterized but not tested.

2: Response time is measured with one comparator input at $(V_{DD} - 1.5)/2$, while the other input transitions from VSS to VDD.

3: Device is functional at $V_{BORMIN} < V_{DD} < V_{DDMIN}$. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.

TABLE 32-62: COMPARATOR MODULE SPECIFICATIONS

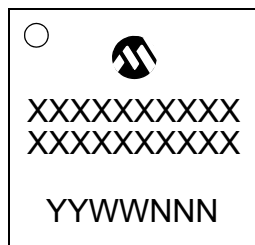
DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (see Note 2) (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
D300	VIOFF	Input Offset Voltage	—	± 10	—	mV	
D301	VICM	Input Common-Mode Voltage	AVSS	—	AVDD	V	
D302	CMRR	Common-Mode Rejection Ratio	-54	—	—	dB	
D305	IVREF	Internal Voltage Reference	0.19	0.20	0.21	V	BGSEL<1:0> = 10
			0.57	0.60	0.63	V	BGSEL<1:0> = 01
			1.14	1.20	1.26	V	BGSEL<1:0> = 00

Note 1: Parameters are characterized but not tested.

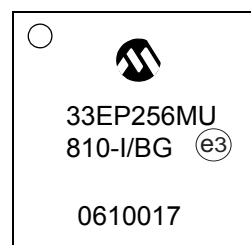
2: Device is functional at $V_{BORMIN} < V_{DD} < V_{DDMIN}$. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.

34.1 Package Marking Information (Continued)

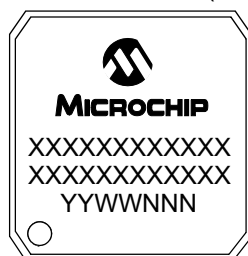
121-Lead TFBGA (10x10x1.2 mm)



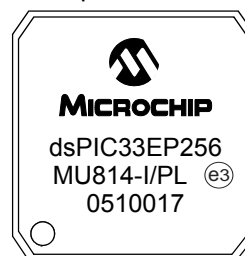
Example



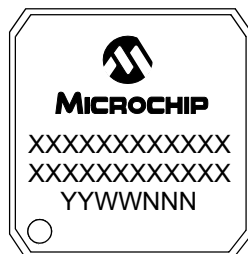
144-Lead LQFP (20x20x1.4 mm)



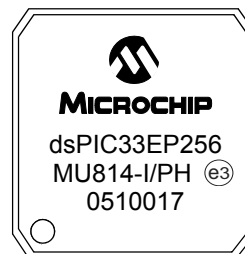
Example



144-Lead TQFP (16x16x1 mm)



Example



NOTES: