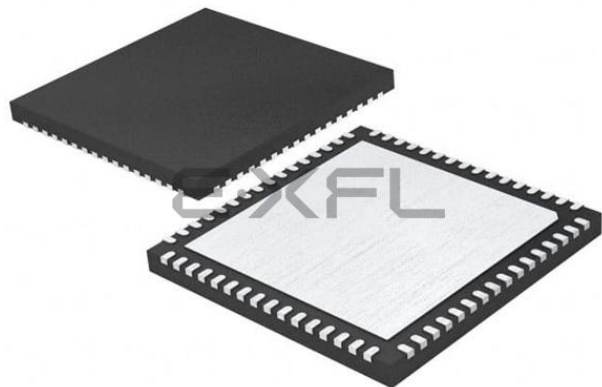




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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	51
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256mu806-i-mr

TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Type	Buffer Type	PPS	Description
AN0-AN31	I	Analog	No	Analog input channels.
CLKI	I	ST/ CMOS	No	External clock source input. Always associated with OSC1 pin function. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
CLKO	O	—	No	Always associated with OSC2 pin function.
OSC1	I	ST/ CMOS	No	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	I/O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
SOSCI	I	ST/ CMOS	No	32.768 kHz low-power oscillator crystal input; CMOS otherwise.
SOSCO	O	—	No	32.768 kHz low-power oscillator crystal output.
IC1-IC16	I	ST	Yes	Capture Inputs 1 through 16.
OCFA	I	ST	Yes	Compare Fault A input (for Compare channels).
OCFB	I	ST	Yes	Compare Fault B input (for Compare channels).
OCFC	I	ST	Yes	Compare Fault C input (for Compare channels).
OC1-OC16	O	—	Yes	Compare Outputs 1 through 16.
INT0	I	ST	No	External Interrupt 0.
INT1	I	ST	Yes	External Interrupt 1.
INT2	I	ST	Yes	External Interrupt 2.
INT3	I	ST	Yes	External Interrupt 3.
INT4	I	ST	Yes	External Interrupt 4.
RA0-RA7, RA9, RA10, RA14, RA15	I/O	ST	No	PORTA is a bidirectional I/O port.
RB0-RB15	I/O	ST	No	PORTB is a bidirectional I/O port.
RC1-RC4, RC12-RC15	I/O	ST	No	PORTC is a bidirectional I/O port.
RD0-RD15	I/O	ST	No	PORTD is a bidirectional I/O port.
RE0-RE9	I/O	ST	No	PORTE is a bidirectional I/O port.
RF0-RF6, RF8 RF12, RF13	I/O	ST	No	PORTF is a bidirectional I/O port.
RG0, RG1	I/O	ST	No	PORTG is a bidirectional I/O port.
RG2, RG3 ⁽³⁾	I/O	ST	No	PORTG is a bidirectional I/O port.
RG6-RG9, RG12-RG15	I/O	ST	No	PORTG is a bidirectional I/O port.
RH0-RH15	I/O	ST	No	PORTH is a bidirectional I/O port.
RJ0-RJ15	I/O	ST	No	PORTJ is a bidirectional I/O port.
RK0-RK1, RK11-RK15	I/O	ST	No	PORTK is a bidirectional I/O port.

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
PPS = Peripheral Pin Select TTL = TTL input buffer

- Note 1:** This pin is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.
- 2:** AVDD must be connected at all times.
- 3:** These pins are input only on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices.
- 4:** These pins are only available on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices.
- 5:** The availability of I²C™ interfaces varies by device. Refer to the “**Pin Diagrams**” section for availability. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 “Special Features”** for more information.
- 6:** Analog functionality is activated by enabling the USB module and is not controlled by the ANSEL register.

TABLE 4-25: ADC1 and ADC2 REGISTER MAP (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
ADC2BUF9	0352	ADCx Data Buffer 9																xxxx	
ADC2BUFA	0354	ADCx Data Buffer 10																xxxx	
ADC2BUFB	0356	ADCx Data Buffer 11																xxxx	
ADC2BUFC	0358	ADCx Data Buffer 12																xxxx	
ADC2BUFD	035A	ADCx Data Buffer 13																xxxx	
ADC2BUFE	035C	ADCx Data Buffer 14																xxxx	
ADC2BUFF	035E	ADCx Data Buffer 15																xxxx	
AD2CON1	0360	ADON	—	ADSIDL	ADDMABM	—	—	FORM<1:0>		SSRC<2:0>			SSRCG	SIMSAM	ASAM	SAMP	DONE	0000	
AD2CON2	0362	VCFG<2:0>			—	—	CSCNA	CHPS<1:0>		BUFS	—	SMPI<3:0>				BUFM	ALTS	0000	
AD2CON3	0364	ADRC	—	—	SAMC<4:0>				ADCS<7:0>										0000
AD2CHS123	0366	—	—	—	—	—	CH123NB<1:0>		CH123SB	—	—	—	—	—	CH123NA<1:0>		CH123SA	0000	
AD2CHS0	0368	CH0NB	—	—	CH0SB<4:0>					CH0NA	—	—	CH0SA<4:0>					0000	
AD2CSSL	0270	CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8	CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0	0000	
AD2CON4	0272	—	—	—	—	—	—	—	ADDMAEN	—	—	—	—	—	DMABL<2:0>			0000	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These bits are not available on dsPIC33EP256MU806 devices.

TABLE 4-28: ECAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 0 OR 1

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C1CTRL1	0400	—	—	CSIDL	ABAT	CANCKS	REQOP<2:0>			OPMODE<2:0>			—	CANCAP	—	—	WIN	0480
C1CTRL2	0402	—	—	—	—	—	—	—	—	—	—	—	DNCNT<4:0>					0000
C1VEC	0404	—	—	—	FILHIT<4:0>					—	ICODE<6:0>							0040
C1FCTRL	0406	DMABS<2:0>			—	—	—	—	—	—	—	—	FSA<4:0>					0000
C1FIFO	0408	—	—	FBP<5:0>						—	—	FNRB<5:0>						0000
C1INTF	040A	—	—	TXBO	TXBP	RXBP	TXWAR	RXWAR	EWARN	IVRIF	WAKIF	ERRIF	—	FIFOIF	RBOVIF	RBIF	TBIF	0000
C1INTE	040C	—	—	—	—	—	—	—	—	IVRIE	WAKIE	ERRIE	—	FIFOIE	RBOVIE	RBIE	TBIE	0000
C1EC	040E	TERRCNT<7:0>								RERRCNT<7:0>								0000
C1CFG1	0410	—	—	—	—	—	—	—	—	SJW<1:0>		BRP<5:0>						0000
C1CFG2	0412	—	WAKFIL	—	—	—	SEG2PH<2:0>			SEG2PHTS	SAM	SEG1PH<2:0>			PRSEG<2:0>			0000
C1FEN1	0414	FLTEN15	FLTEN14	FLTEN13	FLTEN12	FLTEN11	FLTEN10	FLTEN9	FLTEN8	FLTEN7	FLTEN6	FLTEN5	FLTEN4	FLTEN3	FLTEN2	FLTEN1	FLTEN0	FFFF
C1FMSKSEL1	0418	F7MSK<1:0>		F6MSK<1:0>		F5MSK<1:0>		F4MSK<1:0>		F3MSK<1:0>		F2MSK<1:0>		F1MSK<1:0>		F0MSK<1:0>		0000
C1FMSKSEL2	041A	F15MSK<1:0>		F14MSK<1:0>		F13MSK<1:0>		F12MSK<1:0>		F11MSK<1:0>		F10MSK<1:0>		F9MSK<1:0>		F8MSK<1:0>		0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-29: ECAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 0

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
—	0400-041E	See Table 4-28																—
C1RXFUL1	0420	RXFUL15	RXFUL14	RXFUL13	RXFUL12	RXFUL11	RXFUL10	RXFUL9	RXFUL8	RXFUL7	RXFUL6	RXFUL5	RXFUL4	RXFUL3	RXFUL2	RXFUL1	RXFUL0	0000
C1RXFUL2	0422	RXFUL31	RXFUL30	RXFUL29	RXFUL28	RXFUL27	RXFUL26	RXFUL25	RXFUL24	RXFUL23	RXFUL22	RXFUL21	RXFUL20	RXFUL19	RXFUL18	RXFUL17	RXFUL16	0000
C1RXOVF1	0428	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000
C1RXOVF2	042A	RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24	RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16	0000
C1TR01CON	0430	TXEN1	TXABT1	TXLARB1	TXERR1	TXREQ1	RTREN1	TX1PRI<1:0>		TXEN0	TXABAT0	TXLARB0	TXERR0	TXREQ0	RTREN0	TX0PRI<1:0>		0000
C1TR23CON	0432	TXEN3	TXABT3	TXLARB3	TXERR3	TXREQ3	RTREN3	TX3PRI<1:0>		TXEN2	TXABAT2	TXLARB2	TXERR2	TXREQ2	RTREN2	TX2PRI<1:0>		0000
C1TR45CON	0434	TXEN5	TXABT5	TXLARB5	TXERR5	TXREQ5	RTREN5	TX5PRI<1:0>		TXEN4	TXABAT4	TXLARB4	TXERR4	TXREQ4	RTREN4	TX4PRI<1:0>		0000
C1TR67CON	0436	TXEN7	TXABT7	TXLARB7	TXERR7	TXREQ7	RTREN7	TX7PRI<1:0>		TXEN6	TXABAT6	TXLARB6	TXERR6	TXREQ6	RTREN6	TX6PRI<1:0>		xxxx
C1RXD	0440	Received Data Word																xxxx
C1TXD	0442	Transmit Data Word																xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-31: ECAN2 REGISTER MAP WHEN WIN (C2CTRL<0>) = 0 OR 1

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C2CTRL1	0500	—	—	CSIDL	ABAT	CANCKS	REQOP<2:0>			OPMODE<2:0>			—	CANCAP	—	—	WIN	0480
C2CTRL2	0502	—	—	—	—	—	—	—	—	—	—	—	DNCNT<4:0>					0000
C2VEC	0504	—	—	—	FILHIT<4:0>					—	ICODE<6:0>							0040
C2FCTRL	0506	DMABS<2:0>			—	—	—	—	—	—	—	—	FSA<4:0>					0000
C2FIFO	0508	—	—	FBP<5:0>						—	—	FNRB<5:0>						0000
C2INTF	050A	—	—	TXBO	TXBP	RXBP	TXWAR	RXWAR	EWARN	IVRIF	WAKIF	ERRIF	—	FIFOIF	RBOVIF	RBIF	TBIF	0000
C2INTE	050C	—	—	—	—	—	—	—	—	IVRIE	WAKIE	ERRIE	—	FIFOIE	RBOVIE	RBIE	TBIE	0000
C2EC	050E	TERRCNT<7:0>								RERRCNT<7:0>								0000
C2CFG1	0510	—	—	—	—	—	—	—	—	SJW<1:0>		BRP<5:0>						0000
C2CFG2	0512	—	WAKFIL	—	—	—	SEG2PH<2:0>			SEG2PHTS	SAM	SEG1PH<2:0>			PRSEG<2:0>			0000
C2FEN1	0514	FLTEN15	FLTEN14	FLTEN13	FLTEN12	FLTEN11	FLTEN10	FLTEN9	FLTEN8	FLTEN7	FLTEN6	FLTEN5	FLTEN4	FLTEN3	FLTEN2	FLTEN1	FLTEN0	FFFF
C2FMSKSEL1	0518	F7MSK<1:0>		F6MSK<1:0>		F5MSK<1:0>		F4MSK<1:0>		F3MSK<1:0>		F2MSK<1:0>		F1MSK<1:0>		F0MSK<1:0>		0000
C2FMSKSEL2	051A	F15MSK<1:0>		F14MSK<1:0>		F13MSK<1:0>		F12MSK<1:0>		F11MSK<1:0>		F10MSK<1:0>		F9MSK<1:0>		F8MSK<1:0>		0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-32: ECAN2 REGISTER MAP WHEN WIN (C2CTRL<0>) = 0

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
—	0500-051E	See Table 4-31																—
C2RXFUL1	0520	RXFUL15	RXFUL14	RXFUL13	RXFUL12	RXFUL11	RXFUL10	RXFUL9	RXFUL8	RXFUL7	RXFUL6	RXFUL5	RXFUL4	RXFUL3	RXFUL2	RXFUL1	RXFUL0	0000
C2RXFUL2	0522	RXFUL31	RXFUL30	RXFUL29	RXFUL28	RXFUL27	RXFUL26	RXFUL25	RXFUL24	RXFUL23	RXFUL22	RXFUL21	RXFUL20	RXFUL19	RXFUL18	RXFUL17	RXFUL16	0000
C2RXOVF1	0528	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF09	RXOVF08	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000
C2RXOVF2	052A	RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24	RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16	0000
C2TR01CON	0530	TXEN1	TXABAT1	TXLARB1	TXERR1	TXREQ1	RTREN1	TX1PRI<1:0>		TXEN0	TXABAT0	TXLARB0	TXERR0	TXREQ0	RTREN0	TX0PRI<1:0>		0000
C2TR23CON	0532	TXEN3	TXABAT3	TXLARB3	TXERR3	TXREQ3	RTREN3	TX3PRI<1:0>		TXEN2	TXABAT2	TXLARB2	TXERR2	TXREQ2	RTREN2	TX2PRI<1:0>		0000
C2TR45CON	0534	TXEN5	TXABAT5	TXLARB5	TXERR5	TXREQ5	RTREN5	TX5PRI<1:0>		TXEN4	TXABAT4	TXLARB4	TXERR4	TXREQ4	RTREN4	TX4PRI<1:0>		0000
C2TR67CON	0536	TXEN7	TXABAT7	TXLARB7	TXERR7	TXREQ7	RTREN7	TX7PRI<1:0>		TXEN6	TXABAT6	TXLARB6	TXERR6	TXREQ6	RTREN6	TX6PRI<1:0>		xxxx
C2RXD	0540	ECAN2 Received Data Word																xxxx
C2TXD	0542	ECAN2 Transmit Data Word																xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-44: REFERENCE CLOCK REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
REFOCON	074E	ROON	—	ROSSLP	ROSEL	RODIV<3:0>				—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-45: NVM REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
NVMCON	0728	WR	WREN	WRERR	NVMSIDL	—	—	—	—	—	—	—	—	NVMOP<3:0>				0000
NVMADR	072A	NVMADR<15:0>																0000
NVMADRU	072C	—	—	—	—	—	—	—	—	NVMADR<23:16>								0000
NVMKEY	072E	—	—	—	—	—	—	—	—	NVMKEY<7:0>								0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-46: SYSTEM CONTROL REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RCON	0740	TRAPR	IOPUWR	—	—	VREGSF	—	CM	VREGS	EXTR	SWR	SWDTEN	WDTO	SLEEP	IDLE	BOR	POR	Note 1
OSCCON	0742	—	COSC<2:0>			—	NOSC<2:0>			CLKLOCK	IOLOCK	LOCK	—	CF	—	LPOSCEN	OSWEN	Note 2
CLKDIV	0744	ROI	DOZE<2:0>			DOZEN	FRCDIV<2:0>			PLLPOST<1:0>		—	PLLPRE<4:0>					3040
PLLFBD	0746	—	—	—	—	—	—	—	PLLDIV<8:0>									0030
OSCTUN	0748	—	—	—	—	—	—	—	—	—	—	TUN<5:0>						0000
ACLKCON3	0758	ENAPLL	—	SELACLK	AOSCMD<1:0>		ASRCSEL	FRCSEL	—	APLLPOST2<2:0>			—	—	APLLPRE<2:0>			0000
ACLKDIV3	075A	—	—	—	—	—	—	—	—	—	—	—	—	—	APLLDIV<2:0>			0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: RCON register Reset values are dependent on the type of Reset.

Note 2: OSCCON register Reset values are dependent on the Configuration Fuses and by the type of Reset.

REGISTER 8-12: DMARQC: DMA REQUEST COLLISION STATUS REGISTER (CONTINUED)

- bit 2 **RQCOL2:** Channel 2 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected
- bit 1 **RQCOL1:** Channel 1 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected
- bit 0 **RQCOL0:** Channel 0 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

REGISTER 8-14: DMAPPS: DMA PING-PONG STATUS REGISTER

U-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
—	PPST14	PPST13	PPST12	PPST11	PPST10	PPST9	PPST8
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **Unimplemented:** Read as '0'
- bit 14 **PPST14:** Channel 14 Ping-Pong Mode Status Flag bit
 1 = DMASTB14 register selected
 0 = DMASTA14 register selected
- bit 13 **PPST13:** Channel 13 Ping-Pong Mode Status Flag bit
 1 = DMASTB13 register selected
 0 = DMASTA13 register selected
- bit 12 **PPST12:** Channel 12 Ping-Pong Mode Status Flag bit
 1 = DMASTB12 register selected
 0 = DMASTA12 register selected
- bit 11 **PPST11:** Channel 11 Ping-Pong Mode Status Flag bit
 1 = DMASTB11 register selected
 0 = DMASTA11 register selected
- bit 10 **PPST10:** Channel 10 Ping-Pong Mode Status Flag bit
 1 = DMASTB10 register selected
 0 = DMASTA10 register selected
- bit 9 **PPST9:** Channel 9 Ping-Pong Mode Status Flag bit
 1 = DMASTB9 register selected
 0 = DMASTA9 register selected
- bit 8 **PPST8:** Channel 8 Ping-Pong Mode Status Flag bit
 1 = DMASTB8 register selected
 0 = DMASTA8 register selected
- bit 7 **PPST7:** Channel 7 Ping-Pong Mode Status Flag bit
 1 = DMASTB7 register selected
 0 = DMASTA7 register selected
- bit 6 **PPST6:** Channel 6 Ping-Pong Mode Status Flag bit
 1 = DMASTB6 register selected
 0 = DMASTA6 register selected
- bit 5 **PPST5:** Channel 5 Ping-Pong Mode Status Flag bit
 1 = DMASTB5 register selected
 0 = DMASTA5 register selected
- bit 4 **PPST4:** Channel 4 Ping-Pong Mode Status Flag bit
 1 = DMASTB4 register selected
 0 = DMASTA4 register selected
- bit 3 **PPST3:** Channel 3 Ping-Pong Mode Status Flag bit
 1 = DMASTB3 register selected
 0 = DMASTA3 register selected

9.0 OSCILLATOR CONFIGURATION

Note 1: This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7. “Oscillator”** (DS70580) of the “*dsPIC33E/PIC24E Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The oscillator system provides:

- Four external and internal oscillator options
- Auxiliary oscillator that provides clock source to the USB module (if available)
- On-chip Phase-Locked Loop (PLL) to boost internal operating frequency on select internal and external oscillator sources
- On-the-fly clock switching between various clock sources
- Doze mode for system power savings
- Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown
- Nonvolatile Configuration bits for clock source selection

A simplified diagram of the oscillator system is shown in Figure 9-1.

REGISTER 11-59: RPOR15: PERIPHERAL PIN SELECT OUTPUT REGISTER 15

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP127R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP126R<5:0>					
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'bit 13-8 **RP127R<5:0>:** Peripheral Output Function is Assigned to RP127 Output Pin bits
(see Table 11-3 for peripheral function numbers)bit 7-6 **Unimplemented:** Read as '0'bit 5-0 **RP126R<5:0>:** Peripheral Output Function is Assigned to RP126 Output Pin bits
(see Table 11-3 for peripheral function numbers)

REGISTER 17-4: POSxCNTH: POSITION COUNTER x HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSCNT<31:24>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSCNT<23:16>							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **POSCNT<31:16>**: High Word Used to Form 32-Bit Position Counter Register (POSxCNT) bits

REGISTER 17-5: POSxCNTL: POSITION COUNTER x LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSCNT<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSCNT<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **POSCNT<15:0>**: Low Word Used to Form 32-Bit Position Counter Register (POSxCNT) bits

REGISTER 17-6: POSxHLD: POSITION COUNTER x HOLD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSHLD<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSHLD<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **POSHLD<15:0>**: Hold Register for Reading and Writing POSxCNTH bits

REGISTER 17-18: INTxTMRL: INTERVAL TIMER x LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTTMR<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTTMR<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **INTTMR<15:0>**: Low Word Used to Form 32-Bit Interval Timer Register (INTxTMR) bits**REGISTER 17-19: INTxHLDH: INTERVAL TIMER x HOLD HIGH WORD REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<31:24>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<23:16>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **INTHLD<31:16>**: Hold Register for Reading and Writing INTxTMRH bits**REGISTER 17-20: INTxHLDL: INTERVAL TIMER x HOLD LOW WORD REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **INTHLD<15:0>**: Hold Register for Reading and Writing INTxTMRL bits

REGISTER 22-3: UxPWRC: USB POWER CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

HS, HC	U-0	U-0	R/W	U-0	U-0	R/W-0, HC	R/W-0
UACTPND	—	—	USLPGRD	—	—	USUSPND	USBPWR ⁽¹⁾
bit 7							bit 0

Legend:	HS = Hardware Settable bit	HC = Hardware Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **UACTPND:** USB Activity Pending bit

- 1 = Module should not be suspended at the moment (requires the USLPGRD bit to be set)
- 0 = Module may be suspended or powered down

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **USLPGRD:** USB Sleep Guard bit

- 1 = Indicates to the USB module that it is about to be suspended or powered down
- 0 = No suspend

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **USUSPND:** USB Suspend Mode Enable bit

- 1 = USB OTG module is in Suspend mode
- 0 = Normal USB OTG operation

bit 0 **USBPWR:** USB Operation Enable bit⁽¹⁾

- 1 = USB OTG module is enabled
- 0 = USB OTG module is disabled

Note 1: Do not clear this bit unless the HOSTEN, USBEN and OTGEN bits (UxCON<3,0> and UxOTGCON<2>) are also cleared.

REGISTER 22-18: UxEIF: USB ERROR INTERRUPT STATUS REGISTER (DEVICE MODE)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/K-0, HS	R/K-0, HS	R/K-0, HS	R/K-0, HS	R/K-0, HS	R/K-0, HS	R/K-0, HS	R/K-0, HS
BTSEF	BUSACCEF	DMAEF	BTOEF	DFN8EF	CRC16EF	CRC5EF	PIDEF
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	K = Write '1' to clear bit	HS = Hardware Settable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **BTSEF:** Bit Stuff Error Flag bit

- 1 = Bit stuff error has been detected
- 0 = No bit stuff error has been detected

bit 6 **BUSACCEF:** Bus Access Error Flag bit

- 1 = Peripheral tried to access an unimplemented RAM location
- 0 = RAM location access was successful

bit 5 **DMAEF:** DMA Error Flag bit

- 1 = A USB DMA error condition is detected; the data size indicated by the buffer descriptor byte count field is less than the number of received bytes; the received data is truncated
- 0 = No DMA error

bit 4 **BTOEF:** Bus Turnaround Time-out Error Flag bit

- 1 = Bus turnaround time-out has occurred
- 0 = No bus turnaround time-out has occurred

bit 3 **DFN8EF:** Data Field Size Error Flag bit

- 1 = Data field was not an integral number of bytes
- 0 = Data field was an integral number of bytes

bit 2 **CRC16EF:** CRC16 Failure Flag bit

- 1 = CRC16 failed
- 0 = CRC16 passed

bit 1 **CRC5EF:** CRC5 Host Error Flag bit

- 1 = Token packet rejected due to CRC5 error
- 0 = Token packet accepted (no CRC5 error)

bit 0 **PIDEF:** PID Check Failure Flag bit

- 1 = PID check failed
- 0 = PID check passed

NOTES:

REGISTER 23-3: AD2CON2: ADC2 CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
VCFG<2:0>			—	—	CSCNA	CHPS<1:0>	
bit 15							bit 8

R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUFS	—	SMPI<3:0>				BUFM	ALTS
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **VCFG<2:0>**: Converter Voltage Reference Configuration bits

	VREFH	VREFL
000	AVDD	Avss
001	External VREF+	Avss
010	AVDD	External VREF-
011	External VREF+	External VREF-
1xx	AVDD	Avss

bit 12-11 **Unimplemented**: Read as '0'

bit 10 **CSCNA**: Input Scan Select bit

1 = Scans inputs for CH0+ during Sample A bit

0 = Does not scan inputs

bit 9-8 **CHPS<1:0>**: Channel Select bits

When AD12B = 1, CHPS<1:0> is: U-0, Unimplemented. Read as '0':

1x = Converts CH0, CH1, CH2 and CH3

01 = Converts CH0 and CH1

00 = Converts CH0

bit 7 **BUFS**: Buffer Fill Status bit (only valid when BUFM = 1)

1 = ADC is currently filling the second half of the buffer; the user application should access data in the first half of the buffer

0 = ADC is currently filling the first half of the buffer; the user application should access data in the second half of the buffer

bit 6-2 **SMPI<3:0>**: Increment Rate bits

When ADDMAEN = 0:

1111 = Generates interrupt after completion of every 16th sample/conversion operation

1110 = Generates interrupt after completion of every 15th sample/conversion operation

.

.

.

0001 = Generates interrupt after completion of every 2nd sample/conversion operation

0000 = Generates interrupt after completion of every sample/conversion operation

When ADDMAEN = 1:

1111 = Increments the DMA address after completion of every 16th sample/conversion operation

1110 = Increments the DMA address after completion of every 15th sample/conversion operation

.

.

.

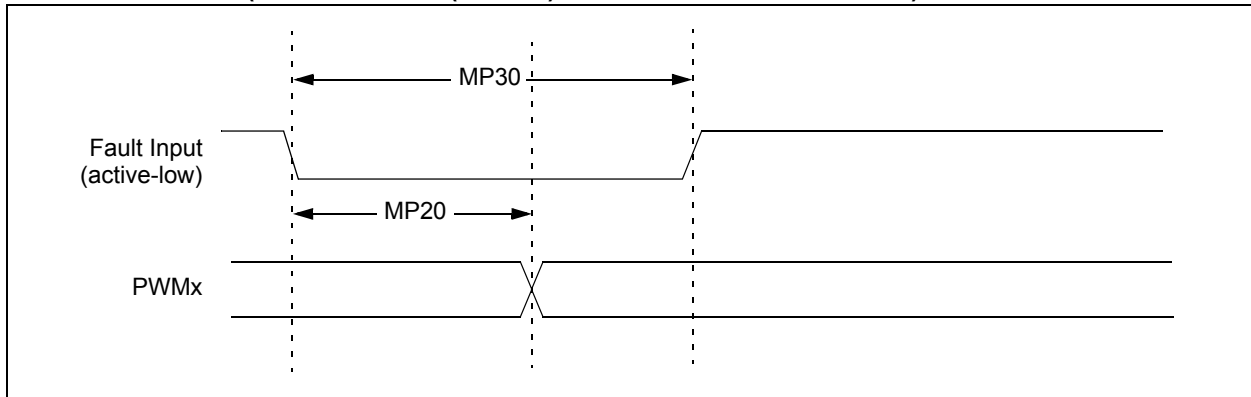
0001 = Increments the DMA address after completion of every 2nd sample/conversion operation

0000 = Increments the DMA address after completion of every sample/conversion operation

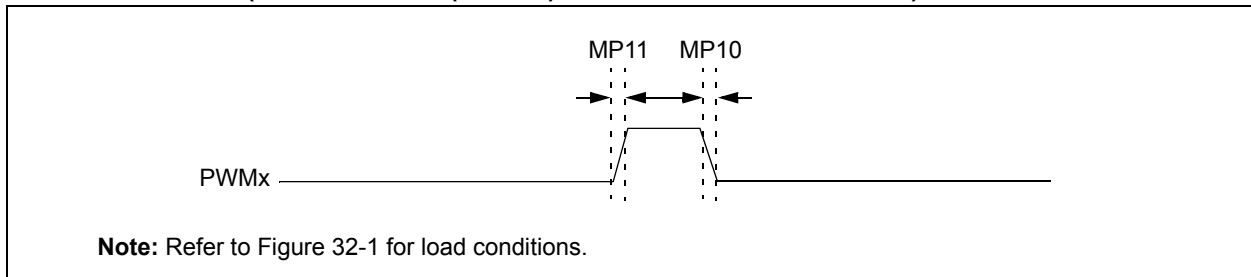
**REGISTER 25-4: CMxMSKCON: COMPARATOR x MASK GATING
CONTROL REGISTER (CONTINUED)**

bit 3	ABEN: AND Gate B Input Enable bit 1 = MBI is connected to AND gate 0 = MBI is not connected to AND gate
bit 2	ABNEN: AND Gate B Input Inverted Enable bit 1 = Inverted MBI is connected to AND gate 0 = Inverted MBI is not connected to AND gate
bit 1	AAEN: AND Gate A Input Enable bit 1 = MAI is connected to AND gate 0 = MAI is not connected to AND gate
bit 0	AAENEN: AND Gate A Input Inverted Enable bit 1 = Inverted MAI is connected to AND gate 0 = Inverted MAI is not connected to AND gate

**FIGURE 32-11: HIGH-SPEED PWMx MODULE FAULT TIMING CHARACTERISTICS
(dsPIC33EPXXX(MC/MU)806/810/814 DEVICES ONLY)**



**FIGURE 32-12: HIGH-SPEED PWMx MODULE TIMING CHARACTERISTICS
(dsPIC33EPXXX(MC/MU)806/810/814 DEVICES ONLY)**



**TABLE 32-30: HIGH-SPEED PWMx MODULE TIMING REQUIREMENTS
(dsPIC33EPXXX(MC/MU)806/810/814 DEVICES ONLY)**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
MP10	T _{FPWM}	PWM Output Fall Time	—	—	—	ns	See Parameter DO32
MP11	T _{RPWM}	PWM Output Rise Time	—	—	—	ns	See Parameter DO31
MP20	T _{FD}	Fault Input ↓ to PWM I/O Change	—	—	15	ns	
MP30	T _{FH}	Fault Input Pulse Width	15	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 32-54: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (see Note 3) (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
Device Supply							
AD01	AVDD ⁽²⁾	Module VDD Supply	Greater of VDD – 0.3 or 3.0	—	Lesser of VDD + 0.3 or 3.6	V	
AD02	AVSS	Module VSS Supply	VSS – 0.3	—	VSS + 0.3	V	
Reference Inputs							
AD05	VREFH	Reference Voltage High	AVSS + 2.5	—	AVDD	V	See Note 1, VREFH = VREF+, VREFL = VREF-
AD05a			3.0	—	3.6	V	VREFH = AVDD, VREFL = AVSS = 0
AD06	VREFL	Reference Voltage Low	AVSS	—	AVDD – 2.5	V	See Note 1
AD06a			0	—	0	V	VREFH = AVDD, VREFL = AVSS = 0
AD07	VREF	Absolute Reference Voltage	2.5	—	3.6	V	VREF = VREFH – VREFL
AD08	IREF	Current Drain	— —	— —	10 600	μA μA	ADC off ADC on
AD09	IAD	Operating Current	— —	9.0 3.2	— —	mA mA	ADC operating in 10-bit mode, see Note 1 ADC operating in 12-bit mode, see Note 1
Analog Input							
AD12	VINH	Input Voltage Range, VINH	VINL	—	VREFH	V	This voltage reflects Sample & Hold Channels 0, 1, 2 and 3 (CH0-CH3), positive input
AD13	VINL	Input Voltage Range, VINL	VREFL	—	AVSS + 1V	V	This voltage reflects Sample & Hold Channels 0, 1, 2 and 3 (CH0-CH3), negative input
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	—	200	Ω	

Note 1: These parameters are not characterized or tested in manufacturing.

2: The voltage difference between AVDD and VDD cannot exceed 300 mV at any time during operation or start-up.

3: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.

TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 4.0 “Memory Organization”	Added the Write Latch and Auxiliary Interrupt Vector to the Program Memory Map (see Figure 4-1). Updated the All Resets value for the DSRPAG and DSWPAG registers in the CPU Core Register Maps (see Table 4-1 and Table 4-2). Updated the All Resets value for the INTCON2 register in the Interrupt Controller Register Maps (see Table 4-3 through Table 4-6). Updated the All Resets values for all registers in the Output Compare 1 - Output Compare 16 Register Map, with the exception of the OCxTMR and OCxCON1 registers (see Table 4-9). Removed the DTM bit (TRGCON1<7>) from all PWM Generator # Register Maps (see Table 4-11 through Table 4-17). Updated the All Resets value for the QE11IOC register in the QE11 Register Map (see Table 4-18). Updated the All Resets value for the QE12IOC register in the QE11 Register Map (see Table 4-19). Added Note 4 to the USB OTG Register Map (see Table 4-25) Updated all addresses in the Real-Time Clock and Calendar Register Map (see Table 4-34). Removed RPINR22 from Table 4-37 through Table 4-40. Updated the All Resets values for all registers in the Peripheral Pin Select Input Register Maps and modified the RPIN37-RPINR43 registers (see Table 4-37 through Table 4-40). Added the VREGSF bit (RCON<11>) to the System Control Register Map (see Table 4-43). Added the REFOMD bit (PMD4<3>) to the PMD Register Maps (see Table 4-44 through Table 4-47). Changed the bit range for CNT from <15:0> to <13:0> for all DMAxCNT registers in the DMAC Register Map (see Table 4-49). Updated the All Resets value and removed the ANSC15 and ANSC12 bits in the ANSLEC registers in the PORTC Register Maps (see Table 4-52 and Table 4-53). Updated DSxPAG and Page Description of O, Read and U, Read in Table 4-66. Added Note to the Table 4-67. Updated Arbiter Architecture in Figure 4-8. Updated the Unimplemented value and removed the LATG3 and LATG2 bits in the LATG registers and the CNPUG3 and CNPUG2 bits from the CNPUG registers in the PORTG Register Maps (see Table 4-60 and Table 4-61) Updated the All Resets value and removed the TRISG3 and TRISG2 bits in the TRISG registers and the ODCG3 and ODCG2 bits from the ODCG registers in the PORTG Register Maps (see Table 4-60 and Table 4-61).
Section 5.0 “Flash Program Memory”	Updated the NVMOP<3:0> = 1110 definition to Reserved and added Note 6 to the Nonvolatile Memory (NVM) Control Register (see Register 5-1).
Section 6.0 “Resets”	Added the VREGSF bit (RCON<11>) to the Reset Control Register (see Register 6-1).

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SPI1, SPI3 and SPI4 Slave Mode (Full-Duplex, CKE = 1, CKP = 0, SMP = 0)	531
SPI1, SPI3 and SPI4 Slave Mode (Full-Duplex, CKE = 1, CKP = 1, SMP = 0)	533
SPI2 Master Mode (Full-Duplex, CKE = 0, CKP = x, SMP = 1)	541
SPI2 Master Mode (Full-Duplex, CKE = 1, CKP = x, SMP = 1)	540
SPI2 Master Mode (Half-Duplex, Transmit Only)	539
SPI2 Slave Mode (Full-Duplex, CKE = 0, CKP = 0, SMP = 0)	549
SPI2 Slave Mode (Full-Duplex, CKE = 0, CKP = 1, SMP = 0)	547
SPI2 Slave Mode (Full-Duplex, CKE = 1, CKP = 0, SMP = 0)	543
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