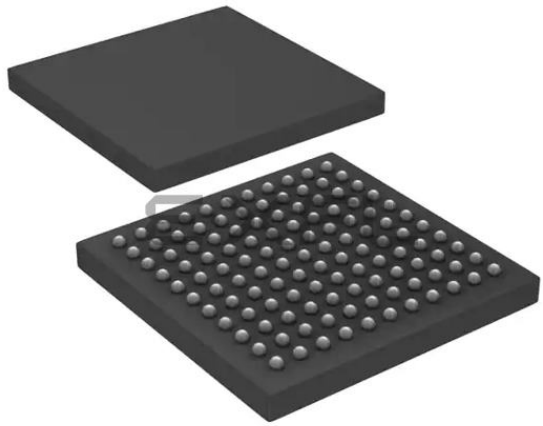
Microchip Technology - DSPIC33EP256MU810-I/BG Datasheet



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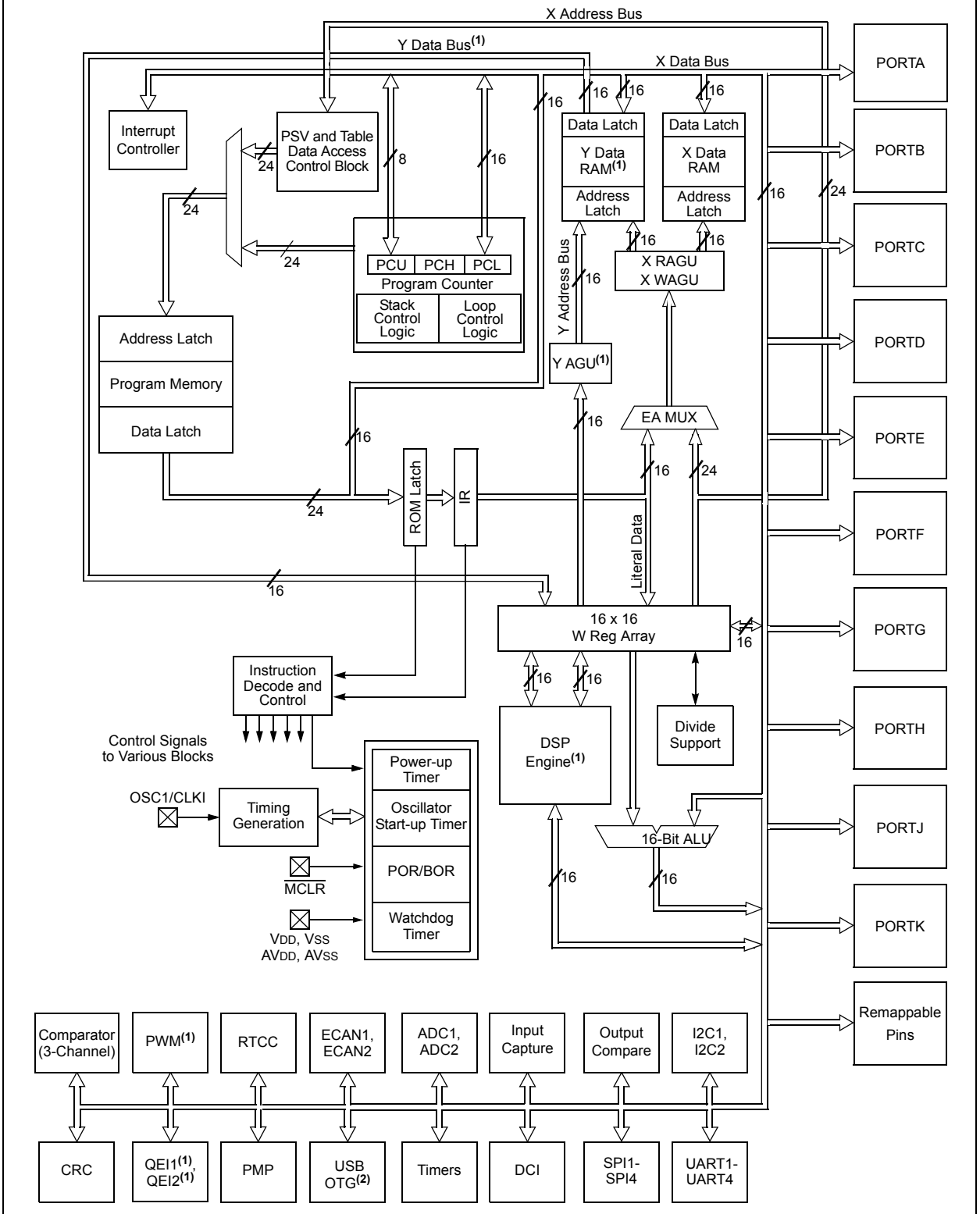
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, QEI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	83
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256mu810-i-bg

FIGURE 3-1: dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 CPU BLOCK DIAGRAM



Note 1: This feature or peripheral is only available on dsPIC33EPXXX(MC/MU)806/810/814 devices.

2: This feature or peripheral is only available on dsPIC33EPXXXMU806/810/814 and PIC24EPXXXGU806/810/814 devices.

TABLE 4-38: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXMU806 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	—	RP65R<5:0>						—	—	RP64R<5:0>						0000
RPOR1	0682	—	—	RP67R<5:0>						—	—	RP66R<5:0>						0000
RPOR2	0684	—	—	RP69R<5:0>						—	—	RP68R<5:0>						0000
RPOR3	0686	—	—	RP71R<5:0>						—	—	RP70R<5:0>						0000
RPOR4	0688	—	—	RP80R<5:0>						—	—	—	—	—	—	—	—	0000
RPOR5	068A	—	—	RP84R<5:0>						—	—	RP82R<5:0>						0000
RPOR6	068C	—	—	RP87R<5:0>						—	—	RP85R<5:0>						0000
RPOR7	068E	—	—	RP97R<5:0>						—	—	RP96R<5:0>						0000
RPOR8	0690	—	—	RP99R<5:0>						—	—	—	—	—	—	—	—	0000
RPOR9	0692	—	—	RP101R<5:0>						—	—	RP100R<5:0>						0000
RPOR13	069A	—	—	RP118R<5:0>						—	—	—	—	—	—	—	—	0000
RPOR14	069C	—	—	—	—	—	—	—	—	—	—	RP120R<5:0>						0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-39: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXX(GP/MC/MU)806 AND PIC24EPXXXGP806 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	—	RP65R<5:0>						—	—	RP64R<5:0>						0000
RPOR1	0682	—	—	RP67R<5:0>						—	—	RP66R<5:0>						0000
RPOR2	0684	—	—	RP69R<5:0>						—	—	RP68R<5:0>						0000
RPOR3	0686	—	—	RP71R<5:0>						—	—	RP70R<5:0>						0000
RPOR4	0688	—	—	RP80R<5:0>						—	—	—	—	—	—	—	—	0000
RPOR5	068A	—	—	RP84R<5:0>						—	—	RP82R<5:0>						0000
RPOR6	068C	—	—	RP87R<5:0>						—	—	RP85R<5:0>						0000
RPOR7	068E	—	—	RP97R<5:0>						—	—	RP96R<5:0>						0000
RPOR8	0690	—	—	RP99R<5:0>						—	—	RP98R<5:0>						0000
RPOR9	0692	—	—	RP101R<5:0>						—	—	RP100R<5:0>						0000
RPOR10	0694	—	—	—	—	—	—	—	—	—	—	RP102R<5:0>						0000
RPOR13	069A	—	—	RP118R<5:0>						—	—	—	—	—	—	—	—	0000
RPOR14	069C	—	—	—	—	—	—	—	—	—	—	RP120R<5:0>						0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.4.4 SOFTWARE STACK

The W15 register serves as a dedicated software Stack Pointer (SP) and is automatically modified by exception processing, subroutine calls and returns; however, W15 can be referenced by any instruction in the same manner as all other W registers. This simplifies reading, writing and manipulating of the Stack Pointer (for example, creating stack frames).

Note:	To protect against misaligned stack accesses, W15<0> is fixed to '0' by the hardware.

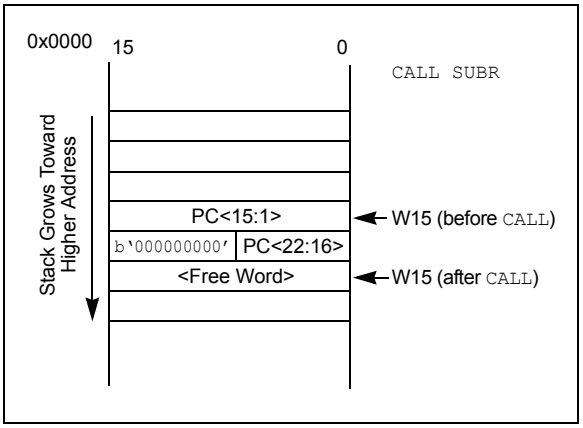
W15 is initialized to 0x1000 during all Resets. This address ensures that the SP points to valid RAM in all dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices and permits stack availability for non-maskable trap exceptions. These can occur before the SP is initialized by the user software. You can reprogram the SP during initialization to any location within data space.

The Stack Pointer always points to the first available free word and fills the software stack working from lower toward higher addresses. Figure 4-9 illustrates how it pre-decrements for a stack pop (read) and post-increments for a stack push (writes).

When the PC is pushed onto the stack, PC<15:0> is pushed onto the first available stack word, then PC<22:16> is pushed into the second available stack location. For a PC push during any CALL instruction, the MSB of the PC is zero-extended before the push, as shown in Figure 4-9. During exception processing, the MSB of the PC is concatenated with the lower 8 bits of the CPU STATUS Register, SR. This allows the contents of SRL to be preserved automatically during interrupt processing.

Note 1:	For main system Stack Pointer (W15) coherency, W15 is never subject to (EDS) paging and is therefore, restricted to the address range of 0x0000 to 0xFFFF. The same applies to W14 when used as a Stack Frame Pointer (SFA = 1).
2:	As the stack can be placed in and across X, Y and DMA RAM spaces, care must be exercised regarding its use, particularly with regard to local automatic variables in a C development environment.

FIGURE 4-9: CALL STACK FRAME



4.5 Instruction Addressing Modes

The addressing modes, shown in Table 4-75, form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

4.5.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire data space.

4.5.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

Operand 3 = Operand 1 <function> Operand 2

where Operand 1 is always a working register (that is, the addressing mode can only be Register Direct), which is referred to as Wb. Operand 2 can be a W register, fetched from data memory, or a 5-bit literal. The result location can be either a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-bit or 10-bit Literal

Note:	Not all instructions support all of the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

5.4 Flash Program Memory Resources

Many useful resources related to Flash program memory are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310

5.4.1 KEY RESOURCES

- **Section 5. "Flash Programming"** (DS70609) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

5.5 Control Registers

Four SFRs are used to read and write the program Flash memory: NVMCON, NVMKEY, NVMADRU and NVMADR.

The NVMCON register (Register 5-1) controls which blocks are to be erased, which memory type is to be programmed and the start of the programming cycle.

NVMKEY (Register 5-4) is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register.

There are two NVM Address registers: NVMADRU and NVMADR. These two registers, when concatenated, form the 24-bit Effective Address (EA) of the selected row or word for programming operations, or the selected page for erase operations.

The NVMADRU register is used to hold the upper 8 bits of the EA, while the NVMADR register is used to hold the lower 16 bits of the EA.

REGISTER 8-12: DMARQC: DMA REQUEST COLLISION STATUS REGISTER

U-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
—	RQCOL14	RQCOL13	RQCOL12	RQCOL11	RQCOL10	RQCOL9	RQCOL8
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
RQCOL7	RQCOL6	RQCOL5	RQCOL4	RQCOL3	RQCOL2	RQCOL1	RQCOL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **RQCOL14:** Channel 14 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 13 **RQCOL13:** Channel 13 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 12 **RQCOL12:** Channel 12 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 11 **RQCOL11:** Channel 11 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 10 **RQCOL10:** Channel 10 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 9 **RQCOL9:** Channel 9 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 8 **RQCOL8:** Channel 8 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 7 **RQCOL7:** Channel 7 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 6 **RQCOL6:** Channel 6 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 5 **RQCOL5:** Channel 5 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 4 **RQCOL4:** Channel 4 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 3 **RQCOL3:** Channel 3 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

REGISTER 10-5: PMD5: PERIPHERAL MODULE DISABLE CONTROL REGISTER 5 (CONTINUED)

bit 3 **OC12MD:** OC12 Module Disable bit
1 = OC12 module is disabled
0 = OC12 module is enabled

bit 2 **OC11MD:** OC11 Module Disable bit
1 = OC11 module is disabled
0 = OC11 module is enabled

bit 1 **OC10MD:** OC10 Module Disable bit
1 = OC10 module is disabled
0 = OC10 module is enabled

bit 0 **OC9MD:** OC9 Module Disable bit
1 = OC9 module is disabled
0 = OC9 module is enabled

REGISTER 11-51: RPOR7: PERIPHERAL PIN SELECT OUTPUT REGISTER 7

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP97R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP96R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP97R<5:0>:** Peripheral Output Function is Assigned to RP97 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP96R<5:0>:** Peripheral Output Function is Assigned to RP96 Output Pin bits (see Table 11-3 for peripheral function numbers)

REGISTER 11-52: RPOR8: PERIPHERAL PIN SELECT OUTPUT REGISTER 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP99R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP98R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP99R<5:0>:** Peripheral Output Function is Assigned to RP99 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP98R<5:0>:** Peripheral Output Function is Assigned to RP98 Output Pin bits (see Table 11-3 for peripheral function numbers)

12.2 Timer1 Control Register

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON(1)	—	TSIDL	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
—	TGATE	TCKPS<1:0>		—	TSYNC(1)	TCS(1)	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timer1 On bit(1)
1 = Starts 16-bit Timer1
0 = Stops 16-bit Timer1

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timer1 Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timer1 Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>** Timer1 Input Clock Prescale Select bits
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3 **Unimplemented:** Read as '0'

bit 2 **TSYNC:** Timer1 External Clock Input Synchronization Select bit(1)
When TCS = 1:
1 = Synchronizes external clock input
0 = Does not synchronize external clock input
When TCS = 0:
This bit is ignored.

bit 1 **TCS:** Timer1 Clock Source Select bit(1)
1 = External clock from T1CK pin (on the rising edge)
0 = Internal clock (FP)

bit 0 **Unimplemented:** Read as '0'

Note 1: When Timer1 is enabled in External Synchronous Counter mode (TCS = 1, TSYNC = 1, TON = 1), any attempts by user software to write to the TMR1 register are ignored.

NOTES:

REGISTER 17-2: QEIxIOC: QEIx I/O CONTROL REGISTER (CONTINUED)

bit 2 **INDEX:** Status of INDXx Input Pin After Polarity Control bit
1 = Pin is at logic '1'
0 = Pin is at logic '0'

bit 1 **QEB:** Status of QEBx Input Pin After Polarity Control And SWPAB Pin Swapping bit
1 = Pin is at logic '1'
0 = Pin is at logic '0'

bit 0 **QEA:** Status of QEAx Input Pin After Polarity Control And SWPAB Pin Swapping bit
1 = Pin is at logic '1'
0 = Pin is at logic '0'

REGISTER 18-2: SPIxCON1: SPIx CONTROL REGISTER 1 (CONTINUED)

bit 4-2 **SPRE<2:0>:** Secondary Prescale bits (Master mode)(3)

111 = Secondary prescale 1:1
110 = Secondary prescale 2:1
•
•
•
000 = Secondary prescale 8:1

bit 1-0 **PPRE<1:0>:** Primary Prescale bits (Master mode)(3)

11 = Primary prescale 1:1
10 = Primary prescale 4:1
01 = Primary prescale 16:1
00 = Primary prescale 64:1

Note 1: The CKE bit is not used in the Framed SPIx modes. Program this bit to '0' for Framed SPIx modes (FRMEN = 1).

2: This bit must be cleared when FRMEN = 1.

3: Do not set both primary and secondary prescalers to a value of 1:1.

4: The SMP bit must be set only after setting the MSTEN bit. The SMP bit remains cleared if MSTEN = 0.

REGISTER 21-24: CxRXOVF1: ECANx RECEIVE BUFFER OVERFLOW REGISTER 1

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0
bit 7							bit 0

Legend:	C = Writable bit, but only ‘0’ can be written to clear the bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **RXOVF<15:0>:** Receive Buffer n Overflow bits
1 = Module attempted to write to a full buffer (set by module)
0 = No overflow condition (cleared by user software)

REGISTER 21-25: CxRXOVF2: ECANx RECEIVE BUFFER OVERFLOW REGISTER 2

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16
bit 7							bit 0

Legend:	C = Writable bit, but only ‘0’ can be written to clear the bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **RXOVF<31:16>:** Receive Buffer n Overflow bits
1 = Module attempted to write to a full buffer (set by module)
0 = No overflow condition (cleared by user software)

REGISTER 22-25: UxBDTP3: USB BUFFER DESCRIPTION TABLE REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BDTPTRU<31:24>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **BDTPTRU<31:24>:** Endpoint BDT Start Address bits
Defines bits 31-24 of the 32-bit endpoint buffer descriptor table start address.

REGISTER 22-26: UxPWMCON: USB VBUS PWM GENERATOR CONTROL REGISTER

R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
PWMEN	—	—	—	—	—	PWMPOL	CNTEN
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **PWMEN:** PWM Enable bit
1 = PWM generator is enabled
0 = PWM generator is disabled; output is held in the Reset state specified by PWMPOL

bit 14-10 **Unimplemented:** Read as ‘0’

bit 9 **PWMPOL:** PWM Polarity bit
1 = PWM output is active-low and resets high
0 = PWM output is active-high and resets low

bit 8 **CNTEN:** PWM Counter Enable bit
1 = Counter is enabled
0 = Counter is disabled

bit 7-0 **Unimplemented:** Read as ‘0’

TABLE 30-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles(2)	Status Flags Affected
25	DAW	DAW	Wn	Wn = decimal adjust Wn	1	1	C
26	DEC	DEC	f	f = f – 1	1	1	C,DC,N,OV,Z
		DEC	f,WREG	WREG = f – 1	1	1	C,DC,N,OV,Z
		DEC	Ws,Wd	Wd = Ws – 1	1	1	C,DC,N,OV,Z
27	DEC2	DEC2	f	f = f – 2	1	1	C,DC,N,OV,Z
		DEC2	f,WREG	WREG = f – 2	1	1	C,DC,N,OV,Z
		DEC2	Ws,Wd	Wd = Ws – 2	1	1	C,DC,N,OV,Z
28	DISI	DISI	#lit14	Disable Interrupts for k instruction cycles	1	1	None
29	DIV	DIV.S	Wm,Wn	Signed 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.SD	Wm,Wn	Signed 32/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.U	Wm,Wn	Unsigned 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.UD	Wm,Wn	Unsigned 32/16-bit Integer Divide	1	18	N,Z,C,OV
30	DIVF	DIVF	Wm,Wn(1)	Signed 16/16-bit Fractional Divide	1	18	N,Z,C,OV
31	DO	DO	#lit15,Expr(1)	Do code to PC + Expr, lit15 + 1 times	2	2	None
		DO	Wn,Expr(1)	Do code to PC + Expr, (Wn) + 1 times	2	2	None
32	ED	ED	Wm*Wm,Acc,Wx,Wy,Wxd(1)	Euclidean Distance (no accumulate)	1	1	OA,OB,OAB, SA,SB,SAB
33	EDAC	EDAC	Wm*Wm,Acc,Wx,Wy,Wxd(1)	Euclidean Distance	1	1	OA,OB,OAB, SA,SB,SAB
34	EXCH	EXCH	Wns,Wnd	Swap Wns with Wnd	1	1	None
35	FBCL	FBCL	Ws,Wnd	Find Bit Change from Left (MSb) Side	1	1	C
36	FF1L	FF1L	Ws,Wnd	Find First One from Left (MSb) Side	1	1	C
37	FF1R	FF1R	Ws,Wnd	Find First One from Right (LSb) Side	1	1	C
38	GOTO	GOTO	Expr	Go to address	2	4	None
		GOTO	Wn	Go to indirect	1	4	None
		GOTO.L	Wn	Go to indirect (long address)	1	4	None
39	INC	INC	f	f = f + 1	1	1	C,DC,N,OV,Z
		INC	f,WREG	WREG = f + 1	1	1	C,DC,N,OV,Z
		INC	Ws,Wd	Wd = Ws + 1	1	1	C,DC,N,OV,Z
40	INC2	INC2	f	f = f + 2	1	1	C,DC,N,OV,Z
		INC2	f,WREG	WREG = f + 2	1	1	C,DC,N,OV,Z
		INC2	Ws,Wd	Wd = Ws + 2	1	1	C,DC,N,OV,Z
41	IOR	IOR	f	f = f .IOR. WREG	1	1	N,Z
		IOR	f,WREG	WREG = f .IOR. WREG	1	1	N,Z
		IOR	#lit10,Wn	Wd = lit10 .IOR. Wd	1	1	N,Z
		IOR	Wb,Ws,Wd	Wd = Wb .IOR. Ws	1	1	N,Z
		IOR	Wb,#lit5,Wd	Wd = Wb .IOR. lit5	1	1	N,Z
42	LAC	LAC	Wso,#Slit4,Acc	Load Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
43	LNK	LNK	#lit14	Link Frame Pointer	1	1	SFA
44	LSR	LSR	f	f = Logical Right Shift f	1	1	C,N,OV,Z
		LSR	f,WREG	WREG = Logical Right Shift f	1	1	C,N,OV,Z
		LSR	Ws,Wd	Wd = Logical Right Shift Ws	1	1	C,N,OV,Z
		LSR	Wb,Wns,Wnd	Wnd = Logical Right Shift Wb by Wns	1	1	N,Z
		LSR	Wb,#lit5,Wnd	Wnd = Logical Right Shift Wb by lit5	1	1	N,Z
45	MAC	MAC	Wm*Wn,Acc,Wx,Wxd,Wy,Wyd,AWB(1)	Multiply and Accumulate	1	1	OA,OB,OAB, SA,SB,SAB
		MAC	Wm*Wm,Acc,Wx,Wxd,Wy,Wyd(1)	Square and Accumulate	1	1	OA,OB,OAB, SA,SB,SAB

Note 1: This instruction is available in dsPIC33EPXXX(GP/MC/MU)806/810/814 devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

TABLE 32-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
Operating Voltage							
DC10	VDD	**Supply Voltage(3)**	3.0	—	3.6	V	
DC12	VDR	**RAM Data Retention Voltage(2)**	1.8	—	—	V	
DC16	VPOR	**VDD Start Voltage** to Ensure Internal Power-on Reset Signal	—	—	VSS	V	
DC17	SVDD	**VDD Rise Rate** to Ensure Internal Power-on Reset Signal	1.0	—	—	V/ms	0-3.0V in 3 ms

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

2: This is the limit to which VDD may be lowered without losing RAM data.

3: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.

FIGURE 32-43: PARALLEL MASTER PORT READ TIMING DIAGRAM

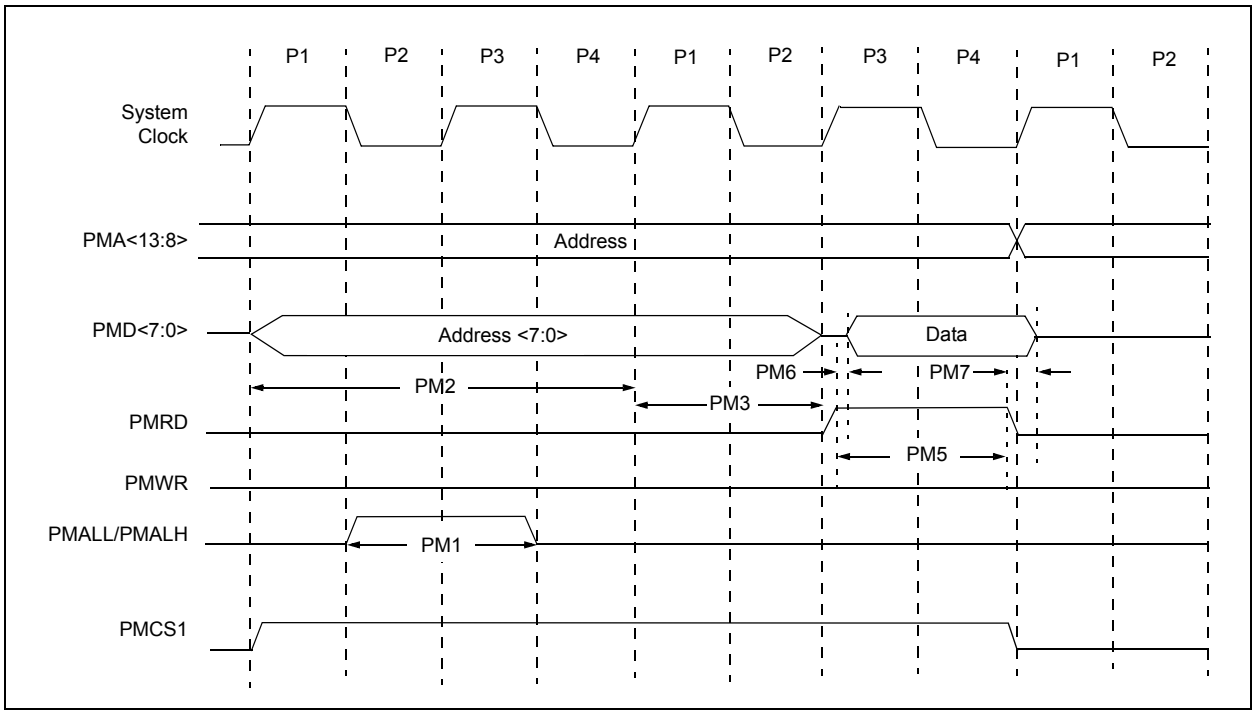


TABLE 32-66: PARALLEL MASTER PORT READ TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Characteristic(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
PM1	PMALL/PMALH Pulse Width	—	0.5 TCY	—	ns	
PM2	Address Out Valid to PMALL/PMALH Invalid (address setup time)	—	1 TCY	—	ns	
PM3	PMALL/PMALH Invalid to Address Out Invalid (address hold time)	—	0.5 TCY	—	ns	
PM5	PMRD Pulse Width	—	0.5 TCY	—	ns	
PM6	PMRD or PMENB Active to Data In Valid (data setup time)	150	—	—	ns	
PM7	PMRD or PMENB Inactive to Data In Invalid (data hold time)	—	—	5	ns	

Note 1: These parameters are characterized, but not tested in manufacturing.

NOTES:

TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 7.0 "Interrupt Controller"	Added the VAR bit (CORCON<15>) to the Core Control Register (see Register 7-2) Changed the default POR value for the GIE bit (INTCON2<15) to R/W-1 (see Register 7-4). Changed the VECNUM<7:0> = 11111111 pending interrupt vector number to 263 in the Interrupt Control and Status Register (see Register 7-7).
Section 8.0 "Direct Memory Access (DMA)"	Updated **Section 8.1 "DMAC Registers"**. Updated DMA Controller in Figure 8-1. Added Note 1 to the DMA Channel x Peripheral Address Register (see Register 8-7). Added Note 1 and Note 2 to the DMA Channel x Transfer Count Register (see Register 8-8). Updated all RQCOLx bit definitions, changing Peripheral Write to Transfer Request in the DMA Request Collision Status Register (see Register 8-12).
Section 9.0 "Oscillator Configuration"	Added the Reference Oscillator Control Register (see Register 9-7). Added Note 3 and 4 to the CLKDIV Register (see Register 9-2)
Section 10.0 "Power-Saving Features"	Added the DCIMD and C2MD bits to the Peripheral Module Disable Control Register 1 (see Register 10-1) Added the IC6MD, IC5MD, IC4MD, IC3MD, OC8MD, OC7MD, OC6MD, and OC5MD bits to the Peripheral Module Disable Control Register 2 (see Register 10-2) Added the T9MD, T8MD, T7MD, and T6MD bits and removed the DSC1MD bit in the Peripheral Module Disable Control Register 3 (see Register 10-3). Added the REFOMD bit (PMD4<3>) to the Peripheral Module Disable Control Register 4 (see Register 10-4).
Section 11.0 "I/O Ports"	Updated the first paragraph of **Section 11.2 "Configuring Analog and Digital Port Pins"**. Updated the PWM Fault, Dead-Time Compensation, and Synch Input register numbers of the Selectable Input Sources (see Table 11-2). Removed RPINR22 register. Bit names and definitions were modified in the following registers: • Peripheral Pin Select Input Register 37 (see Register 11-37) • Peripheral Pin Select Input Register 38 (see Register 11-38) • Peripheral Pin Select Input Register 39 (see Register 11-39) • Peripheral Pin Select Input Register 40 (see Register 11-40) • Peripheral Pin Select Input Register 41 (see Register 11-41) • Peripheral Pin Select Input Register 42 (see Register 11-42) • Peripheral Pin Select Input Register 43 (see Register 11-43)
Section 12.0 "Timer1"	Added Note in Register 12-1.
Section 14.0 "Input Capture"	Added Note 1 to the Input Capture Block Diagram (see Figure 14-1).
Section 15.0 "Output Compare"	Added Note 1 to the Output Compare Module Block Diagram (see Figure 15-1). Added Note 2 to the Output Compare x Control Register 2 (see Register 15-2).
Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMU806/810/814 Devices Only)"	Added Comparator bit values for the CLSRC<4:0> and FLTSRC<4:0> bits in the PWM Fault Current-Limit Control Register (see Register 16-21).

Revision C (May 2011)

This revision includes minor typographical and formatting changes throughout the data sheet text.

These global changes were implemented:

- All instances of VDDCORE have been removed.
- References to remappable pins have been updated to clarify output-only pins (RPn) versus input/output pins (RPIn).
- The minimum VDD value was changed from 2.7V to 3.0V to adhere to the current BOR specification.

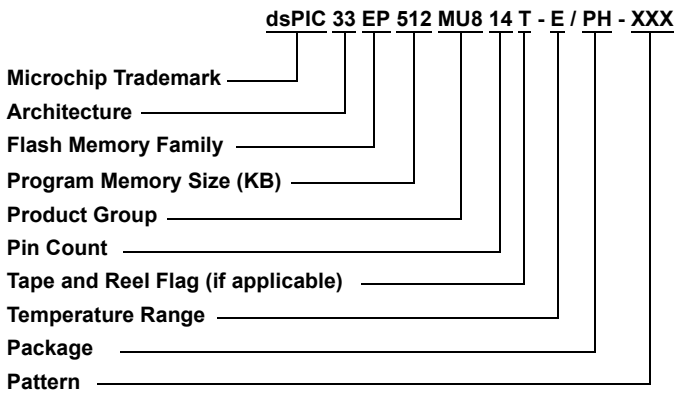
The major changes are referenced by their respective section in Table A-2.

TABLE A-2: MAJOR SECTION UPDATES

Section Name	Update Description
High-Performance, 16-bit Digital Signal Controllers and Microcontrollers	Removed the shading for D+/RG2 and D-/RG3 pin designations in all pin diagrams, as these pins are not 5V tolerant. References to remappable pins have been updated to clarify input/output pins (RPn) and input-only pins (RPIn).
Section 2.0 "Guidelines for Getting Started with 16-bit Digital Signal Controllers and Microcontrollers"	Add information on the VUSB pin in **Section 2.1 "Basic Connection Requirements"**. Updated the title of Section 2.3 to **Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)"** and modified the first paragraph.
Section 3.0 "CPU"	Added Note 2 to the Programmer's Model Register Descriptions (see Table 3-1).
Section 4.0 "Memory Organization"	Added the CANCKS bit (CxCTRL1<11>) to the ECAN1 and ECAN 2 Register Maps (see Table 4-26 and Table 4-29). Added the SBOREN bit (RCON<13>) to the System Control Register Map (see Table 4-43). Added Note 1 to the PORTG Register maps (see Table 4-60 and Table 4-61). Updated the Page Description for DSRPAG = 0x1FF and DSRPAG = 0x200 in Table 4-66. Updated the second paragraph of **Section 4.2.9 "EDS Arbitration and Bus Master Priority"**. Updated the last note box in **Section 4.2.10 "Software Stack"**.
Section 5.0 "Flash Program Memory"	Updated the equation formatting in **Section 5.3 "Programming Operations"**. Added the Non-Volatile Memory Upper Address (NVMADRU) and Non-Volatile Memory Address (NVMADR) registers (see Register 5-2 and Register 5-3).
Section 6.0 "Resets"	Added Security Reset to the Reset System Block Diagram (see Figure 6-1). Added the SBOREN bit (RCON<13>) and Notes 3 and 4 to the Reset Control register (see Register 6-1).
Section 11.0 "I/O Ports"	References to remappable pins have been updated to clarify input/output pins (RPn) and input-only pins (RPIn). Added the new column, Input/Output, to Input Pin Selection for Selectable Input Sources (see Table 11-2).
Section 17.0 "Quadrature Encoder Interface (QEI) Module (dsPIC33EPXXXMU806/810/814 Devices Only)"	Updated the definition for the INTHLD<31:0> bits (see Register 17-19 and Register 17-20).

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Architecture:	33	=	16-bit Digital Signal Controller
	24	=	16-bit Microcontroller
Flash Memory Family:	EP	=	Enhanced Performance
Product Group:	MU8	=	Motor Control family with USB
	GU8	=	General Purpose family with USB
Pin Count:	06	=	64-pin
	10	=	100-pin, 121-pin
	14	=	144-pin
Temperature Range:	I	=	-40°C to+85°C (Industrial)
	E	=	-40°C to+125°C (Extended)
Package:	PT	=	10x10 or 12x12 mm TQFP (Thin Quad Flatpack)
	PF	=	14x14 mm TQFP (Thin Quad Flatpack)
	MR	=	9x9 mm QFN (Plastic Quad Flatpack)
	BG	=	10x10 mm TFBGA (Plastic Thin Profile Ball Grid Array)
	PH	=	16x16 mm TQFP (Thin Quad Flatpack)
	PL	=	20x20 mm LQFP (Low-Profile Quad Flatpack)

Examples:

a) dsPIC33EP512MU814T-E/PH:
Motor Control with USB dsPIC33,
512 KB program memory, 144-pin,
Extended temperature, TQFP package.