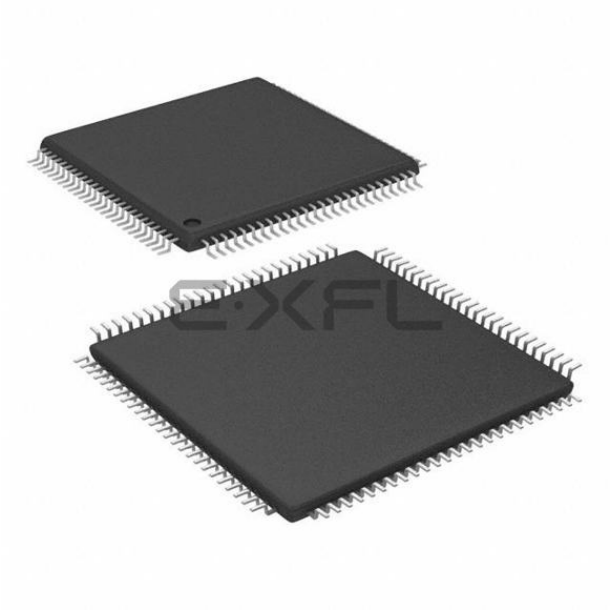

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, QEI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	83
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256mu810t-e-pf

Pin Diagrams (Continued)

121-Pin TFBGA(1)

● = Pins are up to 5V tolerant

PIC24EP256GU810
PIC24EP512GU810

	1	2	3	4	5	6	7	8	9	10	11
A	RE4	RE3	RG13	RE0	RG0	RF1	VDD	NC	RD12	RD2	RD1
B	NC	RG15	RE2	RE1	RA7	RF0	VCAP	RD5	RD3	VSS	RC14
C	RE6	VDD	RG12	RG14	RA6	NC	RD7	RD4	NC	RC13	RD11
D	RC1	RE7	RE5	NC	NC	NC	RD6	RD13	RD0	NC	RD10
E	RC4	RC3	RG6	RC2	NC	RG1	NC	RA15	RD8	RD9	RA14
F	$\overline{\text{MCLR}}$	RG8	RG9	RG7	VSS	NC	NC	VDD	RC12	VSS	RC15
G	RE8	RE9	RA0	NC	VDD	VSS	VSS	NC	RA5	RA3	RA4
H	RB5	RB4	NC	NC	NC	VDD	NC	VBUS	VUSB3V3	RG2	RA2
J	RB3	RB2	RB7	AVDD	RB11	RA1	RB12	NC	NC	RF8	RG3
K	RB1	RB0	RA10	RB8	NC	RF12	RB14	VDD	RD15	RF3	RF2
L	RB6	RA9	AVSS	RB9	RB10	RF13	RB13	RB15	RD14	RF4	RF5

Note 1: Refer to Table 3 for full pin names.

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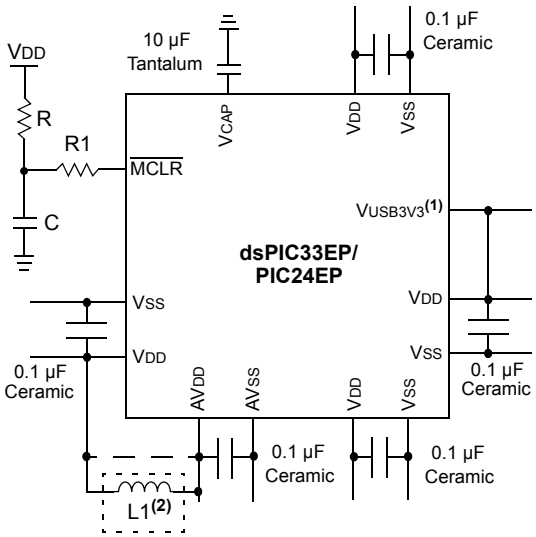
FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



Note 1: If the USB module is not used, V_{USB3V3} must be connected to V_{DD}, as shown.

2: As an option, instead of a hard-wired connection, an inductor (L1) can be substituted between V_{DD} and AV_{DD} to improve ADC noise rejection. The inductor impedance should be less than 1Ω and the inductor capacity greater than 10 mA.

Where:

$$f = \frac{F_{CNV}}{2} \quad \text{(i.e., ADC conversion rate/2)}$$

$$f = \frac{1}{(2\pi\sqrt{LC})}$$

$$L = \left(\frac{1}{(2\pi f\sqrt{C})}\right)^2$$

2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

2.3 CPU Logic Filter Capacitor Connection (V_{CAP})

A low-ESR (< 1 Ohms) capacitor is required on the V_{CAP} pin, which is used to stabilize the voltage regulator output voltage. The V_{CAP} pin must not be connected to V_{DD} and must have a capacitor greater than 4.7 µF (10 µF is recommended), 16V connected to ground. The type can be ceramic or tantalum. See **Section 32.0 "Electrical Characteristics"** for additional information.

The placement of this capacitor should be close to the V_{CAP}. It is recommended that the trace length not exceeds one-quarter inch (6 mm). See **Section 29.2 "On-Chip Voltage Regulator"** for details.

2.4 Master Clear ($\overline{MCLR}$) Pin

The $\overline{MCLR}$ pin provides two specific device functions:

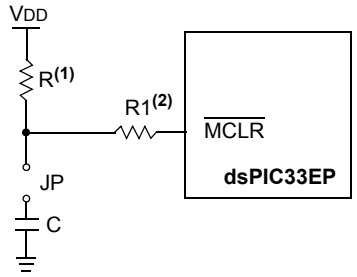
- Device Reset
- Device Programming and Debugging

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{MCLR}$ pin. Consequently, specific voltage levels (V_{IH} and V_{IL}) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-2, it is recommended that the capacitor C, be isolated from the $\overline{MCLR}$ pin during programming and debugging operations.

Place the components as shown in Figure 2-2 within one-quarter inch (6 mm) from the $\overline{MCLR}$ pin.

FIGURE 2-2: EXAMPLE OF $\overline{MCLR}$ PIN CONNECTIONS



Note 1: R ≤ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the $\overline{MCLR}$ pin V_{IH} and V_{IL} specifications are met.

2: R1 ≤ 470Ω will limit any current flowing into $\overline{MCLR}$ from the external capacitor C, in the event of $\overline{MCLR}$ pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the $\overline{MCLR}$ pin V_{IH} and V_{IL} specifications are met.

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FIGURE 2-7: INTERLEAVED PFC

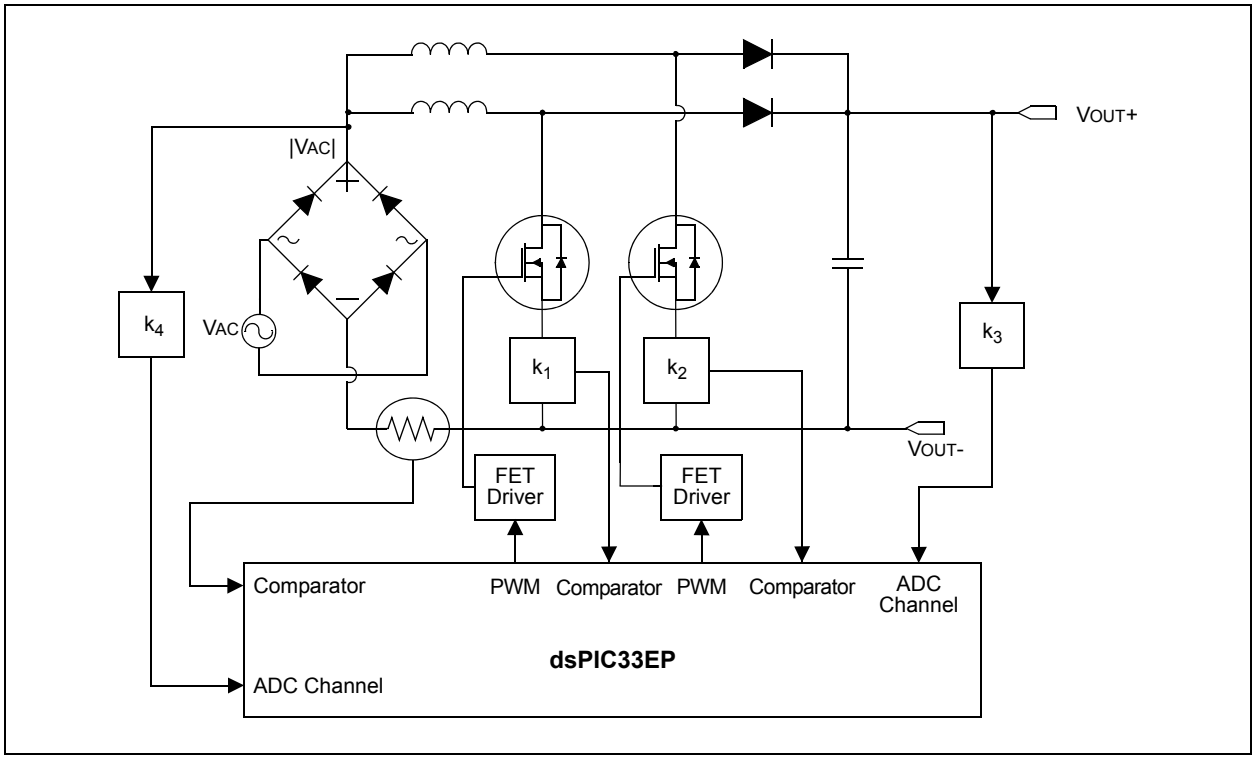

FIGURE 2-8: BEMF VOLTAGE MEASURED USING THE ADC MODULE

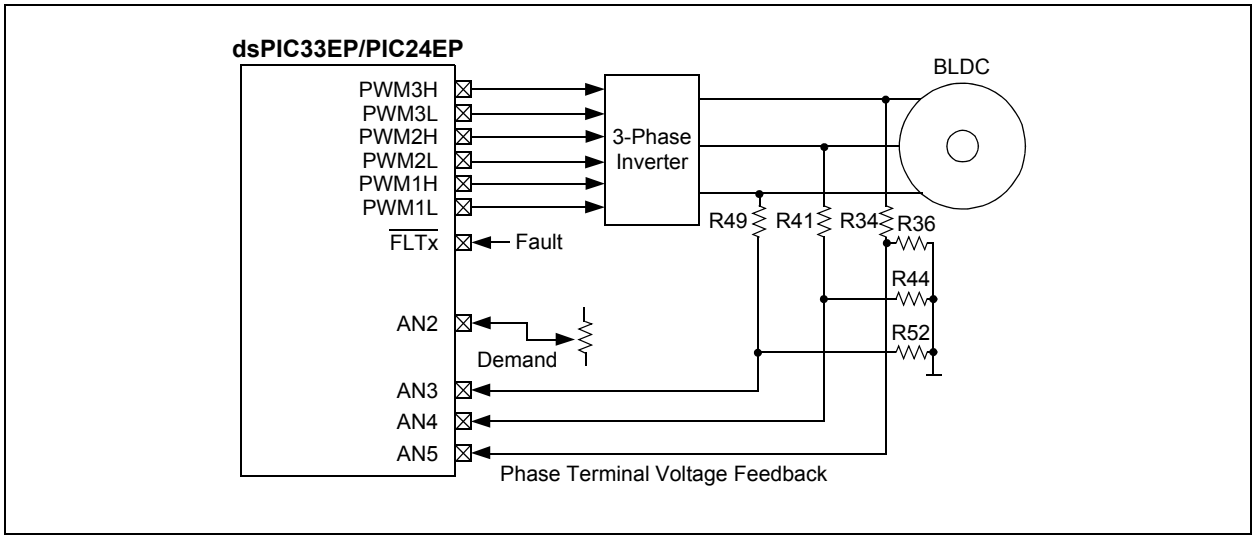

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TABLE 4-30: ECAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 1

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
—	0400-041E	See Table 4-28																—
C1BUFPNT1	0420	F3BP<3:0>				F2BP<3:0>				F1BP<3:0>				F0BP<3:0>				0000
C1BUFPNT2	0422	F7BP<3:0>				F6BP<3:0>				F5BP<3:0>				F4BP<3:0>				0000
C1BUFPNT3	0424	F11BP<3:0>				F10BP<3:0>				F9BP<3:0>				F8BP<3:0>				0000
C1BUFPNT4	0426	F15BP<3:0>				F14BP<3:0>				F13BP<3:0>				F12BP<3:0>				0000
C1RXM0SID	0430	SID<10:3>								SID<2:0>			—	MIDE	—	EID<17:16>		xxxx
C1RXM0EID	0432	EID<15:8>								EID<7:0>								xxxx
C1RXM1SID	0434	SID<10:3>								SID<2:0>			—	MIDE	—	EID<17:16>		xxxx
C1RXM1EID	0436	EID<15:8>								EID<7:0>								xxxx
C1RXM2SID	0438	SID<10:3>								SID<2:0>			—	MIDE	—	EID<17:16>		xxxx
C1RXM2EID	043A	EID<15:8>								EID<7:0>								xxxx
C1RXF0SID	0440	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF0EID	0442	EID<15:8>								EID<7:0>								xxxx
C1RXF1SID	0444	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF1EID	0446	EID<15:8>								EID<7:0>								xxxx
C1RXF2SID	0448	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF2EID	044A	EID<15:8>								EID<7:0>								xxxx
C1RXF3SID	044C	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF3EID	044E	EID<15:8>								EID<7:0>								xxxx
C1RXF4SID	0450	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF4EID	0452	EID<15:8>								EID<7:0>								xxxx
C1RXF5SID	0454	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF5EID	0456	EID<15:8>								EID<7:0>								xxxx
C1RXF6SID	0458	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF6EID	045A	EID<15:8>								EID<7:0>								xxxx
C1RXF7SID	045C	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF7EID	045E	EID<15:8>								EID<7:0>								xxxx
C1RXF8SID	0460	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF8EID	0462	EID<15:8>								EID<7:0>								xxxx
C1RXF9SID	0464	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF9EID	0466	EID<15:8>								EID<7:0>								xxxx
C1RXF10SID	0468	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF10EID	046A	EID<15:8>								EID<7:0>								xxxx
C1RXF11SID	046C	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-53: COMPARATOR REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMSTAT	0A80	CMSIDL	—	—	—	—	C3EVT	C2EVT	C1EVT	—	—	—	—	—	C3OUT	C2OUT	C1OUT	0000
CVRCON	0A82	—	—	—	—	—	VREFSEL	BGSEL<1:0>		CVREN	CVROE	CVRR	CVRSS	CVR<3:0>				0000
CM1CON	0A84	CON	COE	CPOL	—	—	—	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
CM1MSKSRC	0A86	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
CM1MSKCON	0A88	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM1FLTR	0A8A	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000
CM2CON	0A8C	CON	COE	CPOL	—	—	—	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
CM2MSKSRC	0A8E	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
CM2MSKCON	0A90	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM2FLTR	0A92	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000
CM3CON	0A94	CON	COE	CPOL	—	—	—	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
CM3MSKSRC	0A96	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
CM3MSKCON	0A98	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM3FLTR	0A9A	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 7-1: INTERRUPT VECTOR DETAILS (CONTINUED)

Interrupt Source	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
				Flag	Enable	Priority
USB1 – USB OTG Interrupt(2)	94	86	0x0000C0	IFS5<6>	IEC5<6>	IPC21<10:8>
U4E – UART4 Error Interrupt	95	87	0x0000C2	IFS5<7>	IEC5<7>	IPC21<14:12>
U4RX – UART4 Receiver	96	88	0x0000C4	IFS5<8>	IEC5<8>	IPC22<2:0>
U4TX – UART4 Transmitter	97	89	0x0000C6	IFS5<9>	IEC5<9>	IPC22<6:4>
SPI3E – SPI3 Error	98	90	0x0000C8	IFS5<10>	IEC5<10>	IPC22<10:8>
SPI3 – SPI3 Transfer Done	99	91	0x0000CA	IFS5<11>	IEC5<11>	IPC22<14:12>
OC9 – Output Compare 9	100	92	0x0000CC	IFS5<12>	IEC5<12>	IPC23<2:0>
IC9 – Input Capture 9	101	93	0x0000CE	IFS5<13>	IEC5<13>	IPC23<6:4>
PWM1 – PWM Generator 1(1)	102	94	0x0000D0	IFS5<14>	IEC5<14>	IPC23<10:8>
PWM2 – PWM Generator 2(1)	103	95	0x0000D2	IFS5<15>	IEC5<15>	IPC23<14:12>
PWM3 – PWM Generator 3(1)	104	96	0x0000D4	IFS6<0>	IEC6<0>	IPC24<2:0>
PWM4 – PWM Generator 4(1)	105	97	0x0000D6	IFS6<1>	IEC6<1>	IPC24<6:4>
PWM5 – PWM Generator 5(1)	106	98	0x0000D8	IFS6<2>	IEC6<2>	IPC24<10:8>
PWM6 – PWM Generator 6(1)	107	99	0x0000DA	IFS6<3>	IEC6<3>	IPC24<14:12>
PWM7 – PWM Generator 7(1)	108	100	0x0000DC	IFS6<4>	IEC6<4>	IPC25<2:0>
Reserved	109-125	101-117	0x0000DE-0x0000FC	—	—	—
DMA8 – DMA Channel 8	126	118	0x000100	IFS7<6>	IEC7<6>	IPC29<10:8>
DMA9 – DMA Channel 9	127	119	0x000102	IFS7<7>	IEC7<7>	IPC29<14:12>
DMA10 – DMA Channel 10	128	120	0x000104	IFS7<8>	IEC7<8>	IPC30<2:0>
DMA11 – DMA Channel 11	129	121	0x000106	IFS7<9>	IEC7<9>	IPC30<6:4>
SPI4E – SPI4 Error	130	122	0x000108	IFS7<10>	IEC7<10>	IPC30<10:8>
SPI4 – SPI4 Transfer Done	131	123	0x00010A	IFS7<11>	IEC7<11>	IPC30<14:12>
OC10 – Output Compare 10	132	124	0x00010C	IFS7<12>	IEC7<12>	IPC31<2:0>
IC10 – Input Capture 10	133	125	0x00010E	IFS7<13>	IEC7<13>	IPC31<6:4>
OC11 – Output Compare11	134	126	0x000110	IFS7<14>	IEC7<14>	IPC31<10:8>
IC11 – Input Capture 11	135	127	0x000112	IFS7<15>	IEC7<15>	IPC31<14:12>
OC12 – Output Compare 12	136	128	0x000114	IFS8<0>	IEC8<0>	IPC32<2:0>
IC12 – Input Capture 12	137	129	0x000116	IFS8<1>	IEC8<1>	IPC32<6:4>
DMA12 – DMA Channel 12	138	130	0x000118	IFS8<2>	IEC8<2>	IPC32<10:8>
DMA13– DMA Channel 13	139	131	0x00011A	IFS8<3>	IEC8<3>	IPC32<14:12>
DMA14 – DMA Channel 14	140	132	0x00011C	IFS8<4>	IEC8<4>	IPC33<2:0>
Reserved	141	133	0x00011E	—	—	—
OC13 – Output Compare 13	142	134	0x000120	IFS8<6>	IEC8<6>	IPC33<10:8>
IC13 – Input Capture 13	143	135	0x000122	IFS8<7>	IEC8<7>	IPC33<14:12>
OC14 – Output Compare14	144	136	0x000124	IFS8<8>	IEC8<8>	IPC34<2:0>
IC14 – Input Capture 14	145	137	0x000126	IFS8<9>	IEC8<9>	IPC34<6:4>
OC15 – Output Compare 15	146	138	0x000128	IFS8<10>	IEC8<10>	IPC34<10:8>
IC15 – Input Capture 15	147	139	0x00012A	IFS8<11>	IEC8<11>	IPC34<14:12>
OC16 – Output Compare 16	148	140	0x00012C	IFS8<12>	IEC8<12>	IPC35<2:0>
IC16 – Input Capture 16	149	141	0x00012E	IFS8<13>	IEC8<13>	IPC35<6:4>
ICD – ICD Application	150	142	0x000130	IFS8<14>	IEC8<14>	IPC35<10:8>
Reserved	151-245	142-237	0x000130-0x0001FE	—	—	—
Lowest Natural Order Priority						

Note 1: This interrupt source is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

2: This interrupt source is available on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices only.

REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1 (CONTINUED)

bit 4 **MATHERR:** Math Error Status bit
1 = Math error trap has occurred
0 = Math error trap has not occurred

bit 3 **ADDRERR:** Address Error Trap Status bit
1 = Address error trap has occurred
0 = Address error trap has not occurred

bit 2 **STKERR:** Stack Error Trap Status bit
1 = Stack error trap has occurred
0 = Stack error trap has not occurred

bit 1 **OSCFAIL:** Oscillator Failure Trap Status bit
1 = Oscillator failure trap has occurred
0 = Oscillator failure trap has not occurred

bit 0 **Unimplemented:** Read as '0'

Note 1: This bit is available on dsPIC33EPXXX(GP/MC/MU)806/810/814 devices only.

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REGISTER 8-3: DMAxSTAH: DMA CHANNEL x START ADDRESS REGISTER A (HIGH)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STA<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **STA<23:16>:** Primary Start Address bits (source or destination)

REGISTER 8-4: DMAxSTAL: DMA CHANNEL x START ADDRESS REGISTER A (LOW)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STA<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STA<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **STA<15:0>:** Primary Start Address bits (source or destination)

REGISTER 8-12: DMARQC: DMA REQUEST COLLISION STATUS REGISTER (CONTINUED)

bit 2 **RQCOL2:** Channel 2 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 1 **RQCOL1:** Channel 1 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 0 **RQCOL0:** Channel 0 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

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9.3 Oscillator Control Registers

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER(1,3)

U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	R/W-y
—	COSC<2:0>			—	NOSC<2:0>(2)		
bit 15							bit 8

R/W-0	R/W-0	R-0	U-0	R/C-0	U-0	R/W-0	R/W-0
CLKLOCK	IOLOCK	LOCK	—	CF	—	LPOSCEN	OSWEN
bit 7							bit 0

Legend:	y = Value Set from Configuration bits on POR		C = Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits (read-only)
- 111 = Fast RC Oscillator (FRC) with Divide-by-N
- 110 = Fast RC Oscillator (FRC) with Divide-by-16
- 101 = Low-Power RC Oscillator (LPRC)
- 100 = Secondary Oscillator (SOSC)
- 011 = Primary Oscillator (XT, HS, EC) with PLL
- 010 = Primary Oscillator (XT, HS, EC)
- 001 = Fast RC Oscillator (FRC) with Divide-by-N and PLL
- 000 = Fast RC Oscillator (FRC)

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits(2)
- 111 = Fast RC Oscillator (FRC) with Divide-by-N
- 110 = Fast RC Oscillator (FRC) with Divide-by-16
- 101 = Low-Power RC Oscillator (LPRC)
- 100 = Secondary Oscillator (SOSC)
- 011 = Primary Oscillator (XT, HS, EC) with PLL
- 010 = Primary Oscillator (XT, HS, EC)
- 001 = Fast RC Oscillator (FRC) with Divide-by-N and PLL
- 000 = Fast RC Oscillator (FRC)

bit 7 **CLKLOCK:** Clock Lock Enable bit
- 1 = If (FCKSM0 = 1), then clock and PLL configurations are locked
  If (FCKSM0 = 0), then clock and PLL configurations may be modified
- 0 = Clock and PLL selections are not locked, configurations may be modified

bit 6 **IOLOCK:** I/O Lock Enable bit
- 1 = I/O lock is active
- 0 = I/O lock is not active

bit 5 **LOCK:** PLL Lock Status bit (read-only)
- 1 = Indicates that PLL is in lock or PLL start-up timer is satisfied
- 0 = Indicates that PLL is out of lock, start-up timer is in progress or PLL is disabled

bit 4 **Unimplemented:** Read as ‘0’

Note 1: Writes to this register require an unlock sequence. Refer to **Section 7. “Oscillator”** (DS70580) in the *“dsPIC33E/PIC24E Family Reference Manual”* (available from the Microchip web site) for details.

2: Direct clock switches between any Primary Oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.

3: This register resets only on a Power-on Reset (POR).

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REGISTER 10-6: PMD6: PERIPHERAL MODULE DISABLE CONTROL REGISTER 6

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	PWM7MD(1)	PWM6MD(1)	PWM5MD(1)	PWM4MD(1)	PWM3MD(1)	PWM2MD(1)	PWM1MD(1)
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	SPI4MD	SPI3MD
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14 **PWM7MD:** PWM7 Module Disable bit(1)
1 = PWM7 module is disabled
0 = PWM7 module is enabled

bit 13 **PWM6MD:** PWM6 Module Disable bit(1)
1 = PWM6 module is disabled
0 = PWM6 module is enabled

bit 12 **PWM5MD:** PWM5 Module Disable bit(1)
1 = PWM5 module is disabled
0 = PWM5 module is enabled

bit 11 **PWM4MD:** PWM4 Module Disable bit(1)
1 = PWM4 module is disabled
0 = PWM4 module is enabled

bit 10 **PWM3MD:** PWM3 Module Disable bit(1)
1 = PWM3 module is disabled
0 = PWM3 module is enabled

bit 9 **PWM2MD:** PWM2 Module Disable bit(1)
1 = PWM2 module is disabled
0 = PWM2 module is enabled

bit 8 **PWM1MD:** PWM1 Module Disable bit(1)
1 = PWM1 module is disabled
0 = PWM1 module is enabled

bit 7-2 **Unimplemented:** Read as ‘0’

bit 1 **SPI4MD:** SPI4 Module Disable bit
1 = SPI4 module is disabled
0 = SPI4 module is enabled

bit 0 **SPI3MD:** SPI3 Module Disable bit
1 = SPI3 module is disabled
0 = SPI3 module is enabled

Note 1: This bit is available in dsPIC33EPXXX(MC/MU)806/810/814 devices only.

REGISTER 11-49: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP84R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP82R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP84R<5:0>:** Peripheral Output Function is Assigned to RP84 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP82R<5:0>:** Peripheral Output Function is Assigned to RP82 Output Pin bits (see Table 11-3 for peripheral function numbers)

REGISTER 11-50: RPOR6: PERIPHERAL PIN SELECT OUTPUT REGISTER 6

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP87R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP85R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP87R<5:0>:** Peripheral Output Function is Assigned to RP87 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP85R<5:0>:** Peripheral Output Function is Assigned to RP85 Output Pin bits (see Table 11-3 for peripheral function numbers)

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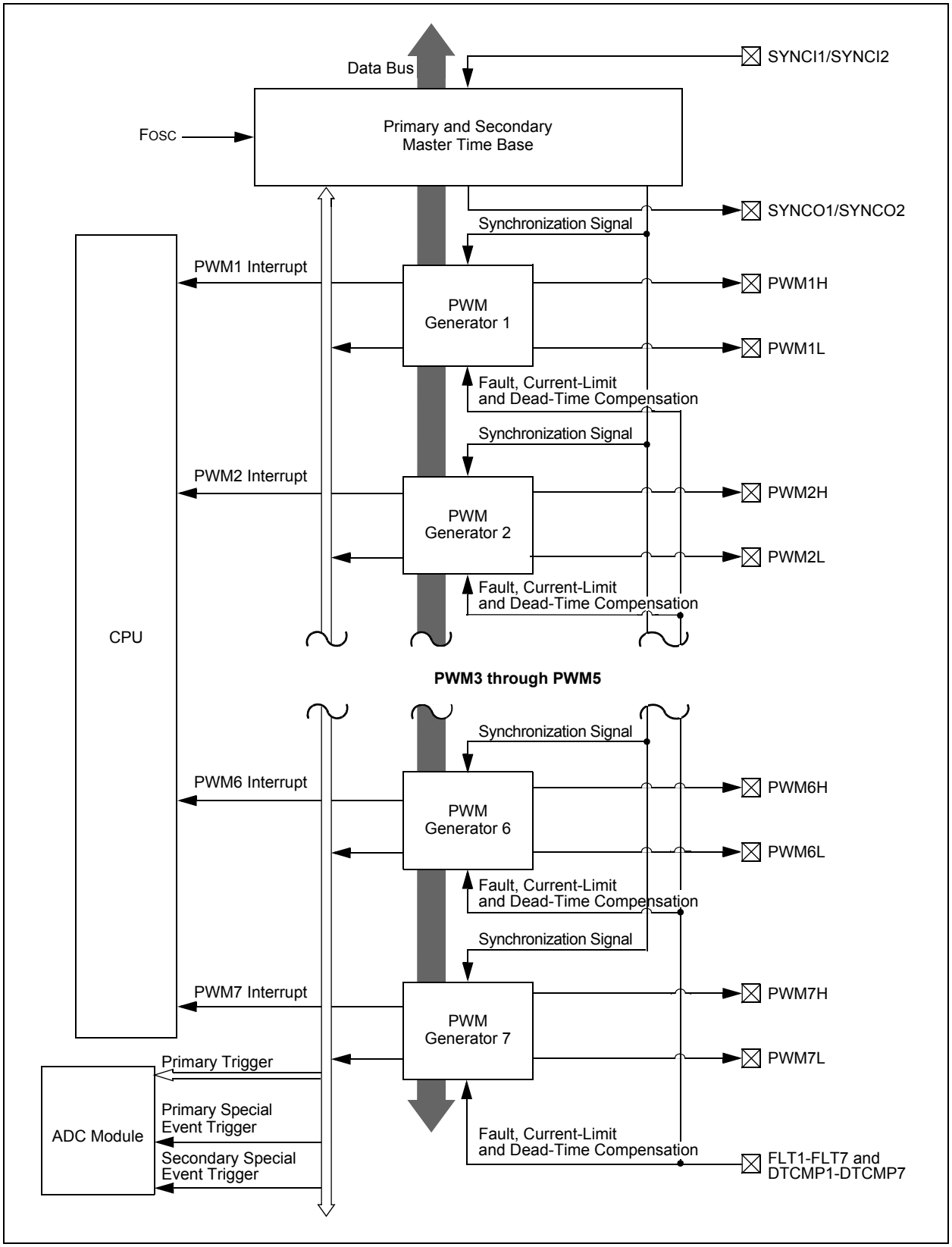
FIGURE 16-1: HIGH-SPEED PWM MODULE ARCHITECTURAL OVERVIEW



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21.2 Modes of Operation

The ECANx module can operate in one of several operation modes selected by the user. These modes include:

- Initialization mode
- Disable mode
- Normal Operation mode
- Listen Only mode
- Listen All Messages mode
- Loopback mode

Modes are requested by setting the REQOP<2:0> bits (CxCTRL1<10:8>). Entry into a mode is Acknowledged by monitoring the OPMODE<2:0> bits (CxCTRL1<7:5>). The module does not change the mode and the OPMODE bits until a change in mode is acceptable, generally during bus Idle time, which is defined as at least 11 consecutive recessive bits.

21.3 ECAN Resources

Many useful resources related to ECAN are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310

21.3.1 KEY RESOURCES

- **Section 21. "Enhanced Controller Area Network (ECAN™)"** (DS70353) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

REGISTER 21-11: CxFEN1: ECANx ACCEPTANCE FILTER ENABLE REGISTER 1

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
FLTEN15	FLTEN14	FLTEN13	FLTEN12	FLTEN11	FLTEN10	FLTEN9	FLTEN8
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
FLTEN7	FLTEN6	FLTEN5	FLTEN4	FLTEN3	FLTEN2	FLTEN1	FLTEN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **FLTENn:** Enable Filter n to Accept Messages bits
`1` = Enables Filter n
`0` = Disables Filter n

REGISTER 21-12: CxBUFPNT1: ECANx FILTER 0-3 BUFFER POINTER REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F3BP<3:0>				F2BP<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F1BP<3:0>				F0BP<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **F3BP<3:0>:** RX Buffer Mask for Filter 3 bits
`1111` = Filter hits received in RX FIFO buffer
`1110` = Filter hits received in RX Buffer 14
•
•
•
`0001` = Filter hits received in RX Buffer 1
`0000` = Filter hits received in RX Buffer 0

bit 11-8 **F2BP<3:0>:** RX Buffer Mask for Filter 2 bits (same values as bit 15-12)

bit 7-4 **F1BP<3:0>:** RX Buffer Mask for Filter 1 bits (same values as bit 15-12)

bit 3-0 **F0BP<3:0>:** RX Buffer Mask for Filter 0 bits (same values as bit 15-12)

REGISTER 21-15: CxBUFPNT4: ECANx FILTER 12-15 BUFFER POINTER REGISTER 4

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F15BP<3:0>				F14BP<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F13BP<3:0>				F12BP<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **F15BP<3:0>:** RX Buffer Mask for Filter 15 bits
`1111` = Filter hits received in RX FIFO buffer
`1110` = Filter hits received in RX Buffer 14
•
•
•
`0001` = Filter hits received in RX Buffer 1
`0000` = Filter hits received in RX Buffer 0

bit 11-8 **F14BP<3:0>:** RX Buffer Mask for Filter 14 bits (same values as bit 15-12)

bit 7-4 **F13BP<3:0>:** RX Buffer Mask for Filter 13 bits (same values as bit 15-12)

bit 3-0 **F12BP<3:0>:** RX Buffer Mask for Filter 12 bits (same values as bit 15-12)

REGISTER 23-3: AD2CON2: ADC2 CONTROL REGISTER 2 (CONTINUED)

bit 1 **BUFM:** Buffer Fill Mode Select bit

1 = Starts buffer filling the first half of the buffer on the first interrupt and the second half of the buffer on the next interrupt

0 = Always starts filling the buffer from the Start address

bit 0 **ALTS:** Alternate Input Sample Mode Select bit

1 = Uses channel input selects for Sample A on first sample and Sample B on next sample

0 = Always uses channel input selects for Sample A

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FIGURE 25-2: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM

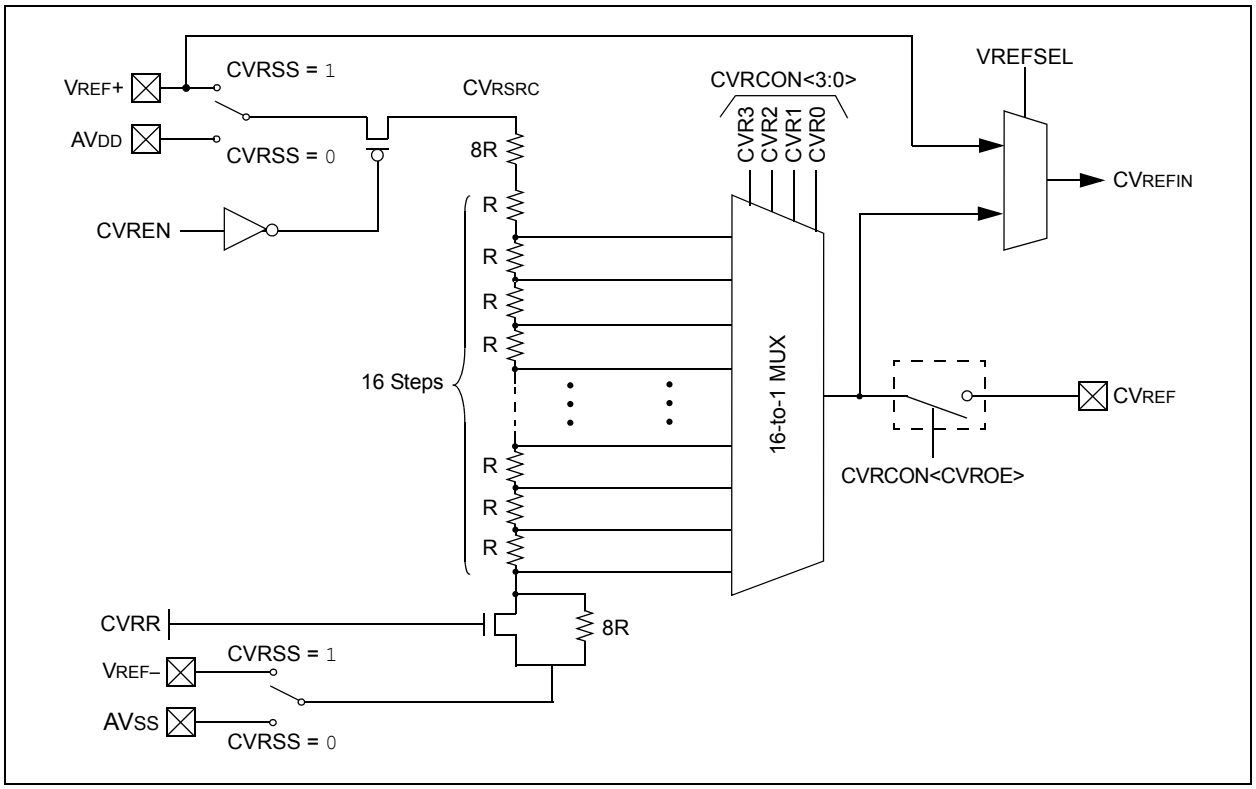
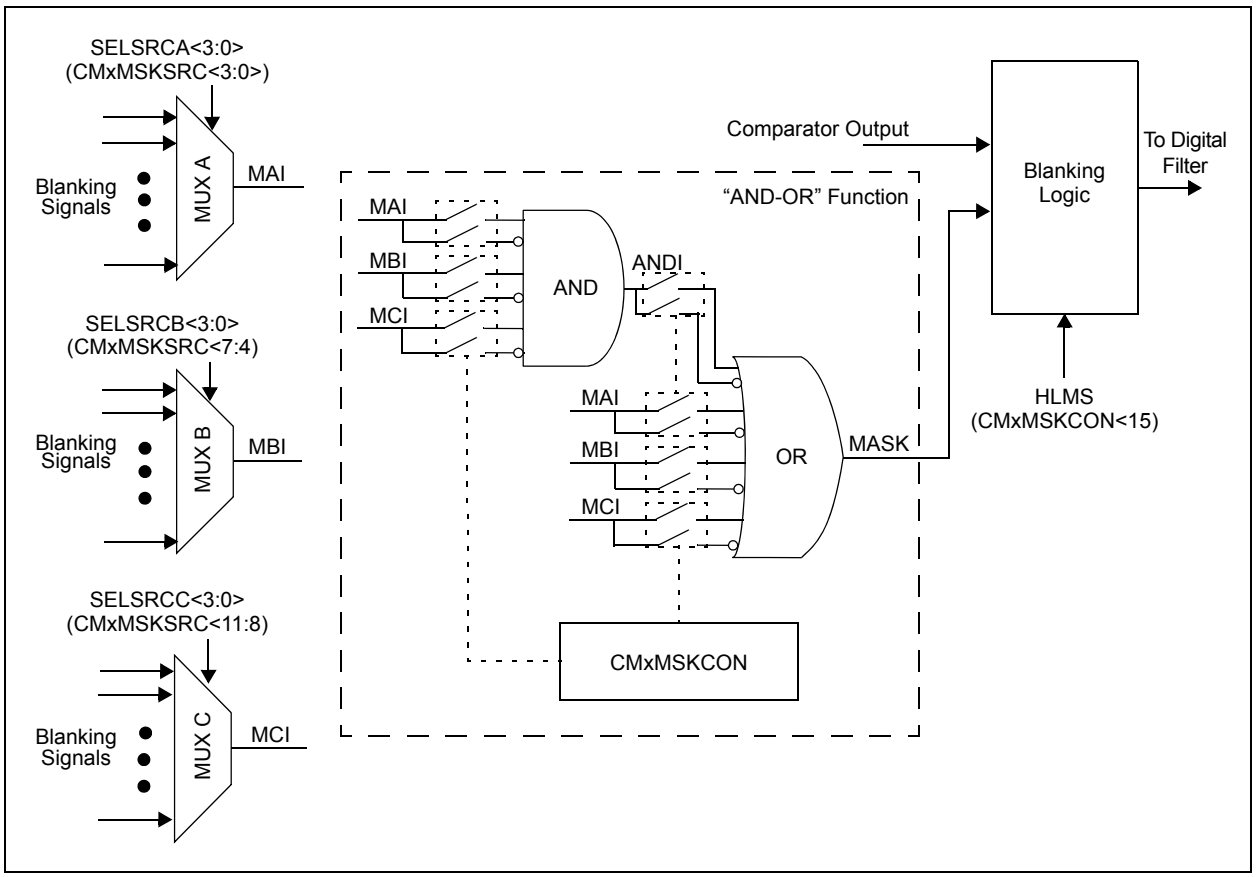


FIGURE 25-3: USER-PROGRAMMABLE BLANKING FUNCTION BLOCK DIAGRAM



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REGISTER 25-5: CMxFLTR: COMPARATOR x FILTER CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	I-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6-4 **CFSEL<2:0>:** Comparator Filter Input Clock Select bits
111 = T5CLK(1)
110 = T4CLK(2)
101 = T3CLK(1)
100 = T2CLK(2)
011 = SYNCO2(3)
010 = SYNCO1(3)
001 = FOSC(4)
000 = FP(4)

bit 3 **CFLTREN:** Comparator Filter Enable bit
1 = Digital filter is enabled
0 = Digital filter is disabled

bit 2-0 **CFDIV<2:0>:** Comparator Filter Clock Divide Select bits
111 = Clock Divide 1:128
110 = Clock Divide 1:64
101 = Clock Divide 1:32
100 = Clock Divide 1:16
011 = Clock Divide 1:8
010 = Clock Divide 1:4
001 = Clock Divide 1:2
000 = Clock Divide 1:1

Note 1: See the Type C Timer Block Diagram (Figure 13-2).
2: See the Type B Timer Block Diagram (Figure 13-1).
3: See the PWM Module Register Interconnect Diagram (Figure 16-2).
4: See the Oscillator System Diagram (Figure 9-1).

REGISTER 28-4: PMAEN: PARALLEL MASTER PORT ADDRESS ENABLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN15	PTEN14	PTEN13	PTEN12	PTEN11	PTEN10	PTEN9	PTEN8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN7	PTEN6	PTEN5	PTEN4	PTEN3	PTEN2	PTEN1	PTEN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at Reset	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **PTEN15:** PMCS2 Strobe Enable bit
1 = PMA15 functions as either PMA<15> or PMCS2
0 = PMA15 functions as port I/O

bit 14 **PTEN14:** PMCS1 Strobe Enable bit
1 = PMA14 functions as either PMA<14> or PMCS1
0 = PMA14 functions as port I/O

bit 13-2 **PTEN<13:2>:** PMP Address Port Enable bits
1 = PMA<13:2> function as PMP address lines
0 = PMA<13:2> function as port I/O

bit 1-0 **PTEN<1:0>:** PMALH/PMALL Strobe Enable bits
1 = PMA1 and PMA0 function as either PMA<1:0> or PMALH and PMALL
0 = PMA1 and PMA0 function as port I/O

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