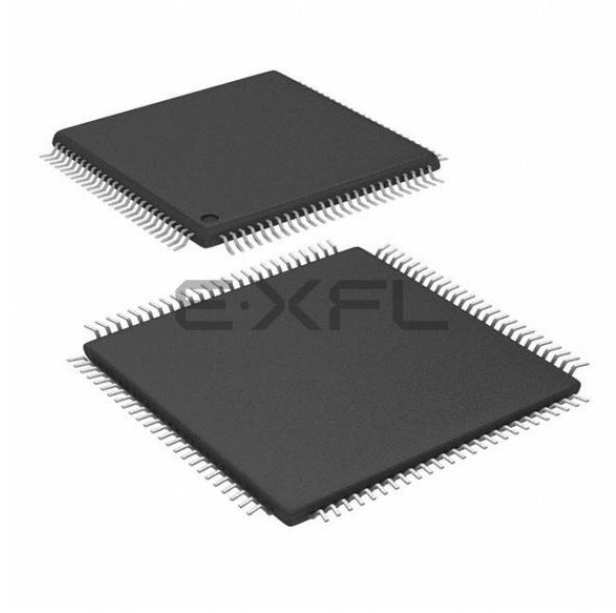
Microchip Technology - DSPIC33EP256MU810T-E/PT Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, QEI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	83
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256mu810t-e-pt

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	PPS	Description
SCL1(5)	I/O	ST	No	Synchronous serial clock input/output for I2C1.
SDA1(5)	I/O	ST	No	Synchronous serial data input/output for I2C1.
ASCL1(5)	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1.
ASDA1(5)	I/O	ST	No	Alternate synchronous serial data input/output for I2C1.
SCL2(5)	I/O	ST	No	Synchronous serial clock input/output for I2C2.
SDA2(5)	I/O	ST	No	Synchronous serial data input/output for I2C2.
ASCL2(5)	I/O	ST	No	Alternate synchronous serial clock input/output for I2C2.
ASDA2(5)	I/O	ST	No	Alternate synchronous serial data input/output for I2C2.
TMS	I	ST	No	JTAG Test mode select pin.
TCK	I	ST	No	JTAG test clock input pin.
TDI	I	ST	No	JTAG test data input pin.
TDO	O	—	No	JTAG test data output pin.
INDX1(1)	I	ST	Yes	Quadrature Encoder Index1 pulse input.
HOME1(1)	I	ST	Yes	Quadrature Encoder Home1 pulse input.
QEA1(1)	I	ST	Yes	Quadrature Encoder Phase A input in QEI1 mode. Auxiliary timer external clock input in Timer mode.
QEB1(1)	I	ST	Yes	Quadrature Encoder Phase A input in QEI1 mode. Auxiliary timer external gate input in Timer mode.
CNTCMP1(1)	O	—	Yes	Quadrature Encoder Compare Output 1.
INDX2(1)	I	ST	Yes	Quadrature Encoder Index2 pulse input.
HOME2(1)	I	ST	Yes	Quadrature Encoder Home2 pulse input.
QEA2(1)	I	ST	Yes	Quadrature Encoder Phase A input in QEI2 mode. Auxiliary timer external clock input in Timer mode.
QEB2(1)	I	ST	Yes	Quadrature Encoder Phase B input in QEI2 mode. Auxiliary timer external gate input in Timer mode.
CNTCMP2(1)	O	—	Yes	Quadrature Encoder Compare Output 2.
COFS	I/O	ST	Yes	Data Converter Interface frame synchronization pin.
CSCK	I/O	ST	Yes	Data Converter Interface serial clock input/output pin.
CSDI	I	ST	Yes	Data Converter Interface serial data input pin.
CSDO	O	—	Yes	Data Converter Interface serial data output pin.
C1RX	I	ST	Yes	ECAN1 bus receive pin.
C1TX	O	—	Yes	ECAN1 bus transmit pin.
C2RX	I	ST	Yes	ECAN2 bus receive pin.
C2TX	O	—	Yes	ECAN2 bus transmit pin.
RTCC	O	—	No	Real-Time Clock alarm output.
CVREF	O	Analog	No	Comparator voltage reference output.
C1IN1+, C1IN2-, C1IN1-, C1IN3-	I	Analog	No	Comparator 1 inputs
C1OUT	O	—	Yes	Comparator 1 output.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

Note 1: This pin is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

2: AVDD must be connected at all times.

3: These pins are input only on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices.

4: These pins are only available on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices.

5: The availability of I^2C™ interfaces varies by device. Refer to the **"Pin Diagrams"** section for availability. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

6: Analog functionality is activated by enabling the USB module and is not controlled by the ANSEL register.

3.7 CPU Control Registers

REGISTER 3-1: SR: CPU STATUS REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R -0	R/W-0
OA(1)	OB(1)	SA(1,4)	SB(1,4)	OAB(1)	SAB(1)	DA(1)	DC
bit 15							bit 8

R/W-0(2,3)	R/W-0(2,3)	R/W-0(2,3)	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL<2:0>			RA	N	OV	Z	C
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	W = Writable bit	C = Clearable bit	
-n = Value at POR	'1'= Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **OA:** Accumulator A Overflow Status bit(1)
1 = Accumulator A has overflowed
0 = Accumulator A has not overflowed

bit 14 **OB:** Accumulator B Overflow Status bit(1)
1 = Accumulator B has overflowed
0 = Accumulator B has not overflowed

bit 13 **SA:** Accumulator A Saturation 'Sticky' Status bit(1,4)
1 = Accumulator A is saturated or has been saturated at some time
0 = Accumulator A is not saturated

bit 12 **SB:** Accumulator B Saturation 'Sticky' Status bit(1,4)
1 = Accumulator B is saturated or has been saturated at some time
0 = Accumulator B is not saturated

bit 11 **OAB:** OA || OB Combined Accumulator Overflow Status bit(1)
1 = Accumulators A or B have overflowed
0 = Neither Accumulators A or B have overflowed

bit 10 **SAB:** SA || SB Combined Accumulator 'Sticky' Status bit(1)
1 = Accumulators A or B are saturated or have been saturated at some time
0 = Neither Accumulator A or B are saturated

bit 9 **DA:** DO Loop Active bit(1)
1 = DO loop in progress
0 = DO loop not in progress

bit 8 **DC:** MCU ALU Half Carry/$\overline{\text{Borrow}}$ bit
1 = A carry-out from the 4th low order bit (for byte-sized data) or 8th low order bit (for word-sized data) of the result occurred
0 = No carry-out from the 4th low order bit (for byte-sized data) or 8th low order bit (for word-sized data) of the result occurred

Note 1: This bit is available on dsPIC33EPXXX(GP/MC/MU)806/810/814 devices only.

2: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1.

3: The IPL<2:0> bits are read-only when NSTDIS = 1 (INTCON1<15>).

4: A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.

TABLE 4-58: PORTC REGISTER MAP FOR dsPIC33EPXXX(GP/MC/MU)806 AND PIC24EPXXXGP806 DEVICES ONLY

File Name	Addr,	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E20	TRISC15	TRISC14	TRISC13	TRISC12	—	—	—	—	—	—	—	—	—	—	—	—	F000
PORTC	0E22	RC15	RC14	RC13	RC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
LATC	0E24	LATC15	LATC14	LATC13	LATC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
ODCC	0E26	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
CNENC	0E28	CNIEC15	CNIEC14	CNIEC13	CNIEC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
CNPUC	0E2A	CNPUC15	CNPUC14	CNPUC13	CNPUC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
CNPDC	0E2C	CNPDC15	CNPDC14	CNPDC13	CNPDC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
ANSELC	0E2E	—	ANSC14	ANSC13	—	—	—	—	—	—	—	—	—	—	—	—	—	6000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-59: PORTD REGISTER MAP FOR dsPIC33EPXXXMU810/814 AND PIC24EPXXXGU810/814 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISD	0E30	TRISD15	TRISD14	TRISD13	TRISD12	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	FFFF
PORTD	0E32	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
LATD	0E34	LATD15	LATD14	LATD13	LATD12	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
ODCD	0E36	ODCD15	ODCD14	ODCD13	ODCD12	ODCD11	ODCD10	ODCD9	ODCD8	—	—	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000
CNEND	0E38	CNIED15	CNIED14	CNIED13	CNIED12	CNIED11	CNIED10	CNIED9	CNIED8	CNIED7	CNIED6	CNIED5	CNIED4	CNIED3	CNIED2	CNIED1	CNIED0	0000
CNPUD	0E3A	CNPUD15	CNPUD14	CNPUD13	CNPUD12	CNPUD11	CNPUD10	CNPUD9	CNPUD8	CNPUD7	CNPUD6	CNPUD5	CNPUD4	CNPUD3	CNPUD2	CNPUD1	CNPUD0	0000
CNPDD	0E3C	CNPDD15	CNPDD14	CNPDD13	CNPDD12	CNPDD11	CNPDD10	CNPDD9	CNPDD8	CNPDD7	CNPDD6	CNPDD5	CNPDD4	CNPDD3	CNPDD2	CNPDD1	CNPDD0	0000
ANSELD	0E3E	—	—	—	—	—	—	—	—	ANSD7	ANSD6	—	—	—	—	—	—	00C0

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-60: PORTD REGISTER MAP FOR dsPIC33EPXXX(GP/MC/MU)806 AND PIC24EPXXXGP806 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISD	0E30	—	—	—	—	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	0FFF
PORTD	0E32	—	—	—	—	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
LATD	0E34	—	—	—	—	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
ODCD	0E36	—	—	—	—	ODCD11	ODCD10	ODCD9	ODCD8	—	—	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000
CNEND	0E38	—	—	—	—	CNIED11	CNIED10	CNIED9	CNIED8	CNIED7	CNIED6	CNIED5	CNIED4	CNIED3	CNIED2	CNIED1	CNIED0	0000
CNPUD	0E3A	—	—	—	—	CNPUD11	CNPUD10	CNPUD9	CNPUD8	CNPUD7	CNPUD6	CNPUD5	CNPUD4	CNPUD3	CNPUD2	CNPUD1	CNPUD0	0000
CNPDD	0E3C	—	—	—	—	CNPDD11	CNPDD10	CNPDD9	CNPDD8	CNPDD7	CNPDD6	CNPDD5	CNPDD4	CNPDD3	CNPDD2	CNPDD1	CNPDD0	0000
ANSELD	0E3E	—	—	—	—	—	—	—	—	ANSD7	ANSD6	—	—	—	—	—	—	00C0

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

NOTES:

REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1 (CONTINUED)

bit 4 **MATHERR:** Math Error Status bit
1 = Math error trap has occurred
0 = Math error trap has not occurred

bit 3 **ADDRERR:** Address Error Trap Status bit
1 = Address error trap has occurred
0 = Address error trap has not occurred

bit 2 **STKERR:** Stack Error Trap Status bit
1 = Stack error trap has occurred
0 = Stack error trap has not occurred

bit 1 **OSCFAIL:** Oscillator Failure Trap Status bit
1 = Oscillator failure trap has occurred
0 = Oscillator failure trap has not occurred

bit 0 **Unimplemented:** Read as '0'

Note 1: This bit is available on dsPIC33EPXXX(GP/MC/MU)806/810/814 devices only.

11.5 I/O Helpful Tips

1. In some cases, certain pins, as defined in Table 32-9 in **Section 32.0 "Electrical Characteristics"** under "Injection Current", have internal protection diodes to VDD and VSS; the term "Injection Current" is also referred to as "Clamp Current". On designated pins, with sufficient external current-limiting precautions by the user, I/O pin input voltages are allowed to be greater or less than the data sheet absolute maximum ratings with respect to the VSS and VDD supplies. Note that when the user application forward biases either of the high or low side internal input clamp diodes, that the resulting current being injected into the device that is clamped internally by the VDD and VSS power rails, may affect the ADC accuracy by four to six counts.
2. I/O pins that are shared with any analog input pin, (i.e., ANx, see Table 1-1 in **Section 1.0 "Device Overview"**), are always analog pins by default after any Reset. Consequently, configuring a pin as an analog input pin, automatically disables the digital input pin buffer and any attempt to read the digital input level by reading PORTx or LATx will always return a '0', regardless of the digital logic level on the pin. To use a pin as a digital I/O pin on a shared analog pin (see Table 1-1 in **Section 1.0 "Device Overview"**), the user application needs to configure the Analog Pin Configuration registers in the I/O ports module (i.e., ANSELx) by setting the appropriate bit that corresponds to that I/O port pin to a '0'.

Note:	Although it is not possible to use a digital input pin when its analog function is enabled, it is possible to use the digital I/O output function, TRISx = 0x0, while the analog function is also enabled. However, this is not recommended, particularly if the analog input is connected to an external analog voltage source, which would create signal contention between the analog signal and the output pin driver.

3. Most I/O pins have multiple functions. Referring to the device pin diagrams in the data sheet, the priorities of the functions allocated to any pins are indicated by reading the pin name from left to right. The left most function name takes precedence over any function to its right in the naming convention. For example: AN16/T2CK/T7CK/RC1; this indicates that AN16 is the highest priority in this example and will supersede all other functions to its right in the list. Those other functions to its right, even if enabled, would not work as long as any other function to its left was enabled. This rule applies to all of the functions listed for a given pin. Dedicated peripheral functions are always higher priority than remappable functions. I/O pins are always the lowest priority.
4. Each pin has an internal weak pull-up resistor and pull-down resistor that can be configured using the CNPUx and CNPDx registers, respectively. These resistors eliminate the need for external resistors in certain applications. The internal pull-up is up to ~(VDD-0.8), not VDD. This value is still above the minimum VIH of CMOS and TTL devices.
5. When driving LEDs directly, the I/O pin can source or sink more current than what is specified in the VOH/IOH and VOL/IOL DC characteristic specification. The respective IOH and IOL current rating only applies to maintaining the corresponding output at or above the VOH and at or below the VOL levels. However, for LEDs, unlike digital inputs of an externally connected device, they are not governed by the same minimum VIH/VIL levels. An I/O pin output can safely sink or source any current less than that listed in the absolute maximum rating section of the data sheet. For example:

   VOH = 2.4v @ IOH = -8 mA and VDD = 3.3V

   The maximum output current sourced by any 8 mA I/O pin = 12 mA.

   LED source current < 12 mA is technically permitted. Refer to the VOH/IOH graphs in **Section 32.0 "Electrical Characteristics"** for additional information.
6. The Peripheral Pin Select (PPS) pin mapping rules are as follows:
   a) Only one "output" function can be active on a given pin at any time regardless if it is a dedicated or remappable function (one pin, one output).
   b) It is possible to assign a "remappable output" function to multiple pins and externally short or tie them together for increased current drive.
   c) If any "dedicated output" function is enabled on a pin, it will take precedence over any remappable "output" function.
   d) If any "dedicated digital" (input or output) function is enabled on a pin, any number of "input" remappable functions can be mapped to the same pin.
   e) If any "dedicated analog" function(s) are enabled on a given pin, "digital input(s)" of any kind will all be disabled, although a single "digital output", at the user's cautionary discretion, can be enabled and active as long as there is no signal contention with an external analog input signal. For example, it is possible for the ADC to convert the digital output logic level, or to toggle a digital output on a comparator or ADC input, provided there is no external analog input, such as for a built-in self test.
   f) Any number of "input" remappable functions can be mapped to the same pin(s) at the same time, including any pin with a single output from either a dedicated or remappable "output".

REGISTER 11-18: RPINR17: PERIPHERAL PIN SELECT INPUT REGISTER 17 (dsPIC33EPXXXMU806/810/814 DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	HOME2R<6:0>(1)						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	INDX2R<6:0>(1)						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **HOME2R<6:0>:** Assign QEI2 HOME2 (HOME2) to the Corresponding RPn/RPIn Pin bits(1) (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **INDX2R<6:0>:** Assign QEI2 INDEX2 (INDX2) to the Corresponding RPn/RPIn Pin bits(1) (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

Note 1: These bits are available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

REGISTER 11-20: RPINR19: PERIPHERAL PIN SELECT INPUT REGISTER 19

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	U2CTSR<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	U2RXR<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **U2CTSR<6:0>:** Assign UART2 Clear-to-Send ($\overline{\text{U2CTS}}$) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **U2RXR<6:0>:** Assign UART2 Receive (U2RX) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

REGISTER 17-2: QEIxIOC: QEIx I/O CONTROL REGISTER (CONTINUED)

bit 2 **INDEX:** Status of INDXx Input Pin After Polarity Control bit
1 = Pin is at logic '1'
0 = Pin is at logic '0'

bit 1 **QEB:** Status of QEBx Input Pin After Polarity Control And SWPAB Pin Swapping bit
1 = Pin is at logic '1'
0 = Pin is at logic '0'

bit 0 **QEA:** Status of QEAx Input Pin After Polarity Control And SWPAB Pin Swapping bit
1 = Pin is at logic '1'
0 = Pin is at logic '0'

20.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 17. "UART"** (DS70582) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 family of devices contains four UART modules.

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 device family. The UART is a full-duplex, asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins, and also includes an IrDA® encoder and decoder.

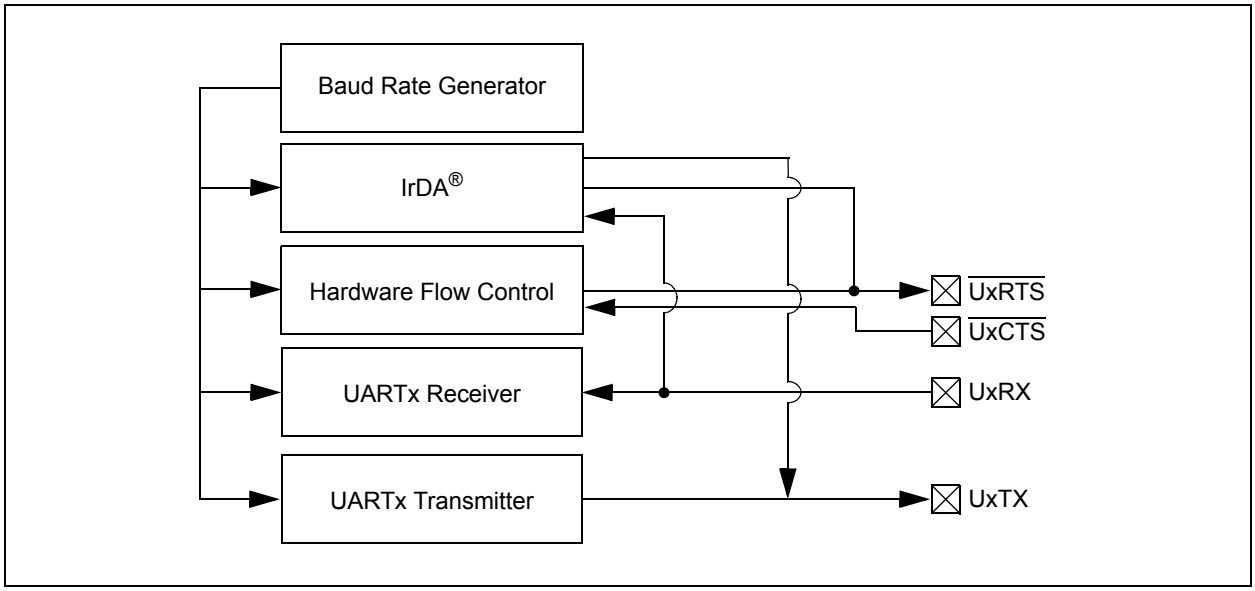
The primary features of the UARTx module are:

- Full-Duplex, 8 or 9-Bit Data Transmission through the UxTX and UxRX Pins
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop bits
- Hardware Flow Control Option with $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ Pins
- Fully Integrated Baud Rate Generator with 16-Bit Prescaler
- Baud Rates Ranging from 4.375 Mbps to 67 bps at 16x mode at 70 MIPS
- Baud Rates Ranging from 17.5 Mbps to 267 bps at 4x mode at 70 MIPS
- 4-Deep First-In First-Out (FIFO) Transmit Data Buffer
- 4-Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-bit mode with Address Detect (9th bit = 1)
- Transmit and Receive Interrupts
- A Separate Interrupt for All UARTx Error Conditions
- Loopback mode for Diagnostic Support
- Support for Sync and Break Characters
- Support for Automatic Baud Rate Detection
- IrDA® Encoder and Decoder Logic
- 16x Baud Clock Output for IrDA Support

A simplified block diagram of the UARTx module is shown in Figure 20-1. The UARTx module consists of these key hardware elements:

- Baud Rate Generator
- Asynchronous Transmitter
- Asynchronous Receiver

FIGURE 20-1: UARTx SIMPLIFIED BLOCK DIAGRAM



REGISTER 21-6: CxINTF: ECANx INTERRUPT FLAG REGISTER

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	TXBO	TXBP	RXBP	TXWAR	RXWAR	EWARN
bit 15							bit 8

R/C-0	R/C-0	R/C-0	U-0	R/C-0	R/C-0	R/C-0	R/C-0
IVRIF	WAKIF	ERRIF	—	FIFOIF	RBOVIF	RBIF	TBIF
bit 7							bit 0

Legend:	C = Writable bit, but only ‘0’ can be written to clear the bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13 **TXBO:** Transmitter in Error State Bus Off bit
1 = Transmitter is in Bus Off state
0 = Transmitter is not in Bus Off state

bit 12 **TXBP:** Transmitter in Error State Bus Passive bit
1 = Transmitter is in Bus Passive state
0 = Transmitter is not in Bus Passive state

bit 11 **RXBP:** Receiver in Error State Bus Passive bit
1 = Receiver is in Bus Passive state
0 = Receiver is not in Bus Passive state

bit 10 **TXWAR:** Transmitter in Error State Warning bit
1 = Transmitter is in Error Warning state
0 = Transmitter is not in Error Warning state

bit 9 **RXWAR:** Receiver in Error State Warning bit
1 = Receiver is in Error Warning state
0 = Receiver is not in Error Warning state

bit 8 **EWARN:** Transmitter or Receiver in Error State Warning bit
1 = Transmitter or Receiver is in Error State Warning state
0 = Transmitter or Receiver is not in Error State Warning state

bit 7 **IVRIF:** Invalid Message Interrupt Flag bit
1 = Interrupt Request has occurred
0 = Interrupt Request has not occurred

bit 6 **WAKIF:** Bus Wake-up Activity Interrupt Flag bit
1 = Interrupt Request has occurred
0 = Interrupt Request has not occurred

bit 5 **ERRIF:** Error Interrupt Flag bit (multiple sources in CxINTF<13:8> register)
1 = Interrupt Request has occurred
0 = Interrupt Request has not occurred

bit 4 **Unimplemented:** Read as ‘0’

bit 3 **FIFOIF:** FIFO Almost Full Interrupt Flag bit
1 = Interrupt Request has occurred
0 = Interrupt Request has not occurred

bit 2 **RBOVIF:** RX Buffer Overflow Interrupt Flag bit
1 = Interrupt Request has occurred
0 = Interrupt Request has not occurred

bit 1 **RBIF:** RX Buffer Interrupt Flag bit
1 = Interrupt Request has occurred
0 = Interrupt Request has not occurred

bit 0 **TBIF:** TX Buffer Interrupt Flag bit
1 = Interrupt Request has occurred
0 = Interrupt Request has not occurred

25.2 Comparator Control Registers

REGISTER 25-1: CMSTAT: COMPARATOR STATUS REGISTER

R/W-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
CMSIDL	—	—	—	—	C3EVT	C2EVT	C1EVT
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
—	—	—	—	—	C3OUT	C2OUT	C1OUT
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CMSIDL:** Comparator Stop in Idle Mode bit
1 = Discontinues operation of all comparators when device enters Idle mode
0 = Continues operation of all comparators in Idle mode

bit 14-11 **Unimplemented:** Read as '0'

bit 10 **C3EVT:** Comparator 3 Event Status bit
1 = Comparator event occurred
0 = Comparator event did not occur

bit 9 **C2EVT:** Comparator 2 Event Status bit
1 = Comparator event occurred
0 = Comparator event did not occur

bit 8 **C1EVT:** Comparator 1 Event Status bit
1 = Comparator event occurred
0 = Comparator event did not occur

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **C3OUT:** Comparator 3 Output Status bit
When CPOL = 0:
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When CPOL = 1:
1 = VIN+ < VIN-
0 = VIN+ > VIN-

bit 1 **C2OUT:** Comparator 2 Output Status bit
When CPOL = 0:
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When CPOL = 1:
1 = VIN+ < VIN-
0 = VIN+ > VIN-

bit 0 **C1OUT:** Comparator 1 Output Status bit
When CPOL = 0:
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When CPOL = 1:
1 = VIN+ < VIN-
0 = VIN+ > VIN-

REGISTER 26-9: ALRMVAL (WHEN ALRMPTR<1:0> = 01): ALARM WEEKDAY AND HOURS VALUE REGISTER(1)

U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	—	—	—	—	WDAY2	WDAY1	WDAY0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	HRTEN<1:0>		HRONE<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **WDAY<2:0>:** Binary Coded Decimal Value of Weekday Digit bits
Contains a value from 0 to 6.

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **HRTEN<1:0>:** Binary Coded Decimal Value of Hour's Tens Digit bits
Contains a value from 0 to 2.

bit 3-0 **HRONE<3:0>:** Binary Coded Decimal Value of Hour's Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

NOTES:

TABLE 29-2: CONFIGURATION BITS DESCRIPTION

Bit Field	Register	RTSP Effect	Description
GSSK<1:0>	FGS	Immediate	General Segment Key bits These bits must be set to '00' if GWRP = 1 and GSS = 1. These bits must be set to '11' for any other value of the GWRP and GSS bits. Any mismatch between either the GWRP or GSS bits, and the GSSK bits (as described above), will result in code protection becoming enabled for the General Segment. A Flash bulk erase will be required to unlock the device.
GSS	FGS	Immediate	General Segment Code-Protect bit 1 = User program memory is not code-protected 0 = User program memory is code-protected
GWRP	FGS	Immediate	General Segment Write-Protect bit 1 = User program memory is not write-protected 0 = User program memory is write-protected
IESO	FOSCSEL	Immediate	Two-Speed Oscillator Start-up Enable bit 1 = Start-up device with FRC, then automatically switch to the user-selected oscillator source when ready 0 = Start-up device with user-selected oscillator source
FNOSC<2:0>	FOSCSEL	If clock switch is enabled, the RTSP effect is on any device Reset; otherwise, immediate	Initial Oscillator Source Selection bits 111 = Internal Fast RC (FRC) Oscillator with Postscaler 110 = Internal Fast RC (FRC) Oscillator with Divide-by-16 101 = LPRC Oscillator 100 = Secondary (LP) Oscillator 011 = Primary (XT, HS, EC) Oscillator with PLL 010 = Primary (XT, HS, EC) Oscillator 001 = Internal Fast RC (FRC) Oscillator with PLL 000 = FRC Oscillator
FCKSM<1:0>	FOSC	Immediate	Clock Switching Mode bits 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
IOL1WAY	FOSC	Immediate	Peripheral Pin Select Configuration bit 1 = Allows only one reconfiguration 0 = Allows multiple reconfigurations
OSCIOFNC	FOSC	Immediate	OSC2 Pin Function bit (except in XT and HS modes) 1 = OSC2 is the clock output 0 = OSC2 is the general purpose digital I/O pin
POSCMD<1:0>	FOSC	Immediate	Primary Oscillator Mode Select bits 11 = Primary Oscillator is disabled 10 = HS Crystal Oscillator mode 01 = XT Crystal Oscillator mode 00 = EC (External Clock) mode
FWDTEN	FWDT	Immediate	Watchdog Timer Enable bit 1 = Watchdog Timer is always enabled (LPRC Oscillator cannot be disabled. Clearing the SWDTEN bit in the RCON register has no effect.) 0 = Watchdog Timer is enabled/disabled by user software (LPRC can be disabled by clearing the SWDTEN bit in the RCON register.)

Note 1: BOR should always be enabled for proper operation (BOREN = 1).

2: This register can only be modified when code protection and write protection are disabled for both the General and Auxiliary Segments (APL = 1, AWRP = 1, APLK = 0, GSS = 1, GWRP = 1 and GSSK = 0).

32.1 DC Characteristics

TABLE 32-1: OPERATING MIPS VS. VOLTAGE

Characteristic	VDD Range (in Volts)	Temp Range (in °C)	Maximum MIPS
			dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814
—	2.95V-3.6V(1)	-40°C to +85°C	70
—	2.95V-3.6V(1)	-40°C to +125°C	60

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.

TABLE 32-2: THERMAL OPERATING CONDITIONS

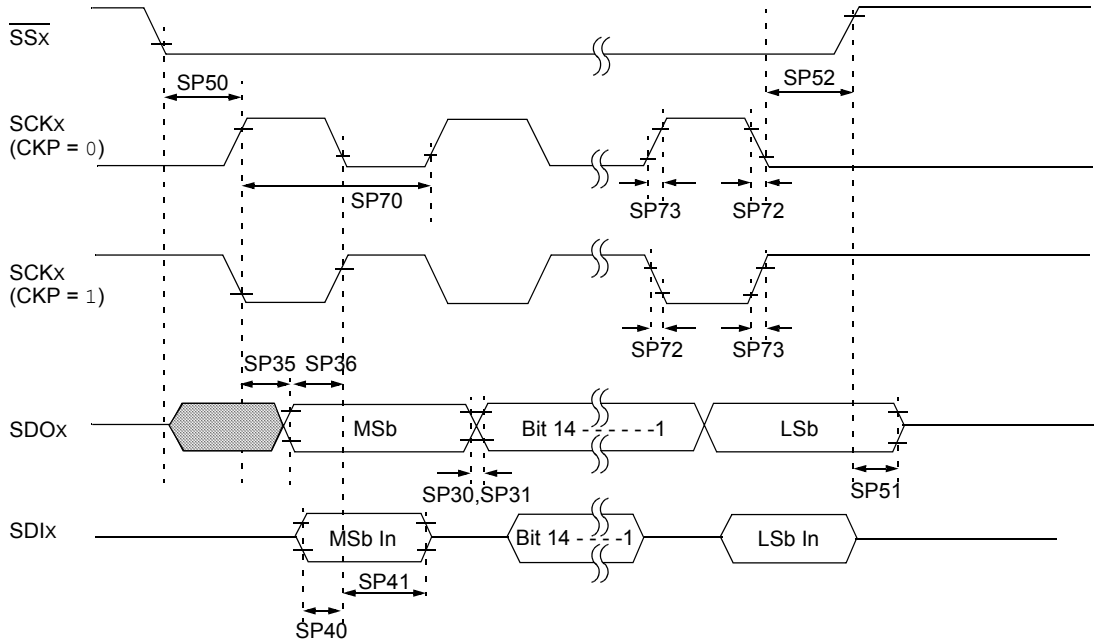
Rating	Symbol	Min.	Typ.	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
Extended Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+140	°C
Operating Ambient Temperature Range	TA	-40	—	+125	°C
Power Dissipation: Internal chip power dissipation: PINT = VDD x (IDD – Σ IOH) I/O Pin Power Dissipation: I/O = Σ ({VDD – VOH} x IOH) + Σ (VOL x IOL)	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θJA			W

TABLE 32-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Typ.	Max.	Unit	Notes
Package Thermal Resistance, 64-pin QFN (9x9 mm)	θJA	28	—	°C/W	1
Package Thermal Resistance, 64-pin TQFP (10x10 mm)	θJA	47	—	°C/W	1
Package Thermal Resistance, 100-pin TQFP (12x12 mm)	θJA	43	—	°C/W	1
Package Thermal Resistance, 100-pin TQFP (14x14 mm)	θJA	43	—	°C/W	1
Package Thermal Resistance, 121-pin TFBGA (10x10 mm)	θJA	40	—	°C/W	1
Package Thermal Resistance, 144-pin LQFP (20x20 mm)	θJA	33	—	°C/W	1
Package Thermal Resistance, 144-pin TQFP (16x16 mm)	θJA	33	—	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θJA) numbers are achieved by package simulations.

FIGURE 32-30: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 32-1 for load conditions.

TABLE 32-55: ADC MODULE SPECIFICATIONS (12-BIT MODE)

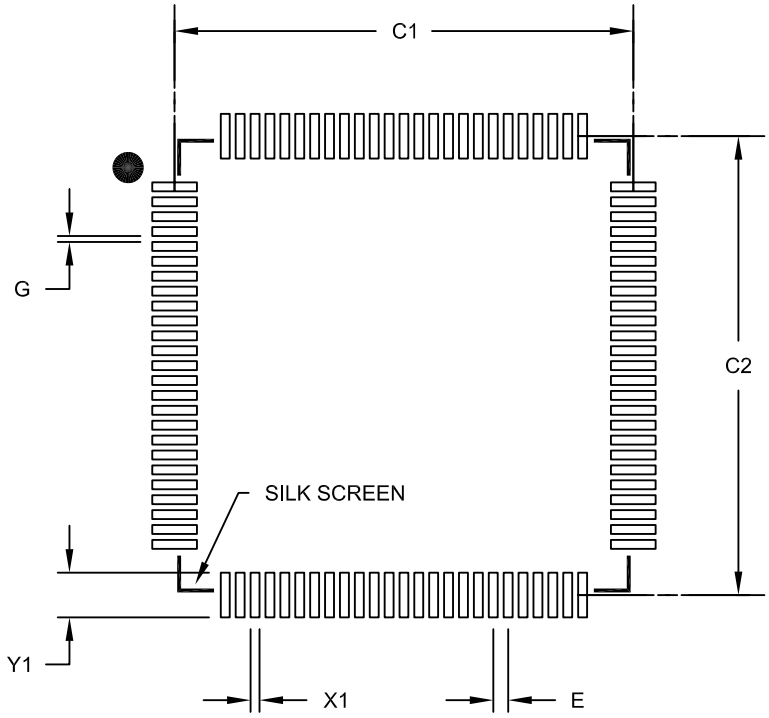
AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (see Note 1) (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
ADC Accuracy (12-Bit Mode) – Measurements with External VREF+/VREF-							
AD20a	Nr	Resolution	12 Data Bits			bits	
AD21a	INL	Integral Nonlinearity	-2	—	+2	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
AD22a	DNL	Differential Nonlinearity	>-1	—	<1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
AD23a	GERR	Gain Error	1.25	1.5	3	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
AD24a	EOFF	Offset Error	1.25	1.52	2	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
AD25a	—	Monotonicity	—	—	—	—	Guaranteed(2)
ADC Accuracy (12-Bit Mode) – Measurements with Internal VREF+/VREF-							
AD20a	Nr	Resolution	12 data bits			bits	
AD21a	INL	Integral Nonlinearity	-2	—	+2	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD22a	DNL	Differential Nonlinearity	>-1	—	<1	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD23a	GERR	Gain Error	2	3	7	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD24a	EOFF	Offset Error	2	3	5	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD25a	—	Monotonicity	—	—	—	—	Guaranteed(2)
Dynamic Performance (12-Bit Mode)							
AD30a	THD	Total Harmonic Distortion	—	—	-75	dB	
AD31a	SINAD	Signal to Noise and Distortion	68.5	69.5	—	dB	
AD32a	SFDR	Spurious Free Dynamic Range	80	—	—	dB	
AD33a	FNYQ	Input Signal Bandwidth	—	—	250	kHz	
AD34a	ENOB	Effective Number of Bits	11.09	11.3	—	bits	

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.

2: The Analog-to-Digital conversion result never decreases with an increase in input voltage and has no missing codes.

100-Lead Plastic Thin Quad Flatpack (PF) - 14x14x1 mm Body 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		15.40	
Contact Pad Spacing	C2		15.40	
Contact Pad Width (X100)	X1			0.30
Contact Pad Length (X100)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2110B

Revision C (May 2011)

This revision includes minor typographical and formatting changes throughout the data sheet text.

These global changes were implemented:

- All instances of VDDCORE have been removed.
- References to remappable pins have been updated to clarify output-only pins (RPn) versus input/output pins (RPIn).
- The minimum VDD value was changed from 2.7V to 3.0V to adhere to the current BOR specification.

The major changes are referenced by their respective section in Table A-2.

TABLE A-2: MAJOR SECTION UPDATES

Section Name	Update Description
High-Performance, 16-bit Digital Signal Controllers and Microcontrollers	Removed the shading for D+/RG2 and D-/RG3 pin designations in all pin diagrams, as these pins are not 5V tolerant. References to remappable pins have been updated to clarify input/output pins (RPn) and input-only pins (RPIn).
Section 2.0 "Guidelines for Getting Started with 16-bit Digital Signal Controllers and Microcontrollers"	Add information on the VUSB pin in **Section 2.1 "Basic Connection Requirements"**. Updated the title of Section 2.3 to **Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)"** and modified the first paragraph.
Section 3.0 "CPU"	Added Note 2 to the Programmer's Model Register Descriptions (see Table 3-1).
Section 4.0 "Memory Organization"	Added the CANCKS bit (CxCTRL1<11>) to the ECAN1 and ECAN 2 Register Maps (see Table 4-26 and Table 4-29). Added the SBOREN bit (RCON<13>) to the System Control Register Map (see Table 4-43). Added Note 1 to the PORTG Register maps (see Table 4-60 and Table 4-61). Updated the Page Description for DSRPAG = 0x1FF and DSRPAG = 0x200 in Table 4-66. Updated the second paragraph of **Section 4.2.9 "EDS Arbitration and Bus Master Priority"**. Updated the last note box in **Section 4.2.10 "Software Stack"**.
Section 5.0 "Flash Program Memory"	Updated the equation formatting in **Section 5.3 "Programming Operations"**. Added the Non-Volatile Memory Upper Address (NVMADRU) and Non-Volatile Memory Address (NVMADR) registers (see Register 5-2 and Register 5-3).
Section 6.0 "Resets"	Added Security Reset to the Reset System Block Diagram (see Figure 6-1). Added the SBOREN bit (RCON<13>) and Notes 3 and 4 to the Reset Control register (see Register 6-1).
Section 11.0 "I/O Ports"	References to remappable pins have been updated to clarify input/output pins (RPn) and input-only pins (RPIn). Added the new column, Input/Output, to Input Pin Selection for Selectable Input Sources (see Table 11-2).
Section 17.0 "Quadrature Encoder Interface (QEI) Module (dsPIC33EPXXXMU806/810/814 Devices Only)"	Updated the definition for the INTHLD<31:0> bits (see Register 17-19 and Register 17-20).