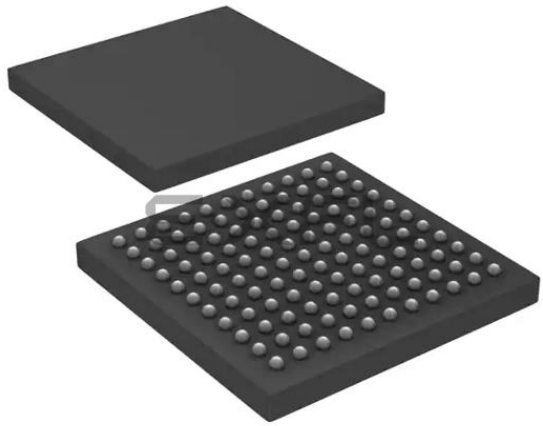
Microchip Technology - DSPIC33EP256MU810T-I/BG Datasheet



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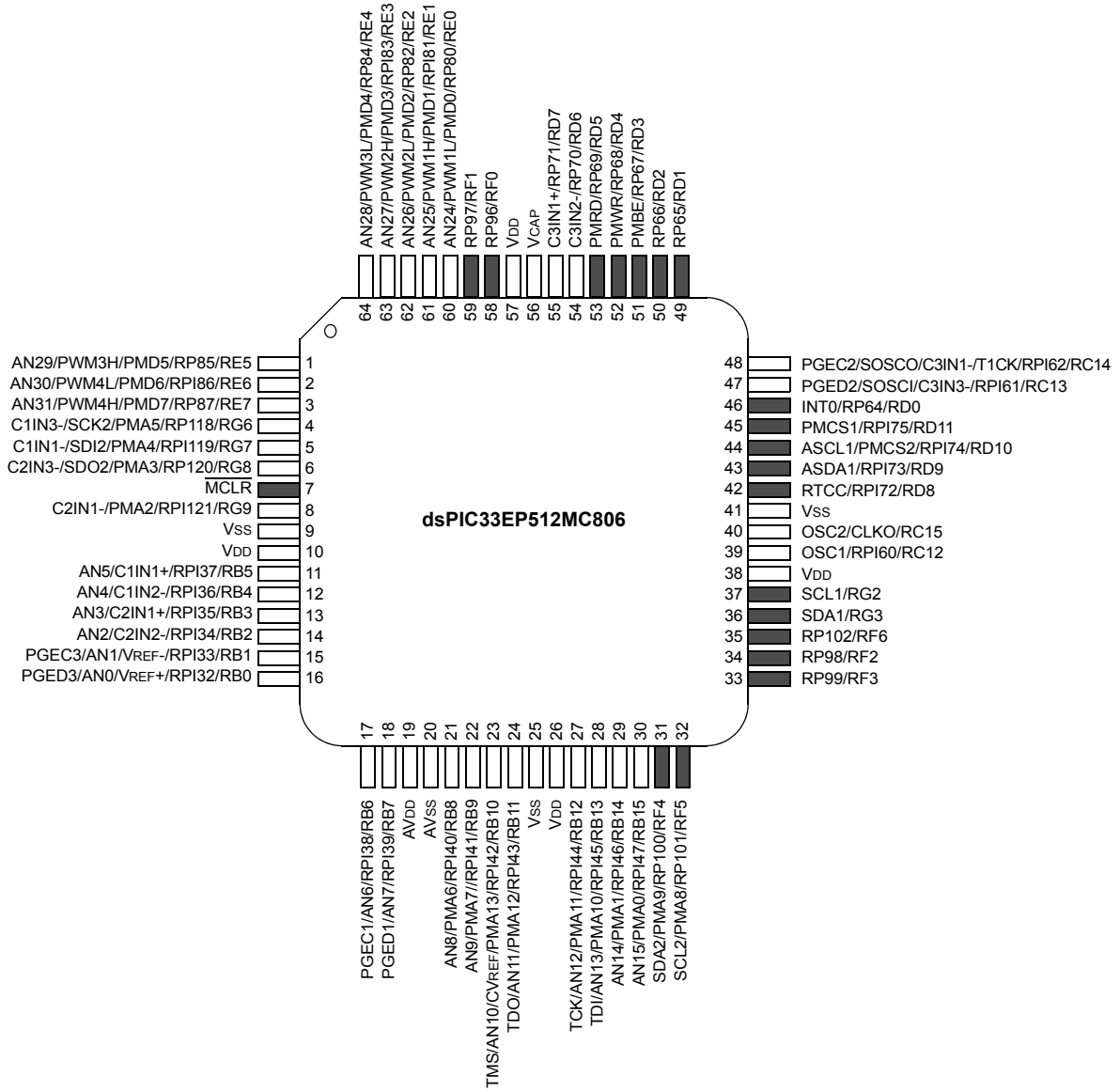
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, QEI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	83
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256mu810t-i-bg

Pin Diagrams (Continued)

64-Pin TQFP

■ = Pins are up to 5V tolerant



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

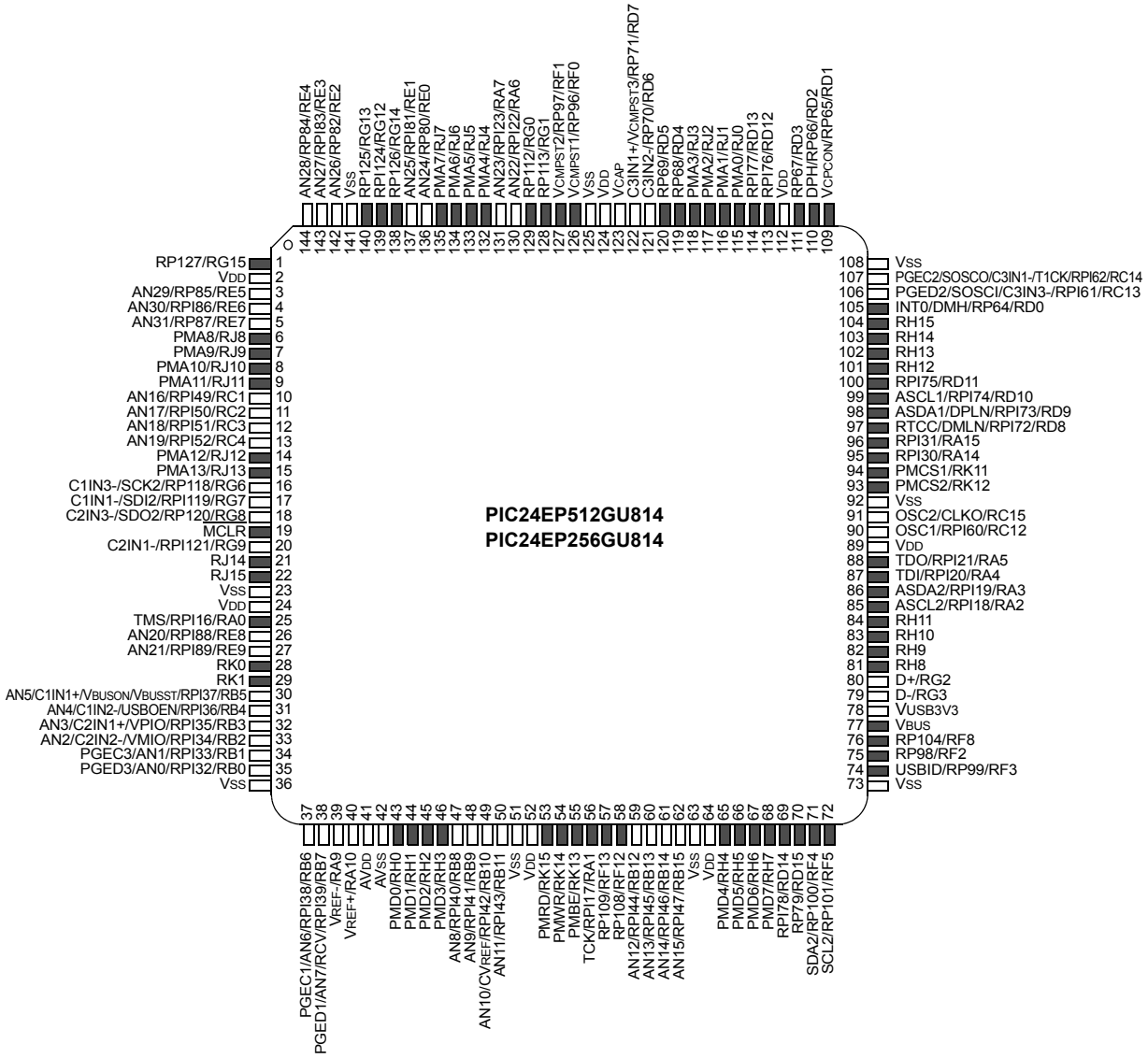
2: Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The availability of I^2C™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

Pin Diagrams (Continued)

144-Pin TQFP, 144-pin LQFP

■ = Pins are up to 5V tolerant

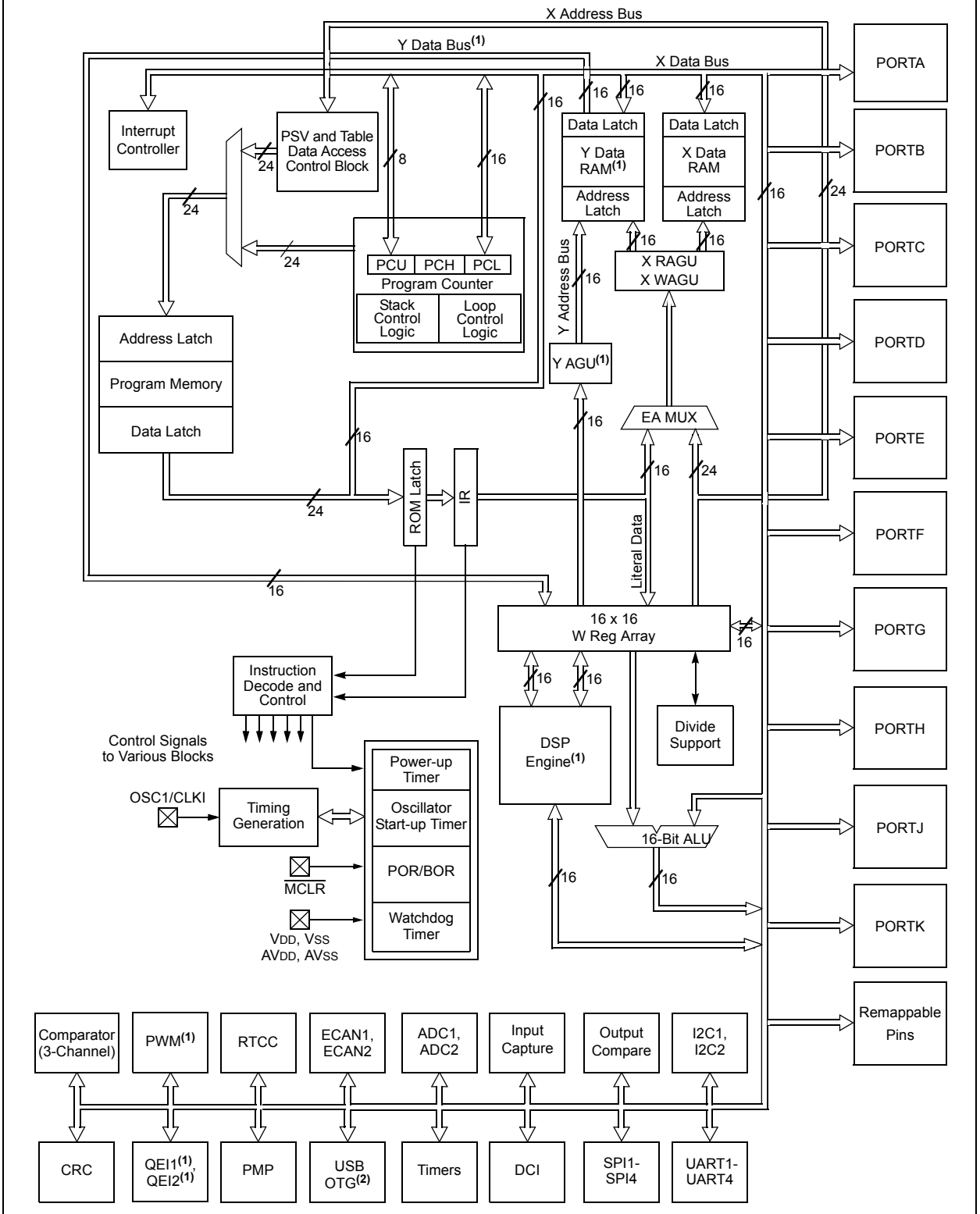


Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RKx) can be used as change notification (CNAx-CNKx). See **Section 11.0 "I/O Ports"** for more information.

3: The availability of I^2C interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

FIGURE 3-1: dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 CPU BLOCK DIAGRAM



Note 1: This feature or peripheral is only available on dsPIC33EPXXX(MC/MU)806/810/814 devices.

2: This feature or peripheral is only available on dsPIC33EPXXXMU806/810/814 and PIC24EPXXXGU806/810/814 devices.

REGISTER 3-2: CORCON: CORE CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
VAR	—	US<1:0>(1)		EDT(1,2)	DL<2:0>(1)		
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R-0	R/W-0	R/W-0
SATA(1)	SATB(1)	SATDW(1)	ACCSAT(1)	IPL3(3)	SFA	RND(1)	IF(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **VAR:** Variable Exception Processing Latency Control bit
1 = Variable exception processing is enabled
0 = Fixed exception processing is enabled

bit 14 **Unimplemented:** Read as '0'

bit 13-12 **US<1:0>:** DSP Multiply Unsigned/Signed Control bits(1)
11 = Reserved
10 = DSP engine multiplies are mixed-sign
01 = DSP engine multiplies are unsigned
00 = DSP engine multiplies are signed

bit 11 **EDT:** Early DO Loop Termination Control bit(1,2)
1 = Terminates executing DO loop at end of current loop iteration
0 = No effect

bit 10-8 **DL<2:0>:** DO Loop Nesting Level Status bits(1)
111 = 7 DO loops are active
•
•
•
001 = 1 DO loop is active
000 = 0 DO loops are active

bit 7 **SATA:** ACCA Saturation Enable bit(1)
1 = Accumulator A saturation is enabled
0 = Accumulator A saturation is disabled

bit 6 **SATB:** ACCB Saturation Enable bit(1)
1 = Accumulator B saturation is enabled
0 = Accumulator B saturation is disabled

bit 5 **SATDW:** Data Space Write from DSP Engine Saturation Enable bit(1)
1 = Data space write saturation is enabled
0 = Data space write saturation is disabled

bit 4 **ACCSAT:** Accumulator Saturation Mode Select bit(1)
1 = 9.31 saturation (super saturation)
0 = 1.31 saturation (normal saturation)

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3(3)
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

Note 1: This bit is available on dsPIC33EPXXX(GP/MC/MU)806/810/814 devices only.
2: This bit is always read as '0'.
3: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 4. "Program Memory"** (DS70613) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

The device architecture features separate program and data memory spaces and buses. This architecture also allows the direct access of program memory from the data space during code execution.

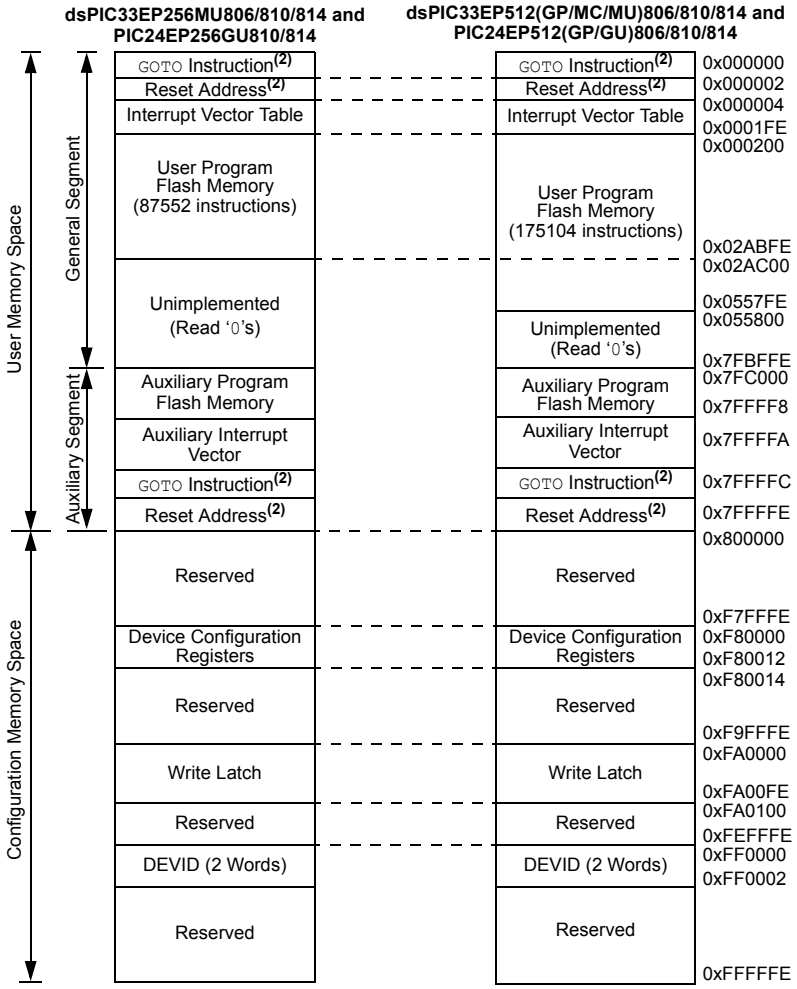
4.1 Program Address Space

The device program address memory space is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit PC during program execution, or from table operation or data space remapping as described in **Section 4.8 "Interfacing Program and Data Memory Spaces"**.

User application access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFF). The exception is the use of `TBLRD/TBLWT` operations, which use TBLPAG<7> to permit access to the Configuration bits and Device ID sections of the configuration memory space.

The device program memory map is shown in Figure 4-1.

FIGURE 4-1: PROGRAM MEMORY MAP FOR dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 DEVICES(1)



Note 1: Memory areas are not shown to scale.

2: The Reset location is controlled by the Reset Target Vector Select bit, RSTPRI (FICD<2>). See **Section 29.0 "Special Features"** for more information.

Allocating different Page registers for read and write access allows the architecture to support data movement between different pages in data memory. This is accomplished by setting the DSRPAG register value to the page from which you want to read and configuring the DSWPAG register to the page to which it needs to be written. Data can also be moved from different PSV to EDS pages, by configuring the DSRPAG and DSWPAG registers to address PSV and EDS space, respectively. The data can be moved between pages by a single instruction.

When an EDS or PSV page overflow or underflow occurs, EA<15> is cleared as a result of the register indirect EA calculation. An overflow or underflow of the EA in the EDS or PSV pages can occur at the page boundaries when:

- The initial address, prior to modification, addresses an EDS or PSV page.
- The EA calculation uses Pre- or Post-Modified Register Indirect Addressing. However, this does not include Register Offset Addressing.

In general, when an overflow is detected, the DSxPAG register is incremented and the EA<15> bit is set to keep the base address within the EDS or PSV window. When an underflow is detected, the DSxPAG register is decremented and the EA<15> bit is set to keep the base address within the EDS or PSV window. This creates a linear EDS and PSV address space, but only when using Register Indirect Addressing modes.

Exceptions to the operation described above arise when entering and exiting the boundaries of Page 0, EDS and PSV spaces. Table 4-73 lists the effects of overflow and underflow scenarios at different boundaries.

In the following cases, when overflow or underflow occurs, the EA<15> bit is set and the DSxPAG is not modified; therefore, the EA will wrap to the beginning of the current page:

- Register Indirect with Register Offset Addressing
- Modulo Addressing
- Bit-Reversed Addressing

TABLE 4-73: OVERFLOW AND UNDERFLOW SCENARIOS AT PAGE 0, EDS and PSV SPACE BOUNDARIES(2,3,4)

O/U, R/W	Operation	Before			After		
		DSxPAG	DS EA<15>	Page Description	DSxPAG	DS EA<15>	Page Description
O, Read	[++Wn] or [Wn++]	DSRPAG = 0x1FF	1	EDS: Last page	DSRPAG = 0x1FF	0	See **Note 1**
O, Read		DSRPAG = 0x2FF	1	PSV: Last lsw page	DSRPAG = 0x300	1	PSV: First MSB page
O, Read		DSRPAG = 0x3FF	1	PSV: Last MSB page	DSRPAG = 0x3FF	0	See **Note 1**
O, Write		DSWPAG = 0x1FF	1	EDS: Last page	DSWPAG = 0x1FF	0	See **Note 1**
U, Read	[--Wn] or [Wn--]	DSRPAG = 0x001	1	EDS page	DSRPAG = 0x001	0	See **Note 1**
U, Read		DSRPAG = 0x200	1	PSV: First lsw page	DSRPAG = 0x200	0	See **Note 1**
U, Read		DSRPAG = 0x300	1	PSV: First MSB page	DSRPAG = 0x2FF	1	PSV: Last lsw page

Legend: O = Overflow, U = Underflow, R = Read, W = Write

Note 1: Register Indirect Addressing now addresses a location in the Base Data Space (0x0000-0x8000).

2: An EDS access with DSxPAG = 0x000 will generate an address error trap.

3: Only reads from PS are supported using DSRPAG. An attempt to write to PS using DSWPAG will generate an address error trap.

4: Pseudo-Linear Addressing is not supported for large offsets.

5.4 Flash Program Memory Resources

Many useful resources related to Flash program memory are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310

5.4.1 KEY RESOURCES

- **Section 5. "Flash Programming"** (DS70609) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

5.5 Control Registers

Four SFRs are used to read and write the program Flash memory: NVMCON, NVMKEY, NVMADRU and NVMADR.

The NVMCON register (Register 5-1) controls which blocks are to be erased, which memory type is to be programmed and the start of the programming cycle.

NVMKEY (Register 5-4) is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register.

There are two NVM Address registers: NVMADRU and NVMADR. These two registers, when concatenated, form the 24-bit Effective Address (EA) of the selected row or word for programming operations, or the selected page for erase operations.

The NVMADRU register is used to hold the upper 8 bits of the EA, while the NVMADR register is used to hold the lower 16 bits of the EA.

REGISTER 9-3: PLLFBD: PLL FEEDBACK DIVISOR REGISTER(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	PLLDIV<8>
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
PLLDIV<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as '0'

bit 8-0 **PLLDIV<8:0>:** PLL Feedback Divisor bits (also denoted as 'M', PLL multiplier)

111111111 = 513
•
•
•
000110000 = 50 (default)
•
•
•
000000010 = 4
000000001 = 3
000000000 = 2

Note 1: This register is reset only on a Power-on Reset (POR).

TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES (CONTINUED)

Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment
010 1011	I	RPI43
010 1100	I	RPI44
101 1010	—	Reserved
101 1011	—	Reserved
101 1100	—	Reserved
101 1101	—	Reserved
101 1110	—	Reserved
101 1111	—	Reserved
110 0000	I/O	RP96
110 0001	I/O	RP97
110 0010	I/O	RP98
110 0011	I/O	RP99
110 0100	I/O	RP100
110 0101	I/O	RP101
110 0110	I/O	RP102
110 0111	—	Reserved
110 1000	I/O	RP104
110 1001	—	Reserved
110 1010	—	Reserved
110 1011	—	Reserved
110 1100	I/O	RP108

Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment
101 1000	I	RPI88
101 1001	I	RPI89
110 1101	I/O	RP109
110 1110	—	Reserved
110 1111	—	Reserved
111 0000	I/O	RP112
111 0001	I/O	RP113
111 0010	—	Reserved
111 0011	—	Reserved
111 0100	—	Reserved
111 0101	—	Reserved
111 0110	I/O	RP118
111 0111	I	RPI119
111 1000	I/O	RP120
111 1001	I	RPI121
111 1010	—	Reserved
111 1011	—	Reserved
111 1100	I	RPI124
111 1101	I/O	RP125
111 1110	I/O	RP126
111 1111	I/O	RP127

Note 1: See **Section 11.4.4.2 “Virtual Connections”** for more information on selecting this pin assignment.

REGISTER 11-7: RPINR6: PERIPHERAL PIN SELECT INPUT REGISTER 6

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	T9CKR<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	T8CKR<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **T9CKR<6:0>:** Assign Timer9 External Clock (T9CK) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **T8CKR<6:0>:** Assign Timer8 External Clock (T8CK) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

REGISTER 11-45: RPOR1: PERIPHERAL PIN SELECT OUTPUT REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP67R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP66R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP67R<5:0>:** Peripheral Output Function is Assigned to RP67 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP66R<5:0>:** Peripheral Output Function is Assigned to RP66 Output Pin bits (see Table 11-3 for peripheral function numbers)

REGISTER 11-46: RPOR2: PERIPHERAL PIN SELECT OUTPUT REGISTER 2

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP69R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP68R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

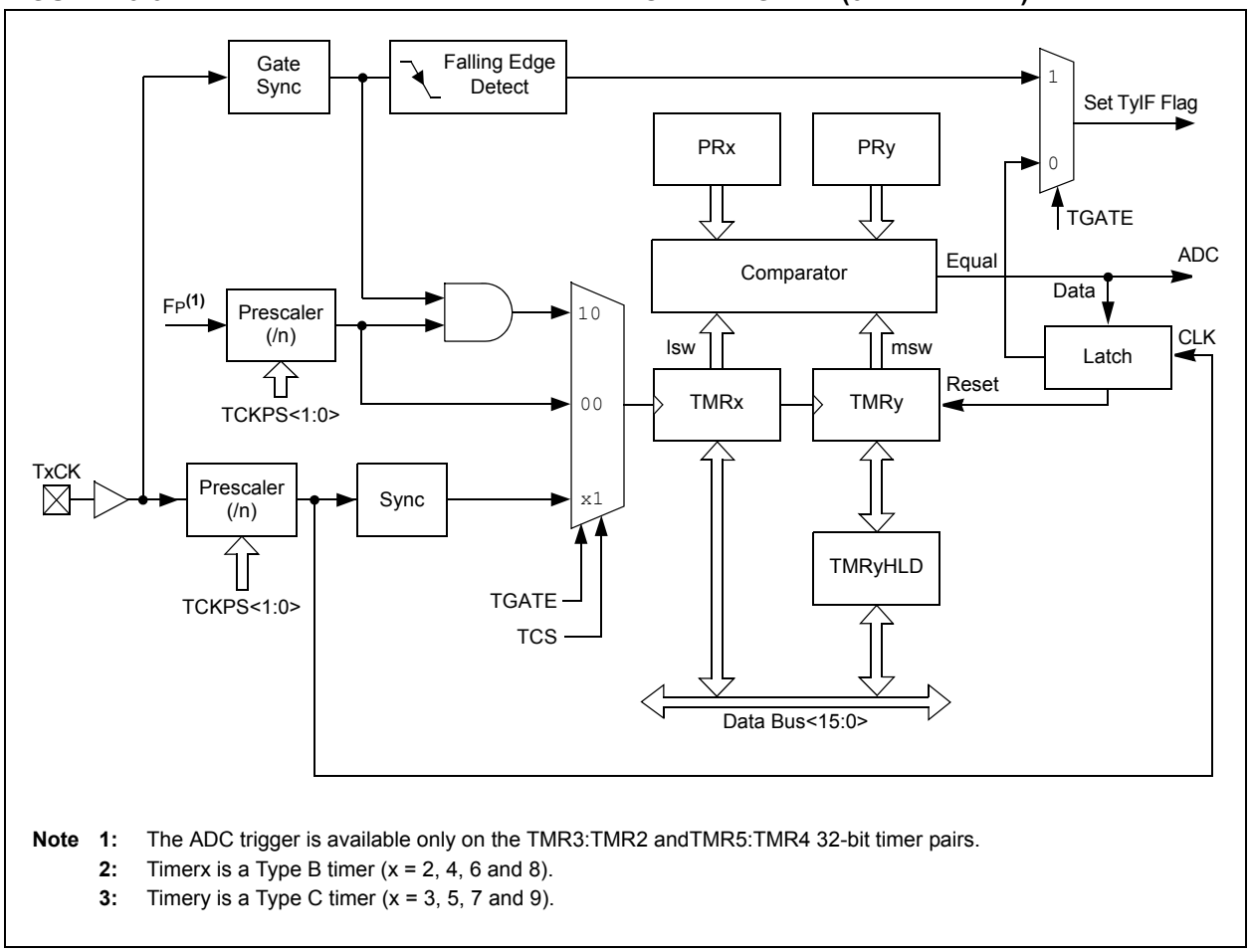
bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP69R<5:0>:** Peripheral Output Function is Assigned to RP69 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP68R<5:0>:** Peripheral Output Function is Assigned to RP68 Output Pin bits (see Table 11-3 for peripheral function numbers)

FIGURE 13-3: TYPE B/TYPE C TIMER PAIR BLOCK DIAGRAM (32-BIT TIMER)



Note 1: The ADC trigger is available only on the TMR3:TMR2 andTMR5:TMR4 32-bit timer pairs.
2: Timerx is a Type B timer (x = 2, 4, 6 and 8).
3: Timery is a Type C timer (x = 3, 5, 7 and 9).

13.1 Timer Resources

Many useful resources related to timers are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310

13.1.1 KEY RESOURCES

- **Section 11. "Timers"** (DS70362) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

16.0 HIGH-SPEED PWM MODULE (dsPIC33EPXXX(MC/MU)8XX DEVICES ONLY)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "High-Speed PWM"** (DS70645) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXX(MC/MU)806/810/814 devices support a dedicated Pulse-Width Modulation (PWM) module with up to 14 outputs.

The high-speed PWM module consists of the following major features:

- Two master time base modules with Special Event Triggers
- PWM module input clock prescaler
- Two synchronization inputs
- Two synchronization outputs
- Up to seven PWM generators
- Two PWM outputs per generator (PWMxH and PWMxL)
- Individual period, duty cycle and phase shift for each PWM output
- Period, duty cycle, phase shift and dead-time resolution of 8.32 ns
- Immediate update mode for PWM period, duty cycle and phase shift
- Independent Fault and current-limited inputs for each PWM
- Cycle-by-Cycle and Latched Fault modes
- PWM time-base capture upon current limit
- Seven Fault inputs and three comparator outputs available for Faults and current limits
- Programmable ADC trigger with interrupt for each PWM pair
- Complementary PWM outputs
- Push-Pull PWM outputs
- Redundant PWM outputs
- Edge-Aligned PWM mode
- Center-Aligned PWM mode
- Variable Phase PWM mode
- Multi-Phase PWM mode
- Fixed Off Time PWM mode
- Current-Limit PWM mode
- Current Reset PWM mode
- PWMxH and PWMxL output override control
- PWMxH and PWMxL output pin swapping
- Chopping mode (also known as Gated mode)
- Dead-time insertion
- Dead-time compensation
- Enhanced Leading-Edge Blanking (LEB)
- 8 mA PWM pin output drive

Note: Duty cycle, dead time, phase shift and frequency resolution is 16.64 ns in Center-Aligned PWM mode.

The high-speed PWM module contains up to seven PWM generators. Each PWM generator provides two PWM outputs: PWMxH and PWMxL. Two master time base generators provide a synchronous signal as a common time base to synchronize the various PWM outputs. Each generator can operate independently or in synchronization with either of the two master time bases. The individual PWM outputs are available on the output pins of the device. The input Fault signals and current-limited signals, when enabled, can monitor and protect the system by placing the PWM outputs into a known "safe" state.

Each PWM can generate a trigger to the ADC module to sample the analog signal at a specific instance during the PWM period. In addition, the high-speed PWM module also generates two Special Event Triggers to the ADC module based on the two master time bases.

The high-speed PWM module can synchronize itself with an external signal or can act as a synchronizing source to any external device. The SYNCI1 and SYNCI2 pins are the input pins, which can synchronize the high-speed PWM module with an external signal. The SYNCO1 and SYNCO2 pins are output pins that provides a synchronous signal to an external device.

Figure 16-1 illustrates an architectural overview of the high-speed PWM module and its interconnection with the CPU and other peripherals.

REGISTER 16-4: SEVTCMP: PWM PRIMARY SPECIAL EVENT COMPARE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SEVTCMP<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SEVTCMP<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **SEVTCMP<15:0>:** Special Event Compare Count Value bits

17.1 QEI Resources

Many useful resources related to QEI are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310

17.1.1 KEY RESOURCES

- **Section 15. "Quadrature Encoder Interface (QEI)"** (DS70601) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

REGISTER 21-16: CxRXFnSID: ECANx ACCEPTANCE FILTER n STANDARD IDENTIFIER REGISTER n (n = 0-15)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3
bit 15							bit 8

R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
SID2	SID1	SID0	—	EXIDE	—	EID17	EID16
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **SID<10:0>:** Standard Identifier bits
1 = Message address bit, SIDx, must be '1' to match filter
0 = Message address bit, SIDx, must be '0' to match filter

bit 4 **Unimplemented:** Read as '0'

bit 3 **EXIDE:** Extended Identifier Enable bit
If MIDE = 1:
1 = Matches only messages with extended identifier addresses
0 = Matches only messages with standard identifier addresses
If MIDE = 0:
Ignores EXIDE bit.

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **EID<17:16>:** Extended Identifier bits
1 = Message address bit, EIDx, must be '1' to match filter
0 = Message address bit, EIDx, must be '0' to match filter

REGISTER 25-4: CMxMSKCON: COMPARATOR x MASK GATING CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **HLMS:** High or Low-Level Masking Select bits
1 = The masking (blanking) function will prevent any asserted (‘0’) comparator signal from propagating
0 = The masking (blanking) function will prevent any asserted (‘1’) comparator signal from propagating

bit 14 **Unimplemented:** Read as '0'

bit 13 **OCEN:** OR Gate C Input Enable bit
1 = MCI is connected to OR gate
0 = MCI is not connected to OR gate

bit 12 **OCNEN:** OR Gate C Input Inverted Enable bit
1 = Inverted MCI is connected to OR gate
0 = Inverted MCI is not connected to OR gate

bit 11 **OBEN:** OR Gate B Input Enable bit
1 = MBI is connected to OR gate
0 = MBI is not connected to OR gate

bit 10 **OBNEN:** OR Gate B Input Inverted Enable bit
1 = Inverted MBI is connected to OR gate
0 = Inverted MBI is not connected to OR gate

bit 9 **OAEN:** OR Gate A Input Enable bit
1 = MAI is connected to OR gate
0 = MAI is not connected to OR gate

bit 8 **OANEN:** OR Gate A Input Inverted Enable bit
1 = Inverted MAI is connected to OR gate
0 = Inverted MAI is not connected to OR gate

bit 7 **NAGS:** AND Gate Output Inverted Enable bit
1 = Inverted ANDI is connected to OR gate
0 = Inverted ANDI is not connected to OR gate

bit 6 **PAGS:** AND Gate Output Enable bit
1 = ANDI is connected to OR gate
0 = ANDI is not connected to OR gate

bit 5 **ACEN:** AND Gate C Input Enable bit
1 = MCI is connected to AND gate
0 = MCI is not connected to AND gate

bit 4 **ACNEN:** AND Gate C Input Inverted Enable bit
1 = Inverted MCI is connected to AND gate
0 = Inverted MCI is not connected to AND gate

TABLE 30-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles(2)	Status Flags Affected
46	MOV	MOV f,Wn	Move f to Wn	1	1	None
		MOV f	Move f to f	1	1	None
		MOV f,WREG	Move f to WREG	1	1	None
		MOV #lit16,Wn	Move 16-bit literal to Wn	1	1	None
		MOV.b #lit8,Wn	Move 8-bit literal to Wn	1	1	None
		MOV Wn,f	Move Wn to f	1	1	None
		MOV Wso,Wdo	Move Ws to Wd	1	1	None
		MOV WREG,f	Move WREG to f	1	1	None
		MOV.D Wns,Wd	Move Double from W(ns):W(ns + 1) to Wd	1	2	None
		MOV.D Ws,Wnd	Move Double from Ws to W(nd + 1):W(nd)	1	2	None
47	MOVPAG	MOVPAG #lit10,DSRPAG	Move 10-bit literal to DSRPAG	1	1	None
		MOVPAG #lit9,DSWPAG	Move 9-bit literal to DSWPAG	1	1	None
		MOVPAG #lit8,TBLPAG	Move 8-bit literal to TBLPAG	1	1	None
		MOVPAGW Ws, DSRPAG	Move Ws<9:0> to DSRPAG	1	1	None
		MOVPAGW Ws, DSWPAG	Move Ws<8:0> to DSWPAG	1	1	None
		MOVPAGW Ws, TBLPAG	Move Ws<7:0> to TBLPAG	1	1	None
48	MOVSAC	MOVSAC Acc,Wx,Wxd,Wy,Wyd,AWB(1)	Prefetch and store accumulator	1	1	None
49	MPY	MPY Wm*Wn,Acc,Wx,Wxd,Wy,Wyd(1)	Multiply Wm by Wn to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		MPY Wm*Wm,Acc,Wx,Wxd,Wy,Wyd(1)	Square Wm to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
50	MPY.N	MPY.N Wm*Wn,Acc,Wx,Wxd,Wy,Wyd(1)	-(Multiply Wm by Wn) to Accumulator	1	1	None
51	MSC	MSC Wm*Wm,Acc,Wx,Wxd,Wy,Wyd,AWB(1)	Multiply and Subtract from Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
52	MUL	MUL.SS Wb,Ws,Wnd	{Wnd + 1, Wnd} = signed(Wb) * signed(Ws)	1	1	None
		MUL.SS Wb,Ws,Acc(1)	Accumulator = signed(Wb) * signed(Ws)	1	1	None
		MUL.SU Wb,Ws,Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb,Ws,Acc(1)	Accumulator = signed(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb,#lit5,Acc(1)	Accumulator = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.US Wb,Ws,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * signed(Ws)	1	1	None
		MUL.US Wb,Ws,Acc(1)	Accumulator = unsigned(Wb) * signed(Ws)	1	1	None
		MUL.UU Wb,Ws,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(Ws)	1	1	None
		MUL.UU Wb,#lit5,Acc(1)	Accumulator = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb,Ws,Acc(1)	Accumulator = unsigned(Wb) * unsigned(Ws)	1	1	None
		MULW.SS Wb,Ws,Wnd	Wnd = signed(Wb) * signed(Ws)	1	1	None
		MULW.SU Wb,Ws,Wnd	Wnd = signed(Wb) * unsigned(Ws)	1	1	None
		MULW.US Wb,Ws,Wnd	Wnd = unsigned(Wb) * signed(Ws)	1	1	None
		MULW.UU Wb,Ws,Wnd	Wnd = unsigned(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb,#lit5,Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.SU Wb,#lit5,Wnd	Wnd = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb,#lit5,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb,#lit5,Wnd	Wnd = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL f	W3:W2 = f * WREG	1	1	None

Note 1: This instruction is available in dsPIC33EPXXX(GP/MC/MU)806/810/814 devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

FIGURE 32-5: BOR AND MASTER CLEAR RESET TIMING CHARACTERISTICS

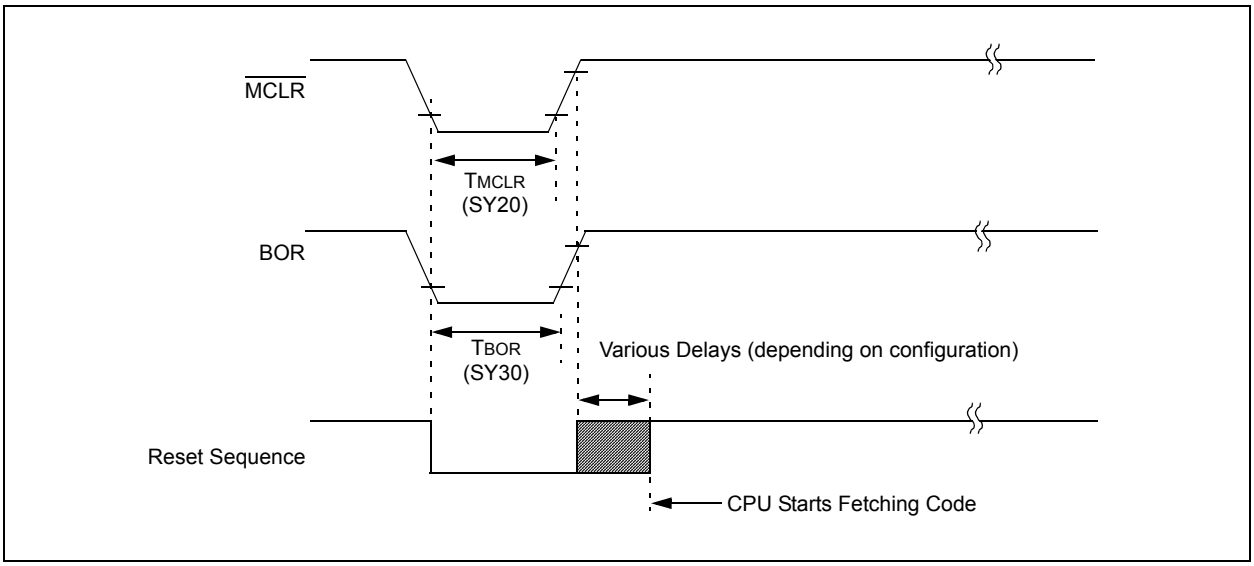


TABLE 32-22: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SY00	TPU	Power-up Period	—	400	600	μs	
SY10	TOST	Oscillator Start-up Time	—	1024 TOSC	—	—	TOSC = OSC1 period
SY11	TPWRT	Power-up Timer Period	—	—	—	—	See **Section 29.1 "Configuration Bits"** and LPRC Parameters F21a and F21b (Table 32-20)
SY12	TWDT	Watchdog Timer Time-out Period	—	—	—	—	See **Section 29.4 "Watchdog Timer (WDT)"** and LPRC Parameters F21a and F21b (Table 32-20)
SY13	TIOZ	I/O High-Impedance from MCLR Low or Watchdog Timer Reset	0.68	0.72	1.2	μs	
SY20	TMCLR	MCLR Pulse Width (low)	2	—	—	μs	
SY30	TBOR	BOR Pulse Width (low)	1	—	—	μs	
SY35	TFSCM	Fail-Safe Clock Monitor Delay	—	500	900	μs	-40°C to +85°C
SY36	TVREG	Voltage Regulator Standby-to-Active Mode Transition Time	—	—	30	μs	
SY37	TOSCDFRC	FRC Oscillator Start-up Delay	—	—	29	μs	
SY38	TOSCDLPRC	LPRC Oscillator Start-up Delay	—	—	70	μs	

Note 1: These parameters are characterized but not tested in manufacturing.
2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

FIGURE 32-42: PARALLEL SLAVE PORT TIMING

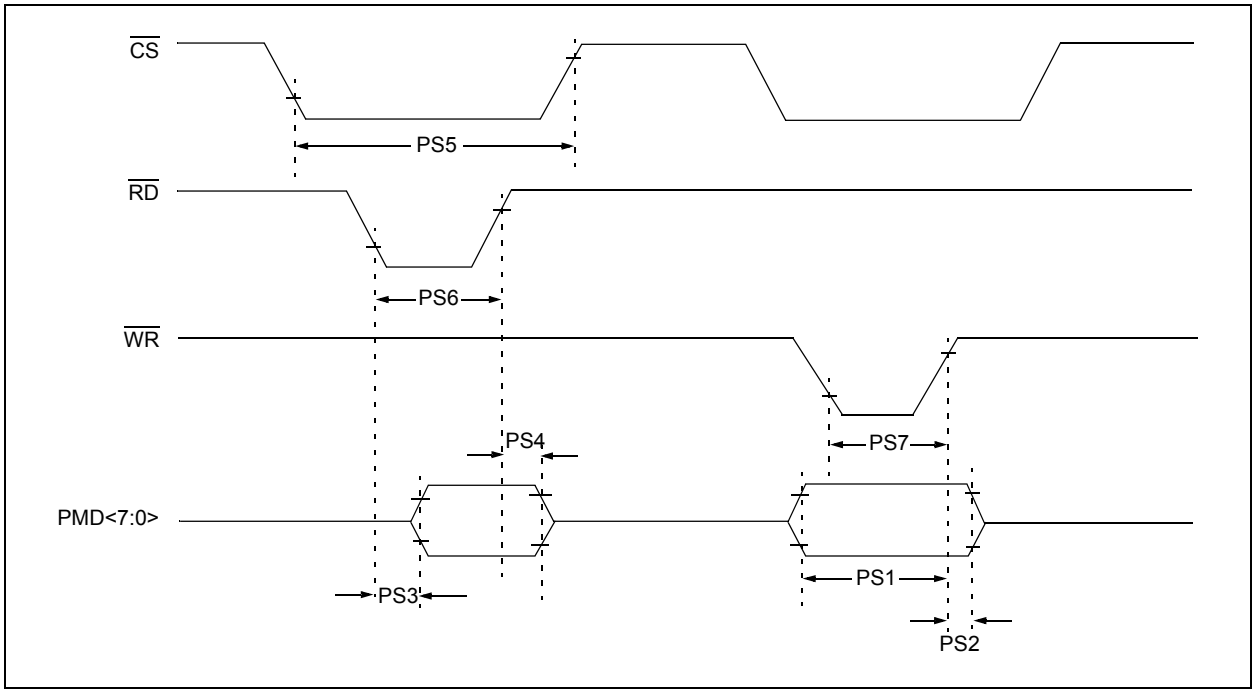


TABLE 32-65: PARALLEL SLAVE PORT TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
PS1	TdtV2wrH	Data In Valid Before $\overline{WR}$ or $\overline{CS}$ Inactive (setup time)	20	—	—	ns	
PS2	TwrH2dtI	$\overline{WR}$ or $\overline{CS}$ Inactive to Data In Invalid (hold time)	20	—	—	ns	
PS3	TrdL2dtV	$\overline{RD}$ and $\overline{CS}$ to Active Data Out Valid	—	—	80	ns	
PS4	TrdH2dtI	$\overline{RD}$ or $\overline{CS}$ Inactive to Data Out Invalid	10	—	30	ns	
PS5	Tcs	$\overline{CS}$ Active Time	33.33	—	—	ns	
PS6	Twr	$\overline{RD}$ Active Time	33.33	—	—	ns	
PS7	Trd	$\overline{WR}$ Active Time	33.33	—	—	ns	

Note 1: These parameters are characterized, but not tested in manufacturing.