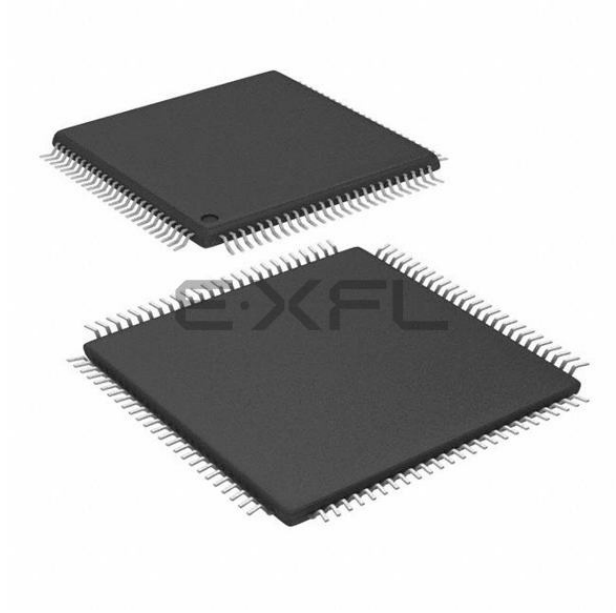
Microchip Technology - DSPIC33EP256MU810T-I/PT Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, QEI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	83
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256mu810t-i-pt

1.0 DEVICE OVERVIEW

Note 1: This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive resource. To complement the information in this data sheet, refer to the related section of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com)

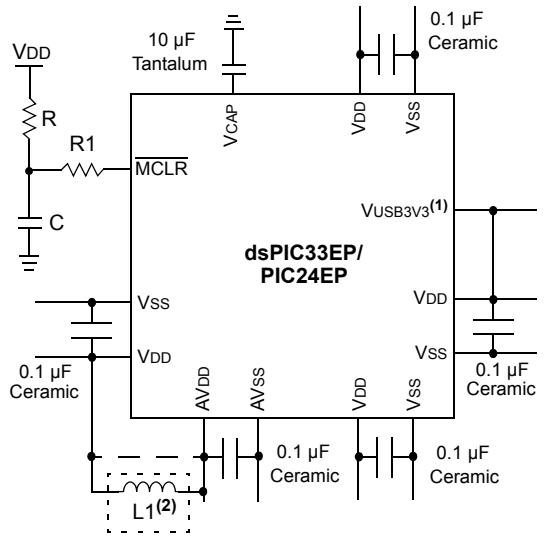
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This document contains device-specific information for the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 Digital Signal Controller (DSC) and Microcontroller (MCU) devices. The dsPIC33EPXXX(GP/MC/MU)806/810/814 devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance 16-bit MCU architecture.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices.

Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



Note 1: If the USB module is not used, VUSB3V3 must be connected to VDD, as shown.

2: As an option, instead of a hard-wired connection, an inductor (L1) can be substituted between VDD and AVDD to improve ADC noise rejection. The inductor impedance should be less than 1Ω and the inductor capacity greater than 10 mA.

Where:

$$f = \frac{F_{CNV}}{2}$$ (i.e., ADC conversion rate/2)

$$f = \frac{1}{(2\pi\sqrt{LC})}$$

$$L = \left(\frac{1}{(2\pi f\sqrt{C})}\right)^2$$

2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

2.3 CPU Logic Filter Capacitor Connection (VCAP)

A low-ESR (< 1 Ohms) capacitor is required on the VCAP pin, which is used to stabilize the voltage regulator output voltage. The VCAP pin must not be connected to VDD and must have a capacitor greater than 4.7 µF (10 µF is recommended), 16V connected to ground. The type can be ceramic or tantalum. See **Section 32.0 "Electrical Characteristics"** for additional information.

The placement of this capacitor should be close to the VCAP. It is recommended that the trace length not exceeds one-quarter inch (6 mm). See **Section 29.2 "On-Chip Voltage Regulator"** for details.

2.4 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions:

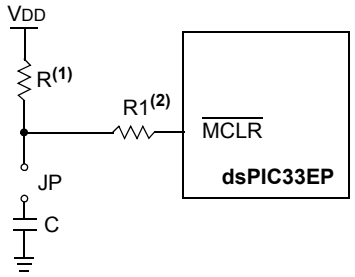
- Device Reset
- Device Programming and Debugging

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-2, it is recommended that the capacitor C, be isolated from the MCLR pin during programming and debugging operations.

Place the components as shown in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



Note 1: R ≤ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the MCLR pin VIH and VIL specifications are met.

2: R1 ≤ 470Ω will limit any current flowing into MCLR from the external capacitor C, in the event of MCLR pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the MCLR pin VIH and VIL specifications are met.

3.8 Arithmetic Logic Unit (ALU)

The ALU is 16 bits wide and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. Depending on the operation, the ALU can affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

Refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157) for information on the SR bits affected by each instruction.

The core CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit divisor division.

3.8.1 MULTIPLIER

Using the high-speed 17-bit x 17-bit multiplier, the ALU supports unsigned, signed, or mixed-sign operation in several MCU multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit signed x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- 8-bit unsigned x 8-bit unsigned

3.8.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

1. 32-bit signed/16-bit signed divide
2. 32-bit unsigned/16-bit unsigned divide
3. 16-bit signed/16-bit signed divide
4. 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. The 16-bit signed and unsigned `DIV` instructions can specify any W register for both the 16-bit divisor (Wn) and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

3.9 DSP Engine (dsPIC33EPXXX(GP/MC/MU)806/810/814 Devices Only)

The DSP engine consists of a high-speed 17-bit x 17-bit multiplier, a 40-bit barrel shifter and a 40-bit adder/subtracter (with two target accumulators, round and saturation logic).

The DSP engine can also perform inherent accumulator-to-accumulator operations that require no additional data. These instructions are: `ADD`, `SUB` and `NEG`.

The DSP engine has options selected through bits in the CPU Core Control register (CORCON), as listed below:

- Fractional or integer DSP multiply (IF)
- Signed, unsigned or mixed-sign DSP multiply (US)
- Conventional or convergent rounding (RND)
- Automatic saturation on/off for ACCA (SATA)
- Automatic saturation on/off for ACCB (SATB)
- Automatic saturation on/off for writes to data memory (SATDW)
- Accumulator Saturation mode selection (ACCSAT)

TABLE 3-2: DSP INSTRUCTIONS SUMMARY

Instruction	Algebraic Operation	ACC Write Back
CLR	$A = 0$	Yes
ED	$A = (x - y)^2$	No
EDAC	$A = A + (x - y)^2$	No
MAC	$A = A + (x \bullet y)$	Yes
MAC	$A = A + x^2$	No
MOVSAC	No change in A	Yes
MPY	$A = x \bullet y$	No
MPY	$A = x^2$	No
MPY.N	$A = -x \bullet y$	No
MSC	$A = A - x \bullet y$	Yes

TABLE 4-4: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMU810 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	NVMIF	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	IC8IF	IC7IF	AD2IF	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	T6IF	DMA4IF	PMPIF	OC8IF	OC7IF	OC6IF	OC5IF	IC6IF	IC5IF	IC4IF	IC3IF	DMA3IF	C1IF	C1RXIF	SPI2IF	SPI2EIF	0000
IFS3	0806	—	RTCIF	DMA5IF	DCIIF	DCIEIF	QEI1IF	PSEMIF	C2IF	C2RXIF	INT4IF	INT3IF	T9IF	T8IF	MI2C2IF	SI2C2IF	T7IF	0000
IFS4	0808	—	—	—	—	QEI2IF	—	PSESMIF	—	C2TXIF	C1TXIF	DMA7IF	DMA6IF	CRCIF	U2EIF	U1EIF	—	0000
IFS5	080A	PWM2IF	PWM1IF	IC9IF	OC9IF	SPI3IF	SPI3EIF	U4TXIF	U4RXIF	U4EIF	USB1IF	—	—	U3TXIF	U3RXIF	U3EIF	—	0000
IFS6	080C	—	—	—	—	—	—	—	—	—	—	—	—	PWM6IF	PWM5IF	PWM4IF	PWM3IF	0000
IFS7	080E	IC11IF	OC11IF	IC10IF	OC10IF	SPI4IF	SPI4EIF	DMA11IF	DMA10IF	DMA9IF	DMA8IF	—	—	—	—	—	—	0000
IFS8	0810	—	ICDIF	IC16IF	OC16IF	IC15IF	OC15IF	IC14IF	OC14IF	IC13IF	OC13IF	—	DMA14IF	DMA13IF	DMA12IF	IC12IF	OC12IF	0000
IEC0	0820	NVMIE	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	IC8IE	IC7IE	AD2IE	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	T6IE	DMA4IE	PMPIE	OC8IE	OC7IE	OC6IE	OC5IE	IC6IE	IC5IE	IC4IE	IC3IE	DMA3IE	C1IE	C1RXIE	SPI2IE	SPI2EIE	0000
IEC3	0826	—	RTCIE	DMA5IE	DCIIE	DCIEIE	QEI1IE	PSEMIE	C2IE	C2RXIE	INT4IE	INT3IE	T9IE	T8IE	MI2C2IE	SI2C2IE	T7IE	0000
IEC4	0828	—	—	—	—	QEI2IE	—	PSESMIE	—	C2TXIE	C1TXIE	DMA7IE	DMA6IE	CRCIE	U2EIE	U1EIE	—	0000
IEC5	082A	PWM2IE	PWM1IE	IC9IE	OC9IE	SPI3IE	SPI3EIE	U4TXIE	U4RXIE	U4EIE	USB1IE	—	—	U3TXIE	U3RXIE	U3EIE	—	0000
IEC6	082C	—	—	—	—	—	—	—	—	—	—	—	—	PWM6IE	PWM5IE	PWM4IE	PWM3IE	0000
IEC7	082E	IC11IE	OC11IE	IC10IE	OC10IE	SPI4IE	SPI4EIE	DMA11IE	DMA10IE	DMA9IE	DMA8IE	—	—	—	—	—	—	0000
IEC8	0830	—	ICDIE	IC16IE	OC16IE	IC15IE	OC15IE	IC14IE	OC14IE	IC13IE	OC13IE	—	DMA14IE	DMA13IE	DMA12IE	IC12IE	OC12IE	0000
IPC0	0840	—	T1IP<2:0>			—	OC1IP<2:0>			—	IC1IP<2:0>			—	INT0IP<2:0>			4444
IPC1	0842	—	T2IP<2:0>			—	OC2IP<2:0>			—	IC2IP<2:0>			—	DMA0IP<2:0>			4444
IPC2	0844	—	U1RXIP<2:0>			—	SPI1IP<2:0>			—	SPI1EIP<2:0>			—	T3IP<2:0>			4444
IPC3	0846	—	NVMIP<2:0>			—	DMA1IP<2:0>			—	AD1IP<2:0>			—	U1TXIP<2:0>			4444
IPC4	0848	—	CNIP<2:0>			—	CMIP<2:0>			—	MI2C1IP<2:0>			—	SI2C1IP<2:0>			4444
IPC5	084A	—	IC8IP<2:0>			—	IC7IP<2:0>			—	AD2IP<2:0>			—	INT1IP<2:0>			4444
IPC6	084C	—	T4IP<2:0>			—	OC4IP<2:0>			—	OC3IP<2:0>			—	DMA2IP<2:0>			4444
IPC7	084E	—	U2TXIP<2:0>			—	U2RXIP<2:0>			—	INT2IP<2:0>			—	T5IP<2:0>			4444
IPC8	0850	—	C1IP<2:0>			—	C1RXIP<2:0>			—	SPI2IP<2:0>			—	SPI2EIP<2:0>			4444
IPC9	0852	—	IC5IP<2:0>			—	IC4IP<2:0>			—	IC3IP<2:0>			—	DMA3IP<2:0>			4444
IPC10	0854	—	OC7IP<2:0>			—	OC6IP<2:0>			—	OC5IP<2:0>			—	IC6IP<2:0>			4444
IPC11	0856	—	T6IP<2:0>			—	DMA4IP<2:0>			—	PMPIP<2:0>			—	OC8IP<2:0>			4444
IPC12	0858	—	T8IP<2:0>			—	MI2C2IP<2:0>			—	SI2C2IP<2:0>			—	T7IP<2:0>			4444
IPC13	085A		C2RXIP<2:0>			—	INT4IP<2:0>			—	INT3IP<2:0>			—	T9IP<2:0>			4444
IPC14	085C	—	DCIEIP<2:0>			—	QEI1IP<2:0>			—	PSEMIP<2:0>			—	C2IP<2:0>			4444
IPC15	085E	—	—	—	—	—	RTCIP<2:0>			—	DMA5IP<2:0>			—	DCIIP<2:0>			0444

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-11: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 16 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OC1CON1	0900	—	—	OCSIDL	OCTSEL<2:0>			ENFLTC	ENFLTB	ENFLTA	OCFLTC	OCFLTB	OCFLTA	TRIGMODE	OCM<2:0>			0000
OC1CON2	0902	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL<4:0>					000C
OC1RS	0904	Output Compare 1 Secondary Register																xxxx
OC1R	0906	Output Compare 1 Register																xxxx
OC1TMR	0908	Timer Value 1 Register																xxxx
OC2CON1	090A	—	—	OCSIDL	OCTSEL<2:0>			ENFLTC	ENFLTB	ENFLTA	OCFLTC	OCFLTB	OCFLTA	TRIGMODE	OCM<2:0>			0000
OC2CON2	090C	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL<4:0>					000C
OC2RS	090E	Output Compare 2 Secondary Register																xxxx
OC2R	0910	Output Compare 2 Register																xxxx
OC2TMR	0912	Timer Value 2 Register																xxxx
OC3CON1	0914	—	—	OCSIDL	OCTSEL<2:0>			ENFLTC	ENFLTB	ENFLTA	OCFLTC	OCFLTB	OCFLTA	TRIGMODE	OCM<2:0>			0000
OC3CON2	0916	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL<4:0>					000C
OC3RS	0918	Output Compare 3 Secondary Register																xxxx
OC3R	091A	Output Compare 3 Register																xxxx
OC3TMR	091C	Timer Value 3 Register																xxxx
OC4CON1	091E	—	—	OCSIDL	OCTSEL<2:0>			ENFLTC	ENFLTB	ENFLTA	OCFLTC	OCFLTB	OCFLTA	TRIGMODE	OCM<2:0>			0000
OC4CON2	0920	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL<4:0>					000C
OC4RS	0922	Output Compare 4 Secondary Register																xxxx
OC4R	0924	Output Compare 4 Register																xxxx
OC4TMR	0926	Timer Value 4 Register																xxxx
OC5CON1	0928	—	—	OCSIDL	OCTSEL<2:0>			ENFLTC	ENFLTB	ENFLTA	OCFLTC	OCFLTB	OCFLTA	TRIGMODE	OCM<2:0>			0000
OC5CON2	092A	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL<4:0>					000C
OC5RS	092C	Output Compare 5 Secondary Register																xxxx
OC5R	092D	Output Compare 5 Register																xxxx
OC5TMR	0930	Timer Value 5 Register																xxxx
OC6CON1	0932	—	—	OCSIDL	OCTSEL<2:0>			ENFLTC	ENFLTB	ENFLTA	OCFLTC	OCFLTB	OCFLTA	TRIGMODE	OCM<2:0>			0000
OC6CON2	0934	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL<4:0>					000C
OC6RS	0936	Output Compare 6 Secondary Register																xxxx
OC6R	0938	Output Compare 6 Register																xxxx
OC6TMR	093A	Timer Value 6 Register																xxxx
OC7CON1	093C	—	—	OCSIDL	OCTSEL<2:0>			ENFLTC	ENFLTB	ENFLTA	OCFLTC	OCFLTB	OCFLTA	TRIGMODE	OCM<2:0>			0000
OC7CON2	093E	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL<4:0>					000C
OC7RS	0940	Output Compare 7 Secondary Register																xxxx
OC7R	0942	Output Compare 7 Register																xxxx
OC7TMR	0944	Timer Value 7 Register																xxxx

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 8-14: DMAPPS: DMA PING-PONG STATUS REGISTER (CONTINUED)

bit 2 **PPST2:** Channel 2 Ping-Pong Mode Status Flag bit
1 = DMASTB2 register selected
0 = DMASTA2 register selected

bit 1 **PPST1:** Channel 1 Ping-Pong Mode Status Flag bit
1 = DMASTB1 register selected
0 = DMASTA1 register selected

bit 0 **PPST0:** Channel 0 Ping-Pong Mode Status Flag bit
1 = DMASTB0 register selected
0 = DMASTA0 register selected

REGISTER 11-27: RPINR27: PERIPHERAL PIN SELECT INPUT REGISTER 27

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	U3CTSR<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	U3RXR<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **U3CTSR<6:0>:** Assign UART3 Clear-to-Send ($\overline{U3CTS}$) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **U3RXR<6:0>:** Assign UART3 Receive (U3RX) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

REGISTER 16-11: PWMCONx: PWMx CONTROL REGISTER (CONTINUED)

bit 7-6 **DTC<1:0>:** Dead-Time Control bits
11 = Dead-Time Compensation mode
10 = Dead-time function is disabled
01 = Negative dead time actively applied for Complementary Output mode
00 = Positive dead time actively applied for all output modes

bit 5 **DTCP:** Dead-Time Compensation Polarity bit(3)
When set to '1':
If DTCMPx = 0, PWMxL is shortened and PWMxH is lengthened.
If DTCMPx = 1, PWMxH is shortened and PWMxL is lengthened.
When set to '0':
If DTCMPx = 0, PWMxH is shortened and PWMxL is lengthened.
If DTCMPx = 1, PWMxL is shortened and PWMxH is lengthened.

bit 4 **Unimplemented:** Read as '0'

bit 3 **MTBS:** Master Time Base Select bit
1 = PWM generator uses the secondary master time base for synchronization and as the clock source for the PWM generation logic (if secondary time base is available)
0 = PWM generator uses the primary master time base for synchronization and as the clock source for the PWM generation logic

bit 2 **CAM:** Center-Aligned Mode Enable bit(2,4)
1 = Center-Aligned mode is enabled
0 = Edge-Aligned mode is enabled

bit 1 **XPRES:** External PWM Reset Control bit(5)
1 = Current-limit source resets the time base for this PWM generator if it is in Independent Time Base mode
0 = External pins do not affect PWM time base

bit 0 **IUE:** Immediate Update Enable bit(2)
1 = Updates to the active MDC/PDCx/SDCx registers are immediate
0 = Updates to the active PDCx registers are synchronized to the PWM time base

Note 1: Software must clear the interrupt status here and in the corresponding IFS bit in the interrupt controller.
2: These bits should not be changed after the PWM is enabled (PTEN = 1).
3: DTC<1:0> = 11 for DTCP to be effective; otherwise, DTCP is ignored.
4: The Independent Time Base (ITB = 1) mode must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
5: To operate in External Period Reset mode, the ITB bit must be '1' and the CLMOD bit in the FCLCONx register must be '0'.

REGISTER 17-4: POSxCNTH: POSITION COUNTER x HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSCNT<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSCNT<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **POSCNT<31:16>:** High Word Used to Form 32-Bit Position Counter Register (POSxCNT) bits

REGISTER 17-5: POSxCNTL: POSITION COUNTER x LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSCNT<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSCNT<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **POSCNT<15:0>:** Low Word Used to Form 32-Bit Position Counter Register (POSxCNT) bits

REGISTER 17-6: POSxHLD: POSITION COUNTER x HOLD REGISTER

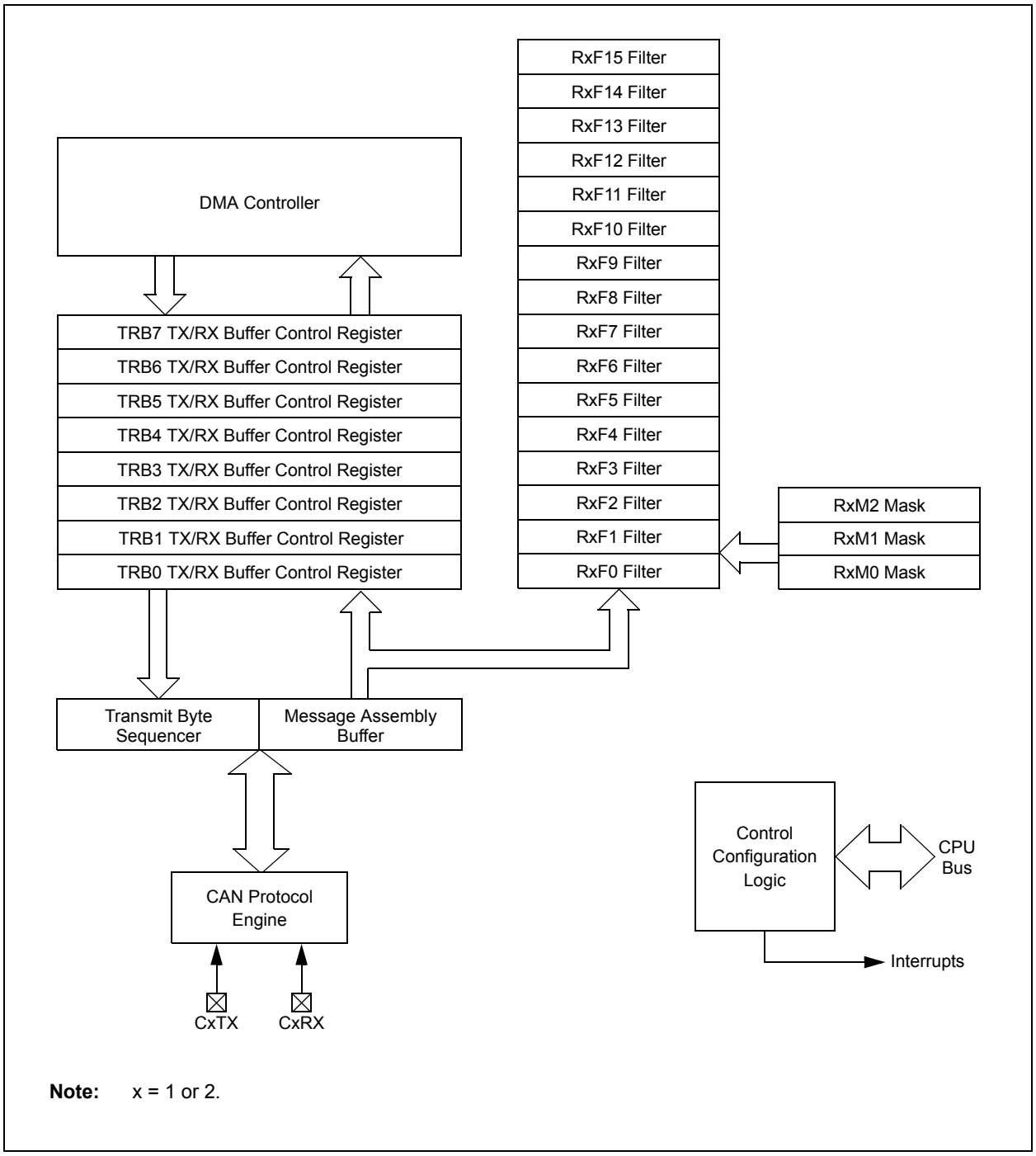
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSHLD<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSHLD<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **POSHLD<15:0>:** Hold Register for Reading and Writing POSxCNTH bits

FIGURE 21-1: ECANx MODULE BLOCK DIAGRAM



Note: x = 1 or 2.

REGISTER 21-11: CxFEN1: ECANx ACCEPTANCE FILTER ENABLE REGISTER 1

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
FLTEN15	FLTEN14	FLTEN13	FLTEN12	FLTEN11	FLTEN10	FLTEN9	FLTEN8
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
FLTEN7	FLTEN6	FLTEN5	FLTEN4	FLTEN3	FLTEN2	FLTEN1	FLTEN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **FLTENn:** Enable Filter n to Accept Messages bits
1 = Enables Filter n
0 = Disables Filter n

REGISTER 21-12: CxBUFPNT1: ECANx FILTER 0-3 BUFFER POINTER REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F3BP<3:0>				F2BP<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F1BP<3:0>				F0BP<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **F3BP<3:0>:** RX Buffer Mask for Filter 3 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F2BP<3:0>:** RX Buffer Mask for Filter 2 bits (same values as bit 15-12)

bit 7-4 **F1BP<3:0>:** RX Buffer Mask for Filter 1 bits (same values as bit 15-12)

bit 3-0 **F0BP<3:0>:** RX Buffer Mask for Filter 0 bits (same values as bit 15-12)

REGISTER 22-4: UxSTAT: USB STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	U-0	U-0
ENDPT<3:0>(2)				DIR	PPBI(1)	—	—
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-4 **ENDPT<3:0>:** Last Endpoint Activity Number bits
(represents the number of the endpoint BDT updated by the last USB transfer)(2)
1111 = Endpoint 15
1110 = Endpoint 14
•
•
•
0001 = Endpoint 1
0000 = Endpoint 0

bit 3 **DIR:** Last Buffer Descriptor Direction Indicator bit
1 = The last transaction was a transmit transfer (TX)
0 = The last transaction was a receive transfer (RX)

bit 2 **PPBI:** Ping-Pong Buffer Descriptor Pointer Indicator bit(1)
1 = The last transaction was to the ODD buffer descriptor bank
0 = The last transaction was to the EVEN buffer descriptor bank

bit 1-0 **Unimplemented:** Read as '0'

Note 1: This bit is only valid for endpoints with available EVEN and ODD buffer descriptor registers.

2: In Host mode, all transactions are processed through Endpoint 0 and the Endpoint 0 BDTs. Therefore, ENDPT<3:0> will always read as '0000'.

REGISTER 23-4: ADxCON3: ADCx CONTROL REGISTER 3

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADRC	—	—	SAMC<4:0>(1)				
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS<7:0>(2,3)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ADRC:** ADC Conversion Clock Source bit
1 = ADC internal RC clock
0 = Clock Derived From System Clock

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits(1)
11111 = 31 TAD
•
•
•
00001 = 1 TAD
00000 = 0 TAD

bit 7-0 **ADCS<7:0>:** ADC Conversion Clock Select bits(2,3)
11111111 = TP • (ADCS<7:0> + 1) = 256 • TCY = TAD
•
•
•
00000010 = TP • (ADCS<7:0> + 1) = 3 • TCY = TAD
00000001 = TP • (ADCS<7:0> + 1) = 2 • TCY = TAD
00000000 = TP • (ADCS<7:0> + 1) = 1 • TCY = TAD

Note 1: This bit is only used if ADxCON1<7:5> (SSRC<2:0>) = 111 and ADxCON1<4> (SSRCG) = 0.
2: This bit is not used if ADxCON3<15> (ADRC) = 1.
3: TP = 1/FP.

REGISTER 23-7: ADxCHS0: ADCx INPUT CHANNEL 0 SELECT REGISTER

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NB	—	—	CH0SB<4:0>(1)				
bit 15							bit 8

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NA	—	—	CH0SA<4:0>(1)				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CH0NB:** Channel 0 Negative Input Select for Sample B bit
Same definition as bit 7.

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **CH0SB<4:0>:** Channel 0 Positive Input Select for Sample B bits(1)
Same definition as bits<4:0>.

bit 7 **CH0NA:** Channel 0 Negative Input Select for Sample A bit
1 = Channel 0 negative input is AN1
0 = Channel 0 negative input is VREFL

bit 6-5 **Unimplemented:** Read as '0'

bit 4-0 **CH0SA<4:0>:** Channel 0 Positive Input Select for Sample A bits(1)
11111 = Channel 0 positive input is AN31
11110 = Channel 0 positive input is AN30
•
•
•
00010 = Channel 0 positive input is AN2
00001 = Channel 0 positive input is AN1
00000 = Channel 0 positive input is AN0

Note 1: The AN16 through AN31 pins are not available for the ADC2 module. The AN16 through AN23 pins are not available for dsPIC33EP256MU806 (64-pin) devices.

REGISTER 25-4: CMxMSKCON: COMPARATOR x MASK GATING CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **HLMS:** High or Low-Level Masking Select bits
1 = The masking (blanking) function will prevent any asserted (‘0’) comparator signal from propagating
0 = The masking (blanking) function will prevent any asserted (‘1’) comparator signal from propagating

bit 14 **Unimplemented:** Read as '0'

bit 13 **OCEN:** OR Gate C Input Enable bit
1 = MCI is connected to OR gate
0 = MCI is not connected to OR gate

bit 12 **OCNEN:** OR Gate C Input Inverted Enable bit
1 = Inverted MCI is connected to OR gate
0 = Inverted MCI is not connected to OR gate

bit 11 **OBEN:** OR Gate B Input Enable bit
1 = MBI is connected to OR gate
0 = MBI is not connected to OR gate

bit 10 **OBNEN:** OR Gate B Input Inverted Enable bit
1 = Inverted MBI is connected to OR gate
0 = Inverted MBI is not connected to OR gate

bit 9 **OAEN:** OR Gate A Input Enable bit
1 = MAI is connected to OR gate
0 = MAI is not connected to OR gate

bit 8 **OANEN:** OR Gate A Input Inverted Enable bit
1 = Inverted MAI is connected to OR gate
0 = Inverted MAI is not connected to OR gate

bit 7 **NAGS:** AND Gate Output Inverted Enable bit
1 = Inverted ANDI is connected to OR gate
0 = Inverted ANDI is not connected to OR gate

bit 6 **PAGS:** AND Gate Output Enable bit
1 = ANDI is connected to OR gate
0 = ANDI is not connected to OR gate

bit 5 **ACEN:** AND Gate C Input Enable bit
1 = MCI is connected to AND gate
0 = MCI is not connected to AND gate

bit 4 **ACNEN:** AND Gate C Input Inverted Enable bit
1 = Inverted MCI is connected to AND gate
0 = Inverted MCI is not connected to AND gate

26.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS70584) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This chapter discusses the Real-Time Clock and Calendar (RTCC) module and its operation.

Some of the key features of this module are:

- Time: Hours, Minutes and Seconds
- 24-Hour Format (military time)
- Calendar: Weekday, Date, Month and Year
- Alarm Configurable
- Year Range: 2000 to 2099
- Leap Year Correction
- BCD Format for Compact Firmware
- Optimized for Low-Power Operation
- User Calibration with Auto-Adjust
- Calibration Range: ±2.64 Seconds Error per Month
- Requirements: External 32.768 kHz Clock Crystal
- Alarm Pulse or Seconds Clock Output on RTCC Pin

The RTCC module is intended for applications where accurate time must be maintained for extended periods with minimum to no intervention from the CPU. The RTCC module is optimized for low-power usage to provide extended battery lifetime while keeping track of time.

The RTCC module is a 100-year clock and calendar with automatic leap year detection. The range of the clock is from 00:00:00 (midnight) on January 1, 2000 to 23:59:59 on December 31, 2099.

The hours are available in 24-hour (military time) format. The clock provides a granularity of one second with half-second visibility to the user.

REGISTER 26-4: RTCVAL (WHEN RTCPTR<1:0> = 11): YEAR VALUE REGISTER(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
YRTEN<3:0>				YRONE<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-4 **YRTEN<3:0>:** Binary Coded Decimal Value of Year's Tens Digit bits
Contains a value from 0 to 9.

bit 3-0 **YRONE<3:0>:** Binary Coded Decimal Value of Year's Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to the YEAR register is only allowed when RTCWREN = 1.

REGISTER 26-5: RTCVAL (WHEN RTCPTR<1:0> = 10): MONTH AND DAY VALUE REGISTER(1)

U-0	U-0	U-0	R-x	R-x	R-x	R-x	R-x
—	—	—	MTHTEN0	MTHONE<3:0>			
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	DAYTEN<1:0>		DAYONE<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **MTHTEN0:** Binary Coded Decimal Value of Month's Tens Digit bit
Contains a value of 0 or 1.

bit 11-8 **MTHONE<3:0>:** Binary Coded Decimal Value of Month's Ones Digit bits
Contains a value from 0 to 9.

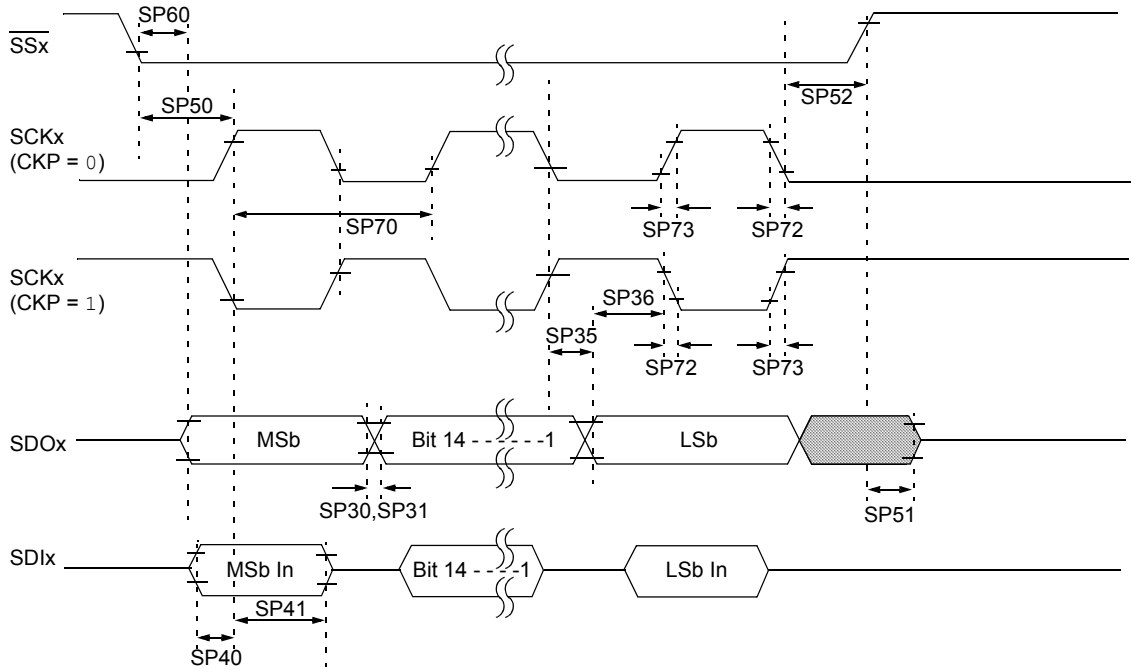
bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DAYTEN<1:0>:** Binary Coded Decimal Value of Day's Tens Digit bits
Contains a value from 0 to 3.

bit 3-0 **DAYONE<3:0>:** Binary Coded Decimal Value of Day's Ones Digit bits
Contains a value from 0 to 9.

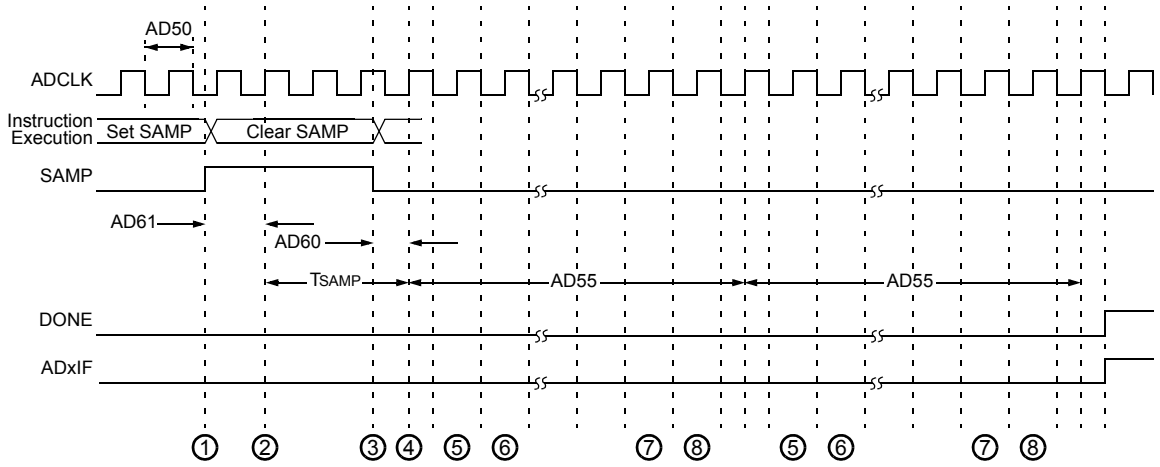
Note 1: A write to this register is only allowed when RTCWREN = 1.

FIGURE 32-27: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 32-1 for load conditions.

FIGURE 32-38: ADC CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (CHPS<1:0> = 01, SIMSAM = 0, ASAM = 0, SSRC<2:0> = 000, SSRCG = 0)



(1) – Software sets ADx1CON1. SAMP to start sampling.

(2) – Sampling starts after discharge period. TSAMP is described in **Section 16. "Analog-to-Digital Converter (ADC)"** (DS70621) of the *"dsPIC33E/PIC24E Family Reference Manual"*.

(3) – Software clears ADxCON1. SAMP to start conversion.

(4) – Sampling ends, conversion sequence starts.

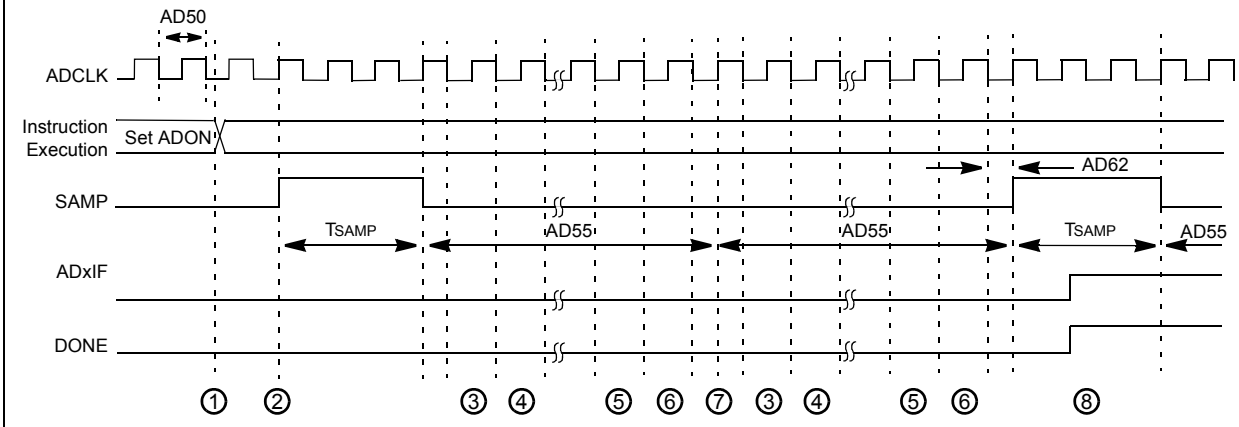
(5) – Convert bit 9.

(6) – Convert bit 8.

(7) – Convert bit 0.

(8) – One TAD for end of conversion.

FIGURE 32-39: ADC CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (CHPS<1:0> = 01, SIMSAM = 0, ASAM = 1, SSRC<2:0> = 111, SSRCG = 0, SAMC<4:0> = 00010)



(1) – Software sets ADxCON1. ADON to start AD operation.

(2) – Sampling starts after discharge period. TSAMP is described in **Section 16. "Analog-to-Digital Converter (ADC)"** (DS70621) of the *"dsPIC33E/PIC24E Family Reference Manual"*.

(3) – Convert bit 9.

(4) – Convert bit 8.

(5) – Convert bit 0.

(6) – One TAD for end of conversion.

(7) – Begin conversion of next channel.

(8) – Sample for time specified by SAMC<4:0>.

TABLE 32-60: DCI MODULE (AC-LINK MODE) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1,2)**	**Min.**	**Typ.(3)**	**Max.**	**Units**	**Conditions**
CS60	TBCLKL	BIT_CLK Low Time	36	40.7	45	ns	
CS61	TBCLKH	BIT_CLK High Time	36	40.7	45	ns	
CS62	TBCLK	BIT_CLK Period	—	81.4	—	ns	Bit clock is input
CS65	TSACL	Input Setup Time to Falling Edge of BIT_CLK	—	—	10	ns	
CS66	THACL	Input Hold Time from Falling Edge of BIT_CLK	—	—	10	ns	
CS70	TSYNCLO	Sync Data Output Low Time	—	19.5	—	µs	
CS71	TSYNCHI	Sync Data Output High Time	—	1.3	—	µs	
CS72	TSYNC	Sync Data Output Period	—	20.8	—	µs	
CS77	TRACL	Rise Time, Sync, SDATA_OUT	—	—	—	ns	See Parameter DO32
CS78	TFACL	Fall Time, Sync, SDATA_OUT	—	—	—	ns	See Parameter DO31
CS80	TOVDACL	Output Valid Delay from Rising Edge of BIT_CLK	—	—	15	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: These values assume the BIT_CLK frequency is 12.288 MHz.

3: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.