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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	122
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256mu814-i-pl

NOTES:

The diagram illustrates a power converter system controlled by a **dsPIC33EP** microcontroller. The system includes the following components and connections:

- dsPIC33EP Microcontroller:** The central control unit, featuring an **ADC Channel**, **Comparator**, **PWM**, **Comparator**, **PWM**, **Comparator**, and **ADC Channel** blocks.
- Power Stage:**
 - Input:** A three-phase AC supply **VAC** is connected to a three-phase bridge rectifier.
 - DC Link:** The rectifier output is connected to a DC link consisting of a capacitor and a resistor.
 - Inverter:** The DC link is connected to a three-phase inverter bridge, which is driven by two **FET Driver** blocks.
 - Output:** The inverter output is connected to a three-phase load, which is a series combination of an inductor and a diode.
- Control and Feedback:**
 - Feedback:** The output voltage **VOUT** is measured and fed back to the **ADC Channel** of the **dsPIC33EP**.
 - Reference:** A reference voltage **VREF** is provided to the **Comparator** block of the **dsPIC33EP**.
 - Control:** The **dsPIC33EP** generates **PWM** signals that are sent to the **FET Driver** blocks to control the inverter.

3.7 CPU Control Registers

REGISTER 3-1: SR: CPU STATUS REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R -0	R/W-0
OA ⁽¹⁾	OB ⁽¹⁾	SA ^(1,4)	SB ^(1,4)	OAB ⁽¹⁾	SAB ⁽¹⁾	DA ⁽¹⁾	DC
bit 15							bit 8

R/W-0 ^(2,3)	R/W-0 ^(2,3)	R/W-0 ^(2,3)	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL<2:0>			RA	N	OV	Z	C
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	W = Writable bit	C = Clearable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **OA:** Accumulator A Overflow Status bit⁽¹⁾
 1 = Accumulator A has overflowed
 0 = Accumulator A has not overflowed
- bit 14 **OB:** Accumulator B Overflow Status bit⁽¹⁾
 1 = Accumulator B has overflowed
 0 = Accumulator B has not overflowed
- bit 13 **SA:** Accumulator A Saturation 'Sticky' Status bit^(1,4)
 1 = Accumulator A is saturated or has been saturated at some time
 0 = Accumulator A is not saturated
- bit 12 **SB:** Accumulator B Saturation 'Sticky' Status bit^(1,4)
 1 = Accumulator B is saturated or has been saturated at some time
 0 = Accumulator B is not saturated
- bit 11 **OAB:** OA || OB Combined Accumulator Overflow Status bit⁽¹⁾
 1 = Accumulators A or B have overflowed
 0 = Neither Accumulators A or B have overflowed
- bit 10 **SAB:** SA || SB Combined Accumulator 'Sticky' Status bit⁽¹⁾
 1 = Accumulators A or B are saturated or have been saturated at some time
 0 = Neither Accumulator A or B are saturated
- bit 9 **DA:** DO Loop Active bit⁽¹⁾
 1 = DO loop in progress
 0 = DO loop not in progress
- bit 8 **DC:** MCU ALU Half Carry/Borrow bit
 1 = A carry-out from the 4th low order bit (for byte-sized data) or 8th low order bit (for word-sized data) of the result occurred
 0 = No carry-out from the 4th low order bit (for byte-sized data) or 8th low order bit (for word-sized data) of the result occurred

- Note 1:** This bit is available on dsPIC33EPXXX(GP/MC/MU)806/810/814 devices only.
- Note 2:** The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1.
- Note 3:** The IPL<2:0> bits are read-only when NSTDIS = 1 (INTCON1<15>).
- Note 4:** A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.

TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMU806 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	NVMIF	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	IC8IF	IC7IF	AD2IF	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	T6IF	DMA4IF	PMPIF	OC8IF	OC7IF	OC6IF	OC5IF	IC6IF	IC5IF	IC4IF	IC3IF	DMA3IF	C1IF	C1RXIF	SPI2IF	SPI2EIF	0000
IFS3	0806	—	RTCIF	DMA5IF	DCIIF	DCIEIF	QE11IF	PSEMIIF	C2IF	C2RXIF	INT4IF	INT3IF	T9IF	T8IF	MI2C2IF	SI2C2IF	T7IF	0000
IFS4	0808	—	—	—	—	QE12IF	—	PSESMIF	—	C2TXIF	C1TXIF	DMA7IF	DMA6IF	CRCIF	U2EIF	U1EIF	—	0000
IFS5	080A	PWM2IF	PWM1IF	IC9IF	OC9IF	SPI3IF	SPI3EIF	U4TXIF	U4RXIF	U4EIF	USB1IF	—	—	U3TXIF	U3RXIF	U3EIF	—	0000
IFS6	080C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM4IF	PWM3IF	0000
IFS7	080E	IC11IF	OC11IF	IC10IF	OC10IF	SPI4IF	SPI4EIF	DMA11IF	DMA10IF	DMA9IF	DMA8IF	—	—	—	—	—	—	0000
IFS8	0810	—	ICDIF	IC16IF	OC16IF	IC15IF	OC15IF	IC14IF	OC14IF	IC13IF	OC13IF	—	DMA14IF	DMA13IF	DMA12IF	IC12IF	OC12IF	0000
IEC0	0820	NVMIE	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	IC8IE	IC7IE	AD2IE	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	T6IE	DMA4IE	PMPIE	OC8IE	OC7IE	OC6IE	OC5IE	IC6IE	IC5IE	IC4IE	IC3IE	DMA3IE	C1IE	C1RXIE	SPI2IE	SPI2EIE	0000
IEC3	0826	—	RTCIE	DMA5IE	DCIIE	DCIEIE	QE11IE	PSEMIIE	C2IE	C2RXIE	INT4IE	INT3IE	T9IE	T8IE	MI2C2IE	SI2C2IE	T7IE	0000
IEC4	0828	—	—	—	—	QE12IE	—	PSESMIE	—	C2TXIE	C1TXIE	DMA7IE	DMA6IE	CRCIE	U2EIE	U1EIE	—	0000
IEC5	082A	PWM2IE	PWM1IE	IC9IE	OC9IE	SPI3IE	SPI3EIE	U4TXIE	U4RXIE	U4EIE	USB1IE	—	—	U3TXIE	U3RXIE	U3EIE	—	0000
IEC6	082C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM4IE	PWM3IE	0000
IEC7	082E	IC11IE	OC11IE	IC10IE	OC10IE	SPI4IE	SPI4EIE	DMA11IE	DMA10IE	DMA9IE	DMA8IE	—	—	—	—	—	—	0000
IEC8	0830	—	ICDIE	IC16IE	OC16IE	IC15IE	OC15IE	IC14IE	OC14IE	IC13IE	OC13IE	—	DMA14IE	DMA13IE	DMA12IE	IC12IE	OC12IE	0000
IPC0	0840	—	T1IP<2:0>			—	OC1IP<2:0>			—	IC1IP<2:0>			—	INT0IP<2:0>			4444
IPC1	0842	—	T2IP<2:0>			—	OC2IP<2:0>			—	IC2IP<2:0>			—	DMA0IP<2:0>			4444
IPC2	0844	—	U1RXIP<2:0>			—	SPI1IP<2:0>			—	SPI1EIP<2:0>			—	T3IP<2:0>			4444
IPC3	0846	—	NVMIP<2:0>			—	DMA1IP<2:0>			—	AD1IP<2:0>			—	U1TXIP<2:0>			4444
IPC4	0848	—	CNIP<2:0>			—	CMIP<2:0>			—	MI2C1IP<2:0>			—	SI2C1IP<2:0>			4444
IPC5	084A	—	IC8IP<2:0>			—	IC7IP<2:0>			—	AD2IP<2:0>			—	INT1IP<2:0>			4444
IPC6	084C	—	T4IP<2:0>			—	OC4IP<2:0>			—	OC3IP<2:0>			—	DMA2IP<2:0>			4444
IPC7	084E	—	U2TXIP<2:0>			—	U2RXIP<2:0>			—	INT2IP<2:0>			—	T5IP<2:0>			4444
IPC8	0850	—	C1IP<2:0>			—	C1RXIP<2:0>			—	SPI2IP<2:0>			—	SPI2EIP<2:0>			4444
IPC9	0852	—	IC5IP<2:0>			—	IC4IP<2:0>			—	IC3IP<2:0>			—	DMA3IP<2:0>			4444
IPC10	0854	—	OC7IP<2:0>			—	OC6IP<2:0>			—	OC5IP<2:0>			—	IC6IP<2:0>			4444
IPC11	0856	—	T6IP<2:0>			—	DMA4IP<2:0>			—	PMPIP<2:0>			—	OC8IP<2:0>			4444
IPC12	0858	—	T8IP<2:0>			—	MI2C2IP<2:0>			—	SI2C2IP<2:0>			—	T7IP<2:0>			4444
IPC13	085A	—	C2RXIP<2:0>			—	INT4IP<2:0>			—	INT3IP<2:0>			—	T9IP<2:0>			4444
IPC14	085C	—	DCIEIP<2:0>			—	QE11IP<2:0>			—	PSEMIP<2:0>			—	C2IP<2:0>			4444
IPC15	085E	—	—	—	—	—	RTCIP<2:0>			—	DMA5IP<2:0>			—	DCIIP<2:0>			0444

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-54: DMAC REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
DMA0CON	0B00	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000	
DMA0REQ	0B02	FORCE	—	—	—	—	—	—	—	IRQSEL<7:0>									00FF
DMA0STAL	0B04	STA<15:0>																	0000
DMA0STAH	0B06	—	—	—	—	—	—	—	—	STA<23:16>									0000
DMA0STBL	0B08	STB<15:0>																	0000
DMA0STBH	0B0A	—	—	—	—	—	—	—	—	STB<23:16>									0000
DMA0PAD	0B0C	PAD<15:0>																	0000
DMA0CNT	0B0E	—	—	CNT<13:0>															0000
DMA1CON	0B10	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000	
DMA1REQ	0B12	FORCE	—	—	—	—	—	—	—	IRQSEL<7:0>									00FF
DMA1STAL	0B14	STA<15:0>																	0000
DMA1STAH	0B16	—	—	—	—	—	—	—	—	STA<23:16>									0000
DMA1STBL	0B18	STB<15:0>																	0000
DMA1STBH	0B1A	—	—	—	—	—	—	—	—	STB<23:16>									0000
DMA1PAD	0B1C	PAD<15:0>																	0000
DMA1CNT	0B1E	—	—	CNT<13:0>															0000
DMA2CON	0B20	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000	
DMA2REQ	0B22	FORCE	—	—	—	—	—	—	—	IRQSEL<7:0>									00FF
DMA2STAL	0B24	STA<15:0>																	0000
DMA2STAH	0B26	—	—	—	—	—	—	—	—	STA<23:16>									0000
DMA2STBL	0B28	STB<15:0>																	0000
DMA2STBH	0B2A	—	—	—	—	—	—	—	—	STB<23:16>									0000
DMA2PAD	0B2C	PAD<15:0>																	0000
DMA2CNT	0B2E	—	—	CNT<13:0>															0000
DMA2CON	0B30	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000	
DMA3REQ	0B32	FORCE	—	—	—	—	—	—	—	IRQSEL<7:0>									00FF
DMA3STAL	0B34	STA<15:0>																	0000
DMA3STAH	0B36	—	—	—	—	—	—	—	—	STA<23:16>									0000
DMA3STBL	0B38	STB<15:0>																	0000
DMA3STBH	0B3A	—	—	—	—	—	—	—	—	STB<23:16>									0000
DMA3PAD	0B3C	PAD<15:0>																	0000
DMA3CNT	0B3E	—	—	CNT<13:0>															0000
DMA4CON	0B40	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000	
DMA4REQ	0B42	FORCE	—	—	—	—	—	—	—	IRQSEL<7:0>									00FF

Legend: × = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 7-1: INTERRUPT VECTOR DETAILS

Interrupt Source	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
				Flag	Enable	Priority
Highest Natural Order Priority						
INT0 – External Interrupt 0	8	0	0x000014	IFS0<0>	IEC0<0>	IPC0<2:0>
IC1 – Input Capture 1	9	1	0x000016	IFS0<1>	IEC0<1>	IPC0<6:4>
OC1 – Output Compare 1	10	2	0x000018	IFS0<2>	IEC0<2>	IPC0<10:8>
T1 – Timer1	11	3	0x00001A	IFS0<3>	IEC0<3>	IPC0<14:12>
DMA0 – DMA Channel 0	12	4	0x00001C	IFS0<4>	IEC0<4>	IPC1<2:0>
IC2 – Input Capture 2	13	5	0x00001E	IFS0<5>	IEC0<5>	IPC1<6:4>
OC2 – Output Compare 2	14	6	0x000020	IFS0<6>	IEC0<6>	IPC1<10:8>
T2 – Timer2	15	7	0x000022	IFS0<7>	IEC0<7>	IPC1<14:12>
T3 – Timer3	16	8	0x000024	IFS0<8>	IEC0<8>	IPC2<2:0>
SPI1E – SPI1 Error	17	9	0x000026	IFS0<9>	IEC0<9>	IPC2<6:4>
SPI1 – SPI1 Transfer Done	18	10	0x000028	IFS0<10>	IEC0<10>	IPC2<10:8>
U1RX – UART1 Receiver	19	11	0x00002A	IFS0<11>	IEC0<11>	IPC2<14:12>
U1TX – UART1 Transmitter	20	12	0x00002C	IFS0<12>	IEC0<12>	IPC3<2:0>
AD1 – ADC1 Convert Done	21	13	0x00002E	IFS0<13>	IEC0<13>	IPC3<6:4>
DMA1 – DMA Channel 1	22	14	0x000030	IFS0<14>	IEC0<14>	IPC3<10:8>
NVM – NVM Write Complete	23	15	0x000032	IFS0<15>	IEC0<15>	IPC3<14:12>
SI2C1 – I2C1 Slave Event	24	16	0x000034	IFS1<0>	IEC1<0>	IPC4<2:0>
MI2C1 – I2C1 Master Event	25	17	0x000036	IFS1<1>	IEC1<1>	IPC4<6:4>
CM – Comparator Combined Event	26	18	0x000038	IFS1<2>	IEC1<2>	IPC4<10:8>
CN – Input Change Interrupt	27	19	0x00003A	IFS1<3>	IEC1<3>	IPC4<14:12>
INT1 – External Interrupt 1	28	20	0x00003C	IFS1<4>	IEC1<4>	IPC5<2:0>
AD2 – ADC2 Convert Done	29	21	0x00003E	IFS1<5>	IEC1<5>	IPC5<6:4>
IC7 – Input Capture 7	30	22	0x000040	IFS1<6>	IEC1<6>	IPC5<10:8>
IC8 – Input Capture 8	31	23	0x000042	IFS1<7>	IEC1<7>	IPC5<14:12>
DMA2 – DMA Channel 2	32	24	0x000044	IFS1<8>	IEC1<8>	IPC6<2:0>
OC3 – Output Compare 3	33	25	0x000046	IFS1<9>	IEC1<9>	IPC6<6:4>
OC4 – Output Compare 4	34	26	0x000048	IFS1<10>	IEC1<10>	IPC6<10:8>
T4 – Timer4	35	27	0x00004A	IFS1<11>	IEC1<11>	IPC6<14:12>
T5 – Timer5	36	28	0x00004C	IFS1<12>	IEC1<12>	IPC7<2:0>
INT2 – External Interrupt 2	37	29	0x00004E	IFS1<13>	IEC1<13>	IPC7<6:4>
U2RX – UART2 Receiver	38	30	0x000050	IFS1<14>	IEC1<14>	IPC7<10:8>
U2TX – UART2 Transmitter	39	31	0x000052	IFS1<15>	IEC1<15>	IPC7<14:12>
SPI2E – SPI2 Error	40	32	0x000054	IFS2<0>	IEC2<0>	IPC8<2:0>
SPI2 – SPI2 Transfer Done	41	33	0x000056	IFS2<1>	IEC2<1>	IPC8<6:4>
C1RX – CAN1 RX Data Ready	42	34	0x000058	IFS2<2>	IEC2<2>	IPC8<10:8>
C1 – CAN1 Event	43	35	0x00005A	IFS2<3>	IEC2<3>	IPC8<14:12>
DMA3 – DMA Channel 3	44	36	0x00005C	IFS2<4>	IEC2<4>	IPC9<2:0>
IC3 – Input Capture 3	45	37	0x00005E	IFS2<5>	IEC2<5>	IPC9<6:4>
IC4 – Input Capture 4	46	38	0x000060	IFS2<6>	IEC2<6>	IPC9<10:8>
IC5 – Input Capture 5	47	39	0x000062	IFS2<7>	IEC2<7>	IPC9<14:12>
IC6 – Input Capture 6	48	40	0x000064	IFS2<8>	IEC2<8>	IPC10<2:0>

Note 1: This interrupt source is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

2: This interrupt source is available on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices only.

REGISTER 8-9: DSADRH: MOST RECENT DMA DATA SPACE HIGH ADDRESS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DSADR<23:16>							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **DSADR<23:16>:** Most Recent DMA Address Accessed by DMA bits

REGISTER 8-10: DSADRL: MOST RECENT DMA DATA SPACE LOW ADDRESS REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DSADR<15:8>							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DSADR<7:0>							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **DSADR<15:0>:** Most Recent DMA Address Accessed by DMA bits

REGISTER 8-12: DMARQC: DMA REQUEST COLLISION STATUS REGISTER (CONTINUED)

- bit 2 **RQCOL2:** Channel 2 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected
- bit 1 **RQCOL1:** Channel 1 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected
- bit 0 **RQCOL0:** Channel 0 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

TABLE 9-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

Oscillator Mode	Oscillator Source	POSCMD<1:0>	FNOSC<2:0>	See Notes
Fast RC Oscillator with Divide-by-N (FRCDIVN)	Internal	xx	111	1, 2
Fast RC Oscillator with Divide-by-16 (FRCDIV16)	Internal	xx	110	1
Low-Power RC Oscillator (LPRC)	Internal	xx	101	1
Secondary (Timer1) Oscillator (SOSC)	Secondary	xx	100	1
Primary Oscillator (HS) with PLL (HSPLL)	Primary	10	011	—
Primary Oscillator (XT) with PLL (XTPLL)	Primary	01	011	—
Primary Oscillator (EC) with PLL (ECPLL)	Primary	00	011	1
Primary Oscillator (HS)	Primary	10	010	—
Primary Oscillator (XT)	Primary	01	010	—
Primary Oscillator (EC)	Primary	00	010	1
Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)	Internal	xx	001	1
Fast RC Oscillator (FRC)	Internal	xx	000	1

Note 1: OSC2 pin function is determined by the OSCIOFNC Configuration bit.

2: This is the default oscillator mode for an unprogrammed (erased) device.

9.2 Oscillator Resources

Many useful resources related to the Oscillator are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310>

9.2.1 KEY RESOURCES

- **Section 7. “Oscillator”** (DS70580) in the “dsPIC33E/PIC24E Family Reference Manual”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related “dsPIC33E/PIC24E Family Reference Manual” Sections
- Development Tools

10.5 Power-Saving Resources

Many useful resources related to Power-Saving features are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310
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10.5.1 KEY RESOURCES

- **Section 9. “Watchdog Timer and Power-Saving Modes”** (DS70615) in the *“dsPIC33E/PIC24E Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *“dsPIC33E/PIC24E Family Reference Manual”* Sections
- Development Tools

10.6 Special Function Registers

Seven registers, PMD1: Peripheral Module Disable Control Register 1 through PMD7: Peripheral Module Disable Control Register 7, are provided for peripheral module control.

REGISTER 11-21: RPNR20: PERIPHERAL PIN SELECT INPUT REGISTER 20

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SCK1R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SDI1R<6:0>						
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'bit 14-8 **SCK1R<6:0>:** Assign SPI1 Clock Input (SCK1) to the Corresponding RPN/RPIn Pin bits
(see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'bit 6-0 **SDI1R<6:0>:** Assign SPI1 Data Input (SDI1) to the Corresponding RPN/RPIn Pin bits
(see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

REGISTER 11-32: RPINR32: PERIPHERAL PIN SELECT INPUT REGISTER 32

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SS4R<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **SS4R<6:0>:** Assign SPI4 Slave Select Input ($\overline{SS4}$) to the Corresponding RPn/RPIn Pin bits
(see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

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0000001 = Input tied to CMP1

0000000 = Input tied to Vss

NOTES:

14.2 Input Capture Control Registers

REGISTER 14-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	ICSIDL	ICTSEL<2:0>			—	—
bit 15						bit 8	

U-0	R/W-0	R/W-0	R/HC/HS-0	R/HC/HS-0	R/W-0	R/W-0	R/W-0
—	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		
bit 7							bit 0

Legend:

R = Readable bit HC = Hardware Clearable bit HS = Hardware Settable bit '0' = Bit is cleared
 -n = Value at POR W = Writable bit U = Unimplemented bit, read as '0'

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **ICSIDL:** Input Capture Stop in Idle Control bit
 1 = Input capture will Halt in CPU Idle mode
 0 = Input capture will continue to operate in CPU Idle mode

bit 12-10 **ICTSEL<12:10>:** Input Capture Timer Select bits
 111 = Peripheral clock (FP) is the clock source of the ICx
 110 = Reserved
 101 = Reserved
 100 = Clock source of T1CLK is the clock source of the ICx (only the synchronous clock is supported)
 011 = Clock source of T5CLK is the clock source of the ICx
 010 = Clock source of T4CLK is the clock source of the ICx
 001 = Clock source of T2CLK is the clock source of the ICx
 000 = Clock source of T3CLK is the clock source of the ICx

bit 9-7 **Unimplemented:** Read as '0'

bit 6-5 **ICI<1:0>:** Number of Captures per Interrupt Select bits (this field is not used if ICM<2:0> = 001 or 111)
 11 = Interrupt on every fourth capture event
 10 = Interrupt on every third capture event
 01 = Interrupt on every second capture event
 00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)
 1 = Input capture buffer overflow occurred
 0 = No input capture buffer overflow occurred

bit 3 **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)
 1 = Input capture buffer is not empty, at least one more capture value can be read
 0 = Input capture buffer is empty

bit 2-0 **ICM<2:0>:** Input Capture Mode Select bits
 111 = Input capture functions as interrupt pin only in CPU Sleep and Idle modes (rising edge detect only, all other control bits are not applicable)
 110 = Unused (module disabled)
 101 = Capture mode, every 16th rising edge (Prescaler Capture mode)
 100 = Capture mode, every 4th rising edge (Prescaler Capture mode)
 011 = Capture mode, every rising edge (Simple Capture mode)
 010 = Capture mode, every falling edge (Simple Capture mode)
 001 = Capture mode, every edge rising and falling (Edge Detect mode (ICI<1:0>) is not used in this mode)
 000 = Input capture module is turned off

REGISTER 22-29: UxFRML: USB FRAME NUMBER LOW REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
FRM<7:0>							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'bit 7-0 **FRM<7:0>:** 11-Bit Frame Number Lower 8 bits

These register bits are updated with the current frame number whenever a SOF token is received.

REGISTER 23-3: AD2CON2: ADC2 CONTROL REGISTER 2 (CONTINUED)

- bit 1 **BUFM:** Buffer Fill Mode Select bit
- 1 = Starts buffer filling the first half of the buffer on the first interrupt and the second half of the buffer on the next interrupt
 - 0 = Always starts filling the buffer from the Start address
- bit 0 **ALTS:** Alternate Input Sample Mode Select bit
- 1 = Uses channel input selects for Sample A on first sample and Sample B on next sample
 - 0 = Always uses channel input selects for Sample A

REGISTER 26-2: PADCFG1: PAD CONFIGURATION CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	RTSECSEL ⁽¹⁾	PMPTTL
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-2 **Unimplemented:** Read as '0'

bit 1 **RTSECSEL:** RTCC Seconds Clock Output Select bit⁽¹⁾

1 = RTCC seconds clock is selected for the RTCC pin

0 = RTCC alarm pulse is selected for the RTCC pin

bit 0 Not used by the RTCC module.

Note 1: To enable the actual RTCC output, the RTCOE bit (RCFGCAL<10>) must be set.

30.0 INSTRUCTION SET SUMMARY

Note: This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the “dsPIC33E/PIC24E Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

The dsPIC33EP instruction set is almost identical to that of the dsPIC30F and dsPIC33F. The PIC24EP instruction set is almost identical to that of the PIC24F and PIC24H.

Most instructions are a single program memory word (24 bits). Only three instructions require two program memory locations.

Each single-word instruction is a 24-bit word, divided into an 8-bit opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction.

The instruction set is highly orthogonal and is grouped into five basic categories:

- Word or byte-oriented operations
- Bit-oriented operations
- Literal operations
- DSP operations
- Control operations

Table 30-1 lists the general symbols used in describing the instructions.

The dsPIC33E instruction set summary in Table 30-2 lists all the instructions, along with the status flags affected by each instruction.

Most word or byte-oriented W register instructions (including barrel shift instructions) have three operands:

- The first source operand, which is typically a register ‘Wb’ without any address modifier
- The second source operand, which is typically a register ‘Ws’ with or without an address modifier
- The destination of the result, which is typically a register ‘Wd’ with or without an address modifier

However, word or byte-oriented file register instructions have two operands:

- The file register specified by the value ‘f’
- The destination, which could be either the file register ‘f’ or the W0 register, which is denoted as ‘WREG’

Most bit-oriented instructions (including simple rotate/shift instructions) have two operands:

- The W register (with or without an address modifier) or file register (specified by the value of ‘Ws’ or ‘f’)
- The bit in the W register or file register (specified by a literal value or indirectly by the contents of register ‘Wb’)

The literal instructions that involve data movement can use some of the following operands:

- A literal value to be loaded into a W register or file register (specified by ‘k’)
- The W register or file register where the literal value is to be loaded (specified by ‘Wb’ or ‘f’)

However, literal instructions that involve arithmetic or logical operations use some of the following operands:

- The first source operand, which is a register ‘Wb’ without any address modifier
- The second source operand, which is a literal value
- The destination of the result (only if not the same as the first source operand), which is typically a register ‘Wd’ with or without an address modifier

The MAC class of DSP instructions can use some of the following operands:

- The accumulator (A or B) to be used (required operand)
- The W registers to be used as the two operands
- The X and Y address space prefetch operations
- The X and Y address space prefetch destinations
- The accumulator write-back destination

The other DSP instructions do not involve any multiplication and can include:

- The accumulator to be used (required)
- The source or destination operand (designated as Wso or Wdo, respectively) with or without an address modifier
- The amount of shift specified by a W register ‘Wn’ or a literal value

The control instructions can use some of the following operands:

- A program memory address
- The mode of the table read and table write instructions

**TABLE 32-38: SPI1, SPI3 AND SPI4 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0)
TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	TscP	Maximum SCKx Input Frequency	—	—	11	MHz	See Note 3
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{\text{SSx}} \downarrow$ to SCKx $\uparrow$ or SCKx $\downarrow$ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{\text{SSx}} \uparrow$ to SDOx Output, High-Impedance	10	—	50	ns	See Note 4
SP52	Tsch2ssH, TscL2ssH	$\overline{\text{SSx}} \uparrow$ after SCKx Edge	$1.5 T_{CY} + 40$	—	—	ns	See Note 4
SP60	TssL2doV	SDOx Data Output Valid after $\overline{\text{SSx}}$ Edge	—	—	50	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCKx is 91 ns. Therefore, the SCKx clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

TABLE 32-63: COMPARATOR REFERENCE VOLTAGE SETTling TIME SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (see Note 3) (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽²⁾	Min.	Typ.	Max.	Units	Conditions
VR310	TSET	Settling Time ⁽¹⁾	—	—	10	μs	

- Note 1:** Setting time measured while CVRR = 1 and CVR<3:0> bits transition from '0000' to '1111'.
- 2:** These parameters are characterized, but not tested in manufacturing.
- 3:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.

TABLE 32-64: COMPARATOR REFERENCE VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (see Note 2) (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
VRD310	CVRES	Resolution	CVRSRC/24	—	CVRSRC/32	LSb	
VRD311	CVRAA	Absolute Accuracy	—	—	0.5	LSb	
VRD312	CVRL	Maximum Load on CVREF Output Pin	—	—	0.75	μA	AVDD = 3.6V, CVRSS = 0, CVRR = 0, CVR<3:0> = 1111

- Note 1:** These parameters are characterized, but not tested in manufacturing.
- 2:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.