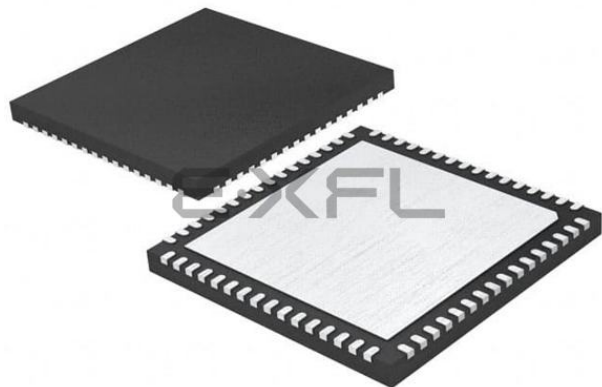




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512gp806-e-mr

TABLE 4-16: PWM GENERATOR 4 REGISTER MAP FOR dsPIC33EPXXX(MC/MU)806/810/814 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
PWMCON4	0C80	FLTSTAT	CLSTAT	TRGSTAT	FLTIEEN	CLIEEN	TRGIEEN	ITB	MDCS	DTC<1:0>		DTCP	—	MTBS	CAM	XPRES	IUE	0000	
IOCON4	0C82	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000	
FCLCON4	0C84	IFLTMOD	CLSRC<4:0>					CLPOL	CLMOD	FLTSRC<4:0>					FLTPOL	FLTMOD<1:0>		0000	
PDC4	0C86	PDC4<15:0>																0000	
PHASE4	0C88	PHASE4<15:0>																0000	
DTR4	0C8A	—	—	DTR4<13:0>														0000	
ALTDTR4	0C8C	—	—	ALTDTR4<13:0>														0000	
SDC4	0C8E	SDC4<15:0>																0000	
SPHASE4	0C90	SPHASE4<15:0>																0000	
TRIG4	0C92	TRGCMP<15:0>																0000	
TRGCON4	0C94	TRGDIV<3:0>				—	—	—	—	—	—	TRGSTRT<5:0>							0000
PWMCAP4	0C98	PWMCAP4<15:0>																0000	
LEBCON4	0C9A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000	
LEBDLY4	0C9C	—	—	—	—	LEB<11:0>												0000	
AUXCON4	0C9E	—	—	—	—	BLANKSEL<3:0>				—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLN	0000	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-17: PWM GENERATOR 5 REGISTER MAP FOR dsPIC33EPXXX(MC/MU)810/814 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets		
PWMCON5	0CA0	FLTSTAT	CLSTAT	TRGSTAT	FLTIEEN	CLIEEN	TRGIEEN	ITB	MDCS	DTC<1:0>		DTCP	—	MTBS	CAM	XPRES	IUE	0000		
IOCON5	0CA2	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000		
FCLCON5	0CA4	IFLTMOD	CLSRC<4:0>					CLPOL	CLMOD	FLTSRC<4:0>					FLTPOL	FLTMOD<1:0>		0000		
PDC5	0CA6	PDC5<15:0>																0000		
PHASE5	0CA8	PHASE5<15:0>																0000		
DTR5	0CAA	—	—	DTR5<13:0>														0000		
ALTDTR5	0CAC	—	—	ALTDTR5<13:0>														0000		
SDC5	0CAE	SDC5<15:0>																0000		
SPHASE5	0CB0	SPHASE5<15:0>																0000		
TRIG5	0CB2	TRGCMP<15:0>																0000		
TRGCON5	0CB4	TRGDIV<3:0>				—	—	—	—	—	—	TRGSTRT<5:0>							0000	
PWMCAP5	0CB8	PWM Capture<15:0>																0000		
LEBCON5	0CBA	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000		
LEBDLY5	0CBC	—	—	—	—	LEB<11:0>														0000
AUXCON5	0CBE	—	—	—	—	BLANKSEL<3:0>				—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLN	0000		

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-20: QE1 REGISTER MAP FOR dsPIC33EPXXX(MC/MU)806/810/814 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
QE1CON	01C0	QE1EN	—	QE1SIDL	PIMOD<2:0>			IMV<1:0>		—	INTDIV<2:0>			CNTPOL	GATEN	CCM<1:0>		0000
QE1IOC	01C2	QCAPEN	FLTREN	QFDIV<2:0>			OUTFNC<1:0>		SWPAB	HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA	000x
QE1STAT	01C4	—	—	PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN	PCIIRQ	PCIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN	0000
POS1CNTL	01C6	POSCNT<15:0>																0000
POS1CNTH	01C8	POSCNT<31:16>																0000
POS1HLD	01CA	POSHLD<15:0>																0000
VEL1CNT	01CC	VELCNT<15:0>																0000
INT1TMRL	01CE	INTTMR<15:0>																0000
INT1TMRH	01D0	INTTMR<31:16>																0000
INT1HLDL	01D2	INTHLD<15:0>																0000
INT1HLDH	01D4	INTHLD<31:16>																0000
INDX1CNTL	01D6	INDXCNT<15:0>																0000
INDX1CNTH	01D8	INDXCNT<31:16>																0000
INDX1HLD	01DA	INDXHLD<15:0>																0000
QE1GECL	01DC	QEIGEC<15:0>																0000
QE1ICL	01DC	QEIIC<15:0>																0000
QE1GECH	01DE	QEIGEC<31:16>																0000
QE1ICH	01DE	QEIIC<31:16>																0000
QE1LECL	01E0	QEILEC<15:0>																0000
QE1LECH	01E2	QEILEC<31:16>																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

5.4 Flash Program Memory Resources

Many useful resources related to Flash program memory are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310>

5.4.1 KEY RESOURCES

- **Section 5. “Flash Programming”** (DS70609) in the *“dsPIC33E/PIC24E Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *“dsPIC33E/PIC24E Family Reference Manual”* Sections
- Development Tools

5.5 Control Registers

Four SFRs are used to read and write the program Flash memory: NVMCON, NVMKEY, NVMADRU and NVMADR.

The NVMCON register (Register 5-1) controls which blocks are to be erased, which memory type is to be programmed and the start of the programming cycle.

NVMKEY (Register 5-4) is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register.

There are two NVM Address registers: NVMADRU and NVMADR. These two registers, when concatenated, form the 24-bit Effective Address (EA) of the selected row or word for programming operations, or the selected page for erase operations.

The NVMADRU register is used to hold the upper 8 bits of the EA, while the NVMADR register is used to hold the lower 16 bits of the EA.

REGISTER 8-14: DMAPPS: DMA PING-PONG STATUS REGISTER (CONTINUED)

- bit 2 **PPST2:** Channel 2 Ping-Pong Mode Status Flag bit
 1 = DMASTB2 register selected
 0 = DMASTA2 register selected
- bit 1 **PPST1:** Channel 1 Ping-Pong Mode Status Flag bit
 1 = DMASTB1 register selected
 0 = DMASTA1 register selected
- bit 0 **PPST0:** Channel 0 Ping-Pong Mode Status Flag bit
 1 = DMASTB0 register selected
 0 = DMASTA0 register selected

REGISTER 9-3: PLLFBD: PLL FEEDBACK DIVISOR REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	PLLDIV<8>
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
PLLDIV<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as '0'

bit 8-0 **PLLDIV<8:0>:** PLL Feedback Divisor bits (also denoted as 'M', PLL multiplier)

11111111 = 513

•

•

•

000110000 = 50 (default)

•

•

•

000000010 = 4

000000001 = 3

000000000 = 2

Note 1: This register is reset only on a Power-on Reset (POR).

**REGISTER 11-13: RPINR12: PERIPHERAL PIN SELECT INPUT REGISTER 12
(dsPIC33EPXXXMU806/810/814 DEVICES ONLY)**

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	FLT2R<6:0> ⁽¹⁾						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	FLT1R<6:0> ⁽¹⁾						
bit 7							bit 0

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **FLT2R<6:0>:** Assign PWM Fault 2 ($\overline{\text{FLT2}}$) to the Corresponding RPN/RPIn Pin bits⁽¹⁾
(see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.
.
.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **FLT1R<6:0>:** Assign PWM Fault 1 ($\overline{\text{FLT1}}$) to the Corresponding RPN/RPIn Pin bits⁽¹⁾
(see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.
.
.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

Note 1: These pins are available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

REGISTER 11-25: RPNR25: PERIPHERAL PIN SELECT INPUT REGISTER 25

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15				bit 8			

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	COFSR<6:0>						
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'bit 6-0 **COFSR<6:0>:** Assign DCI FSYNC Input (COFS) to the Corresponding RPN/RPIn Pin bits
(see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

15.0 OUTPUT COMPARE

Note 1: This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 13. “Output Compare”** (DS70358) of the “dsPIC33E/PIC24E Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

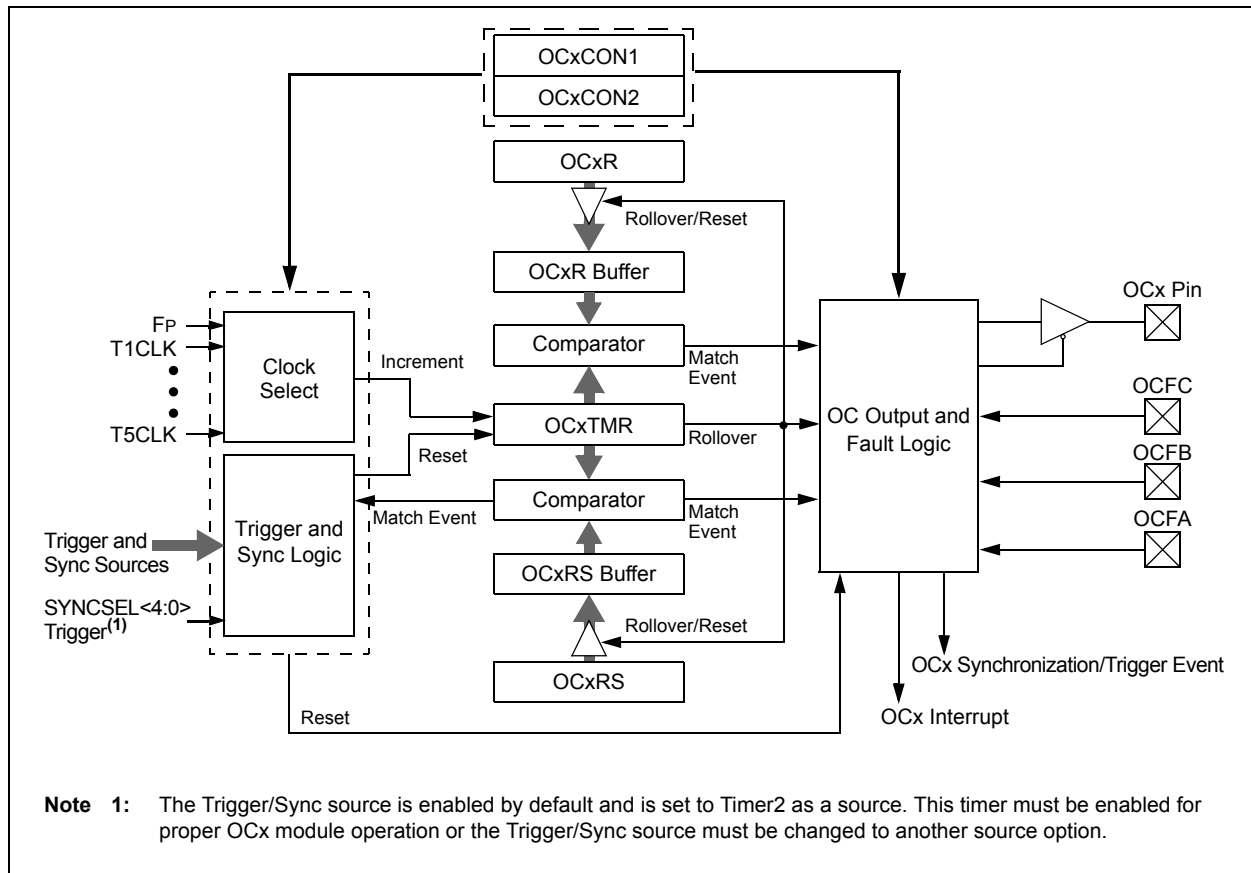
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The output compare module can select one of eight available clock sources for its time base. The module compares the value of the timer with the value of one or two Compare registers, depending on the operating mode selected. The state of the output pin changes when the timer value matches the Compare register value. The output compare module generates either a single output pulse, or a sequence of output pulses, by changing the state of the output pin on the compare match events. The output compare module can also generate interrupts on compare match events.

Note 1: Only OC1, OC2, OC3 and OC4 can trigger a DMA data transfer.

2: See **Section 13. “Output Compare”** (DS70358) in the “dsPIC33E/PIC24E Family Reference Manual” for OCxR and OCxRS register restrictions.

FIGURE 15-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM



REGISTER 16-21: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER (CONTINUED)

bit 7-3	FLTSRC<4:0>: Fault Control Signal Source Select bits for PWM Generator #^(2,3) 11111 = Reserved • • • 01011 = Reserved 01010 = Comparator 3 01001 = Comparator 2 01000 = Comparator 1 00111 = Reserved 00110 = Fault 7 00101 = Fault 6 00100 = Fault 5 00011 = Fault 4 00010 = Fault 3 00001 = Fault 2 00000 = Fault 1
bit 2	FLTPOL: Fault Polarity bit for PWM Generator #⁽¹⁾ 1 = The selected Fault source is active-low 0 = The selected Fault source is active-high
bit 1-0	FLTMOD<1:0>: Fault Mode bits for PWM Generator # 11 = Fault input is disabled 10 = Reserved 01 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (cycle) 00 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (latched condition)

- Note 1:** These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.
- 2:** When Independent Fault mode is enabled (IFLTMOD = 1) and Fault 1 is used for Fault mode (FLTSRC<4:0> = 01000), the Current-Limit Control Source Select bits (CLSRC<4:0>) should be set to an unused current-limit source to prevent the current-limit source from disabling both the PWMxH and PWMxL outputs.
- 3:** When Independent Fault mode is enabled (IFLTMOD = 1) and Fault 1 is used for Current-Limit mode (CLSRC<4:0> = 01000), the Fault Control Source Select bits (FLTSRC<4:0>) should be set to an unused Fault source to prevent Fault 1 from disabling both the PWMxL and PWMxH outputs.

17.0 QUADRATURE ENCODER INTERFACE (QEI) MODULE (dsPIC33EPXXX(MC/MU)8XX DEVICES ONLY)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. “Quadrature Encoder Interface (QEI)”** (DS70601) of the “*dsPIC33E/PIC24E Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

This chapter describes the Quadrature Encoder Interface (QEI) module and associated operational modes. The QEI module provides the interface to incremental encoders for obtaining mechanical position data.

The operational features of the QEI module include:

- 32-Bit Position Counter
- 32-Bit Index Pulse Counter
- 32-Bit Interval Timer
- 16-Bit Velocity Counter
- 32-Bit Position Initialization/Capture/Compare High Register
- 32-Bit Position Compare Low Register
- x4 Quadrature Count mode
- External Up/Down Count mode
- External Gated Count mode
- External Gated Timer mode
- Internal Timer mode

Figure 17-1 illustrates the QEI block diagram.

Note: An ‘x’ used in the names of pins, control/status bits and registers denotes a particular Quadrature Encoder Interface (QEI) module number (x = 1 or 2).

REGISTER 20-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

bit 4	URXINV: Receive Polarity Inversion bit 1 = UxRX Idle state is '0' 0 = UxRX Idle state is '1'
bit 3	BRGH: High Baud Rate Enable bit 1 = BRG generates 4 clocks per bit period (4x baud clock, High-Speed mode) 0 = BRG generates 16 clocks per bit period (16x baud clock, Standard mode)
bit 2-1	PDSEL<1:0>: Parity and Data Selection bits 11 = 9-bit data, no parity 10 = 8-bit data, odd parity 01 = 8-bit data, even parity 00 = 8-bit data, no parity
bit 0	STSEL: Stop Bit Selection bit 1 = Two Stop bits 0 = One Stop bit

- Note 1:** Refer to **Section 17. “UART”** (DS70582) in the “*dsPIC33E/PIC24E Family Reference Manual*” for information on enabling the UARTx module for receive or transmit operation.
- 2:** This feature is only available for the 16x BRG mode (BRGH = 0).

REGISTER 21-10: CxCFG2: ECANx BAUD RATE CONFIGURATION REGISTER 2

U-0	R/W-x	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	WAKFIL	—	—	—	SEG2PH<2:0>		
bit 15						bit 8	

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SEG2PHTS	SAM	SEG1PH<2:0>			PRSEG<2:0>		
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **WAKFIL:** Select CAN Bus Line Filter for Wake-up bit

1 = Uses CAN bus line filter for wake-up

0 = CAN bus line filter is not used for wake-up

bit 13-11 **Unimplemented:** Read as '0'

bit 10-8 **SEG2PH<2:0>:** Phase Segment 2 bits

111 = Length is 8 x T_Q

•

•

•

000 = Length is 1 x T_Q

bit 7 **SEG2PHTS:** Phase Segment 2 Time Select bit

1 = Freely programmable

0 = Maximum of SEG1PH bits or Information Processing Time (IPT), whichever is greater

bit 6 **SAM:** Sample of the CAN Bus Line bit

1 = Bus line is sampled three times at the sample point

0 = Bus line is sampled once at the sample point

bit 5-3 **SEG1PH<2:0>:** Phase Segment 1 bits

111 = Length is 8 x T_Q

•

•

•

000 = Length is 1 x T_Q

bit 2-0 **PRSEG<2:0>:** Propagation Time Segment bits

111 = Length is 8 x T_Q

•

•

•

000 = Length is 1 x T_Q

REGISTER 23-3: AD2CON2: ADC2 CONTROL REGISTER 2 (CONTINUED)

- bit 1 **BUFM:** Buffer Fill Mode Select bit
- 1 = Starts buffer filling the first half of the buffer on the first interrupt and the second half of the buffer on the next interrupt
 - 0 = Always starts filling the buffer from the Start address
- bit 0 **ALTS:** Alternate Input Sample Mode Select bit
- 1 = Uses channel input selects for Sample A on first sample and Sample B on next sample
 - 0 = Always uses channel input selects for Sample A

**REGISTER 26-1: RCFGAL: RTCC CALIBRATION AND CONFIGURATION
REGISTER⁽¹⁾ (CONTINUED)**

bit 7-0 **CAL<7:0>**: RTCC Drift Calibration bits
01111111 = Maximum positive adjustment; adds 508 RTCC clock pulses every one minute
•
•
•
00000001 = Minimum positive adjustment; adds four RTCC clock pulses every one minute
00000000 = No adjustment
11111111 = Minimum negative adjustment; subtracts four RTCC clock pulses every one minute
•
•
•
10000000 = Maximum negative adjustment; subtracts 512 RTCC clock pulses every one minute

- Note 1:** The RCFGAL register is only affected by a POR.
2: A write to the RTCEN bit is only allowed when RTCWREN = 1.
3: This bit is read-only. It is cleared when the lower half of the MINSEC register is written.

28.1 PMP Resources

Many useful resources related to PMP are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310
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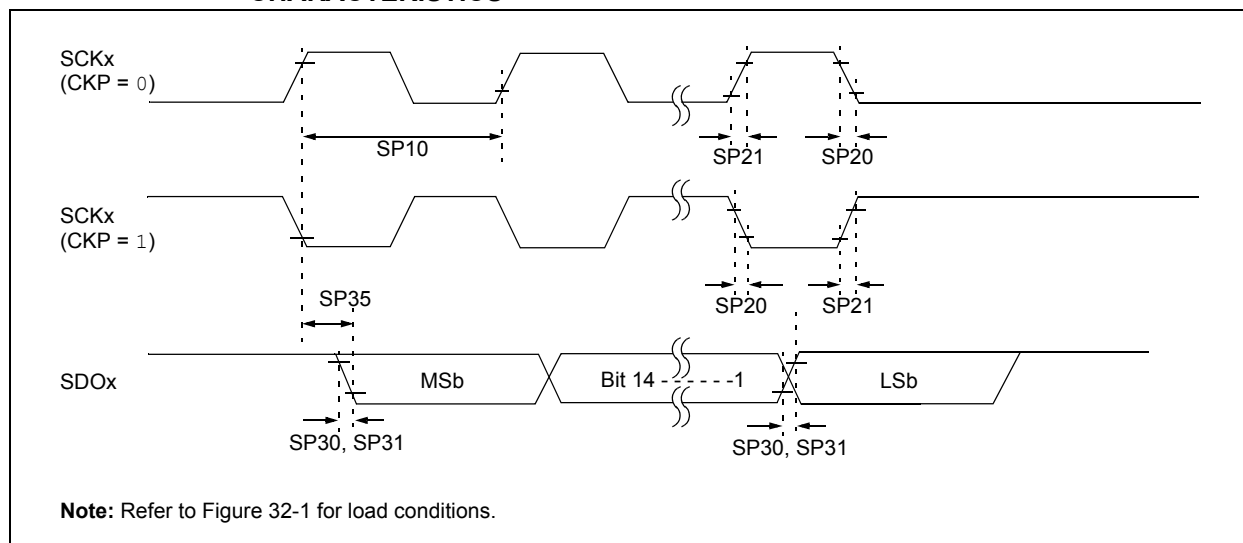
28.1.1 KEY RESOURCES

- **Section 28. “Parallel Master Port (PMP)”** (DS70576) in the *“dsPIC33E/PIC24E Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *“dsPIC33E/PIC24E Family Reference Manual”* Sections
- Development Tools

TABLE 32-41: SPI2 MAXIMUM DATA/CLOCK RATE SUMMARY

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended		
Maximum Data Rate	Master Transmit Only (Half-Duplex)	Master Transmit/Receive (Full-Duplex)	Slave Transmit/Receive (Full-Duplex)	CKE	CKP	SMP
15 MHz	Table 32-42	—	—	0,1	0,1	0,1
10 MHz	—	Table 32-43	—	1	0,1	1
10 MHz	—	Table 32-44	—	0	0,1	1
15 MHz	—	—	Table 32-45	1	0	0
11 MHz	—	—	Table 32-46	1	1	0
15 MHz	—	—	Table 32-47	0	1	0
11 MHz	—	—	Table 32-48	0	0	0

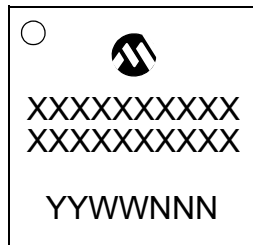
FIGURE 32-23: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS



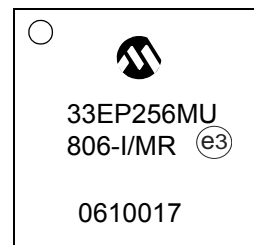
34.0 PACKAGING INFORMATION

34.1 Package Marking Information

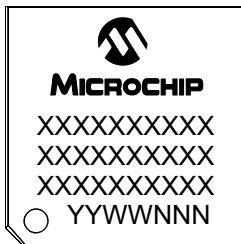
64-Lead QFN (9x9x0.9 mm)



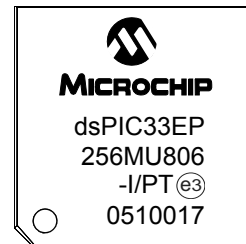
Example



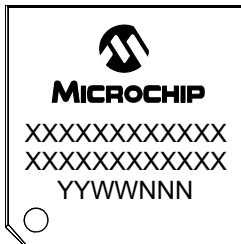
64-Lead TQFP (10x10x1 mm)



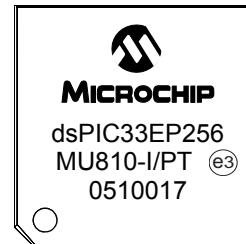
Example



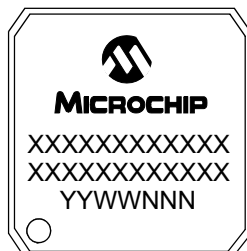
100-Lead TQFP (12x12x1 mm)



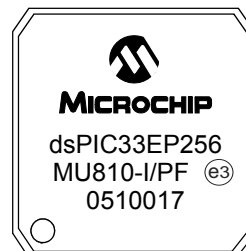
Example



100-Lead TQFP (14x14x1 mm)



Example



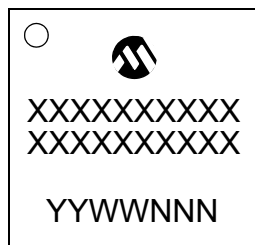
Legend:

XX...X	Customer-specific information
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week '01')
NNN	Alphanumeric traceability code
(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

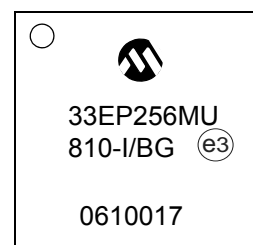
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

34.1 Package Marking Information (Continued)

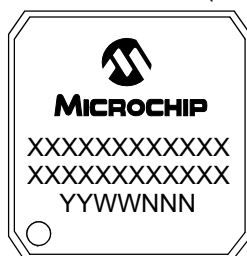
121-Lead TFBGA (10x10x1.2 mm)



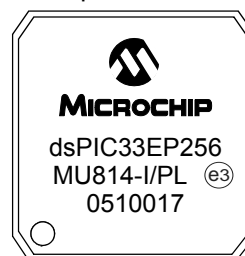
Example



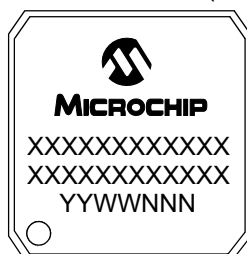
144-Lead LQFP (20x20x1.4 mm)



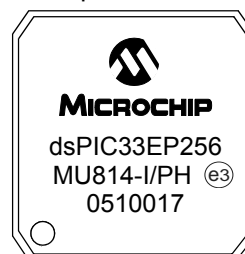
Example



144-Lead TQFP (16x16x1 mm)

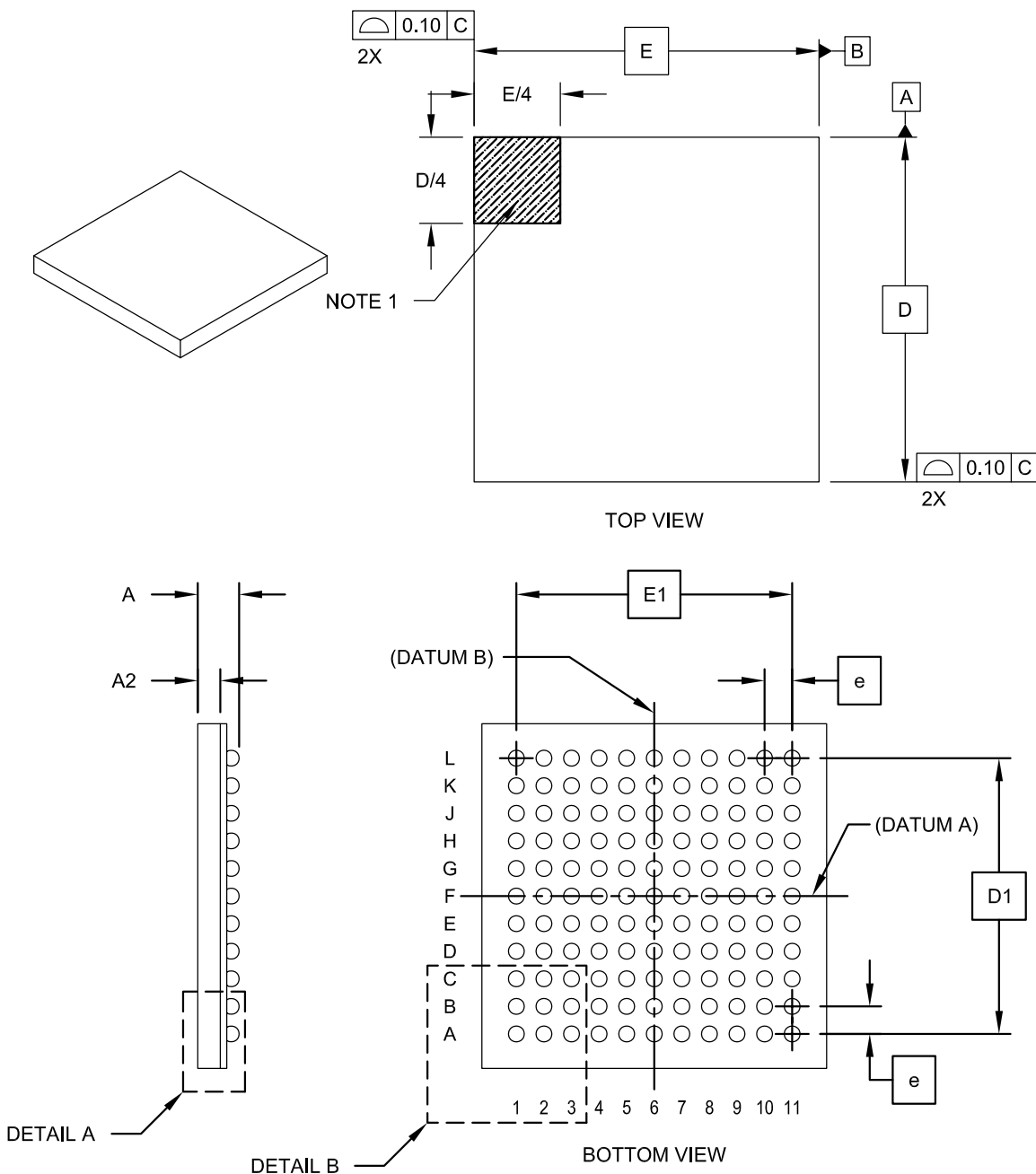


Example



121-Lead Plastic Thin Profile Ball Grid Array (BG) - 10x10x1.10 mm Body [TFBGA—Formerly XBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



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