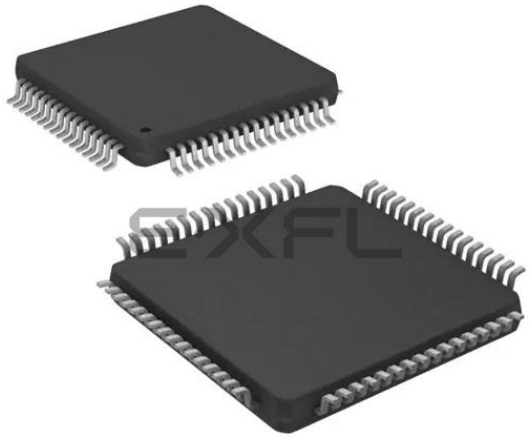
# Microchip Technology - DSPIC33EP512GP806-I/PT Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 70 MIPs |
| Connectivity | CANbus, I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 53 |
| Program Memory Size | 512KB (170K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 24K x 16 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 24x10/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-TQFP |
| Supplier Device Package | 64-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512gp806-i-pt |

**TABLE 2: PIN NAMES: dsPIC33EP256MU810 AND dsPIC33EP512MU810 DEVICES(1,2)**

| Pin Number | Full Pin Name |
|---|---|
| A1 | AN28/PWM3L/PMD4/RP84/RE4 |
| A2 | AN27/PWM2H/PMD3/RPI83/RE3 |
| A3 | RP125/RG13 |
| A4 | AN24/PWM1L/PMD0/RP80/RE0 |
| A5 | RP112/RG0 |
| A6 | VCMPST2/RP97/RF1 |
| A7 | VDD |
| A8 | No Connect |
| A9 | RPI76/RD12 |
| A10 | DPH/RP66/RD2 |
| A11 | VCPCON/RP65/RD1 |
| B1 | No Connect |
| B2 | RP127/RG15 |
| B3 | AN26/PWM2L/PMD2/RP82/RE2 |
| B4 | AN25/PWM1H/PMD1/RPI81/RE1 |
| B5 | AN23/RPI23/RA7 |
| B6 | VCMPST1/RP96/RF0 |
| B7 | VCAP |
| B8 | PMRD/RP69/RD5 |
| B9 | PMBE/RP67/RD3 |
| B10 | VSS |
| B11 | PGEC2/SOSCO/C3IN1-/T1CK/RPI62/RC14 |
| C1 | AN30/PWM4L/PMD6/RPI86/RE6 |
| C2 | VDD |
| C3 | RPI124/RG12 |
| C4 | RP126/RG14 |
| C5 | AN22/RPI22/RA6 |
| C6 | No Connect |
| C7 | C3IN1+/VCMPST3/RP71/RD7 |
| C8 | PMWR/RP68/RD4 |
| C9 | No Connect |
| C10 | PGED2/SOSCI/C3IN3-/RPI61/RC13 |
| C11 | PMCS1/RPI75/RD11 |
| D1 | AN16/PWM5L/RPI49/RC1 |
| D2 | AN31/PWM4H/PMD7/RP87/RE7 |
| D3 | AN29/PWM3H/PMD5/RP85/RE5 |
| D4 | No Connect |
| D5 | No Connect |
| D6 | No Connect |
| D7 | C3IN2-/RP70/RD6 |
| D8 | RPI77/RD13 |
| D9 | INT0/DMH/RP64/RD0 |
| D10 | No Connect |
| D11 | ASCL1(3)/PMCS2/RPI74/RD10 |

| Pin Number | Full Pin Name |
|---|---|
| E8 | RPI31/RA15 |
| E9 | RTCC/DMLN/RPI72/RD8 |
| E10 | ASDA1(3)/DPLN/RPI73/RD9 |
| E11 | RPI30/RA14 |
| F1 | $\overline{\text{MCLR}}$ |
| F2 | C2IN3-/SDO2/PMA3/RP120/RG8 |
| F3 | C2IN1-/PMA2/RPI121/RG9 |
| F4 | C1IN1-/SDI2/PMA4/RPI119/RG7 |
| F5 | VSS |
| F6 | No Connect |
| F7 | No Connect |
| F8 | VDD |
| F9 | OSC1/RPI60/RC12 |
| F10 | VSS |
| F11 | OSC2/CLKO/RC15 |
| G1 | AN20/RPI88/RE8 |
| G2 | AN21/RPI89/RE9 |
| G3 | TMS/RPI16/RA0 |
| G4 | No Connect |
| G5 | VDD |
| G6 | VSS |
| G7 | VSS |
| G8 | No Connect |
| G9 | TDO/RPI21/RA5 |
| G10 | ASDA2(3)/RPI19/RA3 |
| G11 | TDI/RPI20/RA4 |
| H1 | AN5/C1IN1+/VBUSON/VBUSST/RPI37/RB5 |
| H2 | AN4/C1IN2-/USBOEN/RPI36/RB4 |
| H3 | No Connect |
| H4 | No Connect |
| H5 | No Connect |
| H6 | VDD |
| H7 | No Connect |
| H8 | VBUS |
| H9 | VUSB3V3 |
| H10 | D+/RG2(4) |
| H11 | ASCL2(3)/RPI18/RA2 |
| J1 | AN3/C2IN1+/VPIO/RPI35/RB3 |
| J2 | AN2/C2IN2-/VMIO/RPI34/RB2 |
| J3 | PGED1/AN7/RCV/RPI39/RB7 |
| J4 | AVDD |
| J5 | AN11/PMA12/RPI43/RB11 |
| J6 | TCK/RPI17/RA1 |
| J7 | AN12/PMA11/RPI44/RB12 |

**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The availability of $I^2C$™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

**4:** The pin name is SCL1/RG2 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.

**5:** The pin name is SDA1/RG3 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.

**REGISTER 5-2: NVMADRU: NONVOLATILE MEMORY UPPER ADDRESS REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| NVMADRU<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **NVMADRU<7:0>:** Nonvolatile Memory Upper Write Address bits

Selects the upper 8 bits of the location to program or erase in program Flash memory. This register may be read or written by the user application.

**REGISTER 5-3: NVMADR: NONVOLATILE MEMORY ADDRESS REGISTER**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| NVMADR<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| NVMADR<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **NVMADR<15:0>:** Nonvolatile Memory Write Address bits

Selects the lower 16 bits of the location to program or erase in program Flash memory. This register may be read or written by the user application.

**REGISTER 5-4: NVMKEY: NONVOLATILE MEMORY KEY REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
|---|---|---|---|---|---|---|---|
| NVMKEY<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **NVMKEY<7:0>:** Key Register (write-only) bits

**REGISTER 7-5: INTCON3: INTERRUPT CONTROL REGISTER 3**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | UAE | DAE | DOOVR | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-7 **Unimplemented:** Read as '0'

bit 6 **UAE:** USB Address Error Soft Trap Status bit
1 = USB address error (soft) trap has occurred
0 = USB address error (soft) trap has not occurred

bit 5 **DAE:** DMA Address Error Soft Trap Status bit
1 = DMA address error soft trap has occurred
0 = DMA address error soft trap has not occurred

bit 4 **DOOVR:** Do Stack Overflow Soft Trap Status bit
1 = Do stack overflow soft trap has occurred
0 = Do stack overflow soft trap has not occurred

bit 3-0 **Unimplemented:** Read as '0'

**REGISTER 7-6: INTCON4: INTERRUPT CONTROL REGISTER 4**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | SGHT |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-1 **Unimplemented:** Read as '0'

bit 0 **SGHT:** Software Generated Hard Trap Status bit
1 = Software generated hard trap has occurred
0 = Software generated hard trap has not occurred

**REGISTER 8-13: DMALCA: DMA LAST CHANNEL ACTIVE STATUS REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | R-1 | R-1 | R-1 | R-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | LSTCH<3:0> | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-4 **Unimplemented:** Read as '0'

bit 3-0 **LSTCH<3:0>:** Last DMAC Channel Active Status bits

1111 = No DMA transfer has occurred since system Reset
1110 = Last data transfer was handled by Channel 14
1101 = Last data transfer was handled by Channel 13
1100 = Last data transfer was handled by Channel 12
1011 = Last data transfer was handled by Channel 11
1010 = Last data transfer was handled by Channel 10
1001 = Last data transfer was handled by Channel 9
1000 = Last data transfer was handled by Channel 8
0111 = Last data transfer was handled by Channel 7
0110 = Last data transfer was handled by Channel 6
0101 = Last data transfer was handled by Channel 5
0100 = Last data transfer was handled by Channel 4
0011 = Last data transfer was handled by Channel 3
0010 = Last data transfer was handled by Channel 2
0001 = Last data transfer was handled by Channel 1
0000 = Last data transfer was handled by Channel 0

## 10.5 Power-Saving Resources

Many useful resources related to Power-Saving features are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310 |

### 10.5.1 KEY RESOURCES

- **Section 9. "Watchdog Timer and Power-Saving Modes"** (DS70615) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

## 10.6 Special Function Registers

Seven registers, PMD1: Peripheral Module Disable Control Register 1 through PMD7: Peripheral Module Disable Control Register 7, are provided for peripheral module control.

#### 11.4.4.1 Output Mapping

In contrast to inputs, the outputs of the Peripheral Pin Select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Like the RPINRx registers, each register contains sets of 6 bit fields, with each set associated with one RPn pin (see Register 11-44 through Register 11-51). The value of the bit field corresponds to one of the peripherals and that peripheral's output is mapped to the pin (see Table 11-3 and Figure 11-3).

A null output is associated with the Output Register Reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

**FIGURE 11-3: MULTIPLEXING OF REMAPPABLE OUTPUT FOR RPn**

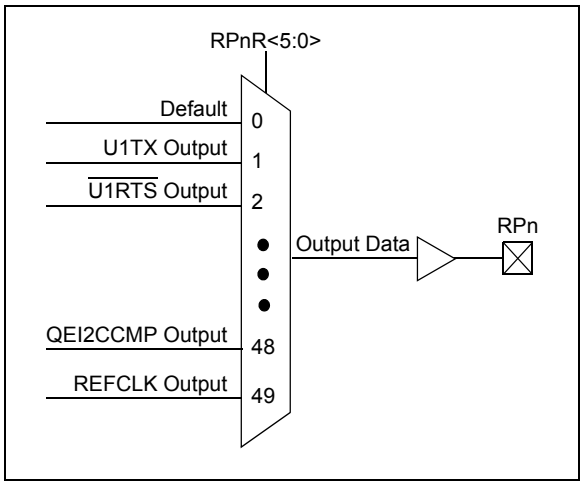



**TABLE 11-3: OUTPUT SELECTION FOR REMAPPABLE PINS (RPn)**

| Function | RPnR<5:0> | Output Name |
|---|---|---|
| DEFAULT PORT | 000000 | RPn tied to Default Pin |
| U1TX | 000001 | RPn tied to UART1 Transmit |
| U1RTS | 000010 | RPn tied to UART1 Ready-to-Send |
| U2TX | 000011 | RPn tied to UART2 Transmit |
| U2RTS | 000100 | RPn tied to UART2 Ready-to-Send |
| SDO1 | 000101 | RPn tied to SPI1 Data Output |
| SCK1 | 000110 | RPn tied to SPI1 Clock Output |
| SS1 | 000111 | RPn tied to SPI1 Slave Select |
| SS2 | 001010 | RPn tied to SPI2 Slave Select |
| CSDO | 001011 | RPn tied to DCI Data Output |
| CSCK | 001100 | RPn tied to DCI Clock Output |
| COFS | 001101 | RPn tied to DCI FSYNC Output |
| C1TX | 001110 | RPn tied to CAN1 Transmit |
| C2TX | 001111 | RPn tied to CAN2 Transmit |
| OC1 | 010000 | RPn tied to Output Compare 1 Output |
| OC2 | 010001 | RPn tied to Output Compare 2 Output |
| OC3 | 010010 | RPn tied to Output Compare 3 Output |
| OC4 | 010011 | RPn tied to Output Compare 4 Output |
| OC5 | 010100 | RPn tied to Output Compare 5 Output |
| OC6 | 010101 | RPn tied to Output Compare 6 Output |
| OC7 | 010110 | RPn tied to Output Compare 7 Output |
| OC8 | 010111 | RPn tied to Output Compare 8 Output |
| C1OUT | 011000 | RPn tied to Comparator Output 1 |
| C2OUT | 011001 | RPn tied to Comparator Output 2 |
| C3OUT | 011010 | RPn tied to Comparator Output 3 |
| U3TX | 011011 | RPn tied to UART3 Transmit |
| U3RTS | 011100 | RPn tied to UART3 Ready-to-Send |

**Note 1:** This function is available in dsPIC33EPXXX(MC/MU)806/810/814 devices only.

**REGISTER 11-4: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | T3CKR<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | T2CKR<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **T3CKR<6:0>:** Assign Timer3 External Clock (T3CK) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **T2CKR<6:0>:** Assign Timer2 External Clock (T2CK) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-25: RPINR25: PERIPHERAL PIN SELECT INPUT REGISTER 25**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | COFSR<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6-0 **COFSR<6:0>:** Assign DCI FSYNC Input (COFS) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-34: RPINR34: PERIPHERAL PIN SELECT INPUT REGISTER 34**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | IC12R<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | IC11R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **IC12R<6:0>:** Assign Input Capture 12 (IC12) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **IC11R<6:0>:** Assign Input Capture 11 (IC11) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

## 19.0 INTER-INTEGRATED CIRCUIT™ ($I^2C$™)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 19. "Inter-Integrated Circuit™ ($I^2C$™)"** (DS70330) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 family of devices contain two Inter-Integrated Circuit ($I^2C$) modules: I2C1 and I2C2.

The $I^2C$ module provides complete hardware support for both Slave and Multi-Master modes of the $I^2C$ serial communication standard, with a 16-bit interface.

The $I^2C$ module has a 2-pin interface:

- The SCLx pin is the clock.
- The SDAx pin is the data.

The $I^2C$ module offers the following key features:

- $I^2C$ interface supporting both Master and Slave modes of operation.
- $I^2C$ Slave mode supports 7 and 10-bit addressing.
- $I^2C$ Master mode supports 7 and 10-bit addressing.
- $I^2C$ port allows bidirectional transfers between master and slaves.
- Serial clock synchronization for $I^2C$ port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control).
- $I^2C$ supports multi-master operation, detects bus collision and arbitrates accordingly.
- IPMI support
- SMBus support

## 19.1 I²C Resources

Many useful resources related to I²C are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310 |

### 19.1.1 KEY RESOURCES

- **Section 19. "Inter-Integrated Circuit™ (I²C™)"** (DS70330) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

**REGISTER 22-2: UxOTGCON: USB ON-THE-GO CONTROL REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| DPPULUP | DMPULUP | DPPULDWN(1) | DMPULDWN(1) | VBUSON(1) | OTGEN(1) | VBUSCHG(1) | VBUSDIS(1) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **DPPULUP:** D+ Pull-Up Enable bit
1 = D+ data line pull-up resistor is enabled
0 = D+ data line pull-up resistor is disabled

bit 6 **DMPULUP:** D- Pull-Up Enable bit
1 = D- data line pull-up resistor is enabled
0 = D- data line pull-up resistor is disabled

bit 5 **DPPULDWN:** D+ Pull-Down Enable bit(1)
1 = D+ data line pull-down resistor is enabled
0 = D+ data line pull-down resistor is disabled

bit 4 **DMPULDWN:** D- Pull-Down Enable bit(1)
1 = D- data line pull-down resistor is enabled
0 = D- data line pull-down resistor is disabled

bit 3 **VBUSON:** VBUS Power-on bit(1)
1 = VBUS line is powered
0 = VBUS line is not powered

bit 2 **OTGEN:** OTG Features Enable bit(1)
1 = USB OTG is enabled; all D+/D- pull-ups and pull-downs are enabled
0 = USB OTG is disabled; D+/D- pull-ups and pull-downs are controlled in hardware by the settings of the HOSTEN and USBEN bits (UxCON<3,0>)

bit 1 **VBUSCHG:** VBUS Charge Selection bit(1)
1 = VBUS line is set to charge to 3.3V
0 = VBUS line is set to charge to 5V

bit 0 **VBUSDIS:** VBUS Discharge Enable bit(1)
1 = VBUS line is discharged through a resistor
0 = VBUS line is not discharged

**Note 1:** These bits are only used in Host mode; do not use in Device mode.

**REGISTER 22-17: UxIE: USB INTERRUPT ENABLE REGISTER (HOST MODE)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| STALLIE | ATTACHIE(1) | RESUMEIE | IDLEIE | TRNIE | SOFIE | UERRIE | DETACHIE |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **STALLIE:** STALL Handshake Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 6 **ATTACHIE:** Peripheral Attach Interrupt bit(1)
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 5 **RESUMEIE:** Resume Interrupt bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 4 **IDLEIE:** Idle Detect Interrupt bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 3 **TRNIE:** Token Processing Complete Interrupt bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 2 **SOFIE:** Start-of-Frame Token Interrupt bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 1 **UERRIE:** USB Error Condition Interrupt bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 0 **DETACHIE:** USB Detach Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

**Note 1:** Unimplemented in OTG mode, read as '0'.

**REGISTER 22-29: UxFRML: USB FRAME NUMBER LOW REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| FRM<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **FRM<7:0>:** 11-Bit Frame Number Lower 8 bits
These register bits are updated with the current frame number whenever a SOF token is received.

## 26.3 RTCC Registers

**REGISTER 26-1: RCFGCAL: RTCC CALIBRATION AND CONFIGURATION REGISTER(1)**

| R/W-0 | U-0 | R/W-0 | R-0 | R-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| RTCEN(2) | — | RTCWREN | RTCSYNC | HALFSEC(3) | RTCOE | RTCPTR<1:0> | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CAL<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **RTCEN:** RTCC Enable bit(2)
1 = RTCC module is enabled
0 = RTCC module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **RTCWREN:** RTCC Value Registers Write Enable bit
1 = RTCVAL register can be written to by the user application
0 = RTCVAL register is locked out from being written to by the user application

bit 12 **RTCSYNC:** RTCC Value Registers Read Synchronization bit
1 = A rollover is about to occur in 32 clock edges (approximately 1 ms)
0 = A rollover will not occur

bit 11 **HALFSEC:** Half-Second Status bit(3)
1 = Second half period of a second
0 = First half period of a second

bit 10 **RTCOE:** RTCC Output Enable bit
1 = RTCC output is enabled
0 = RTCC output is disabled

bit 9-8 **RTCPTR<1:0>:** RTCC Value Register Pointer bits
Points to the corresponding RTCC Value register when reading the RTCVAL register; the RTCPTR<1:0> value decrements on every access of the RTCVAL register until it reaches '00'.

**Note 1:** The RCFGCAL register is only affected by a POR.
**2:** A write to the RTCEN bit is only allowed when RTCWREN = 1.
**3:** This bit is read-only. It is cleared when the lower half of the MINSEC register is written.

## 31.7 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

## 31.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC® Flash MCUs and dsPIC® Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

## 31.9 MPLAB ICD 3 In-Circuit Debugger System

MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost effective high-speed hardware debugger/programmer for Microchip Flash Digital Signal Controller (DSC) and microcontroller (MCU) devices. It debugs and programs PIC® Flash microcontrollers and dsPIC® DSCs with the powerful, yet easy-to-use graphical user interface of MPLAB Integrated Development Environment (IDE).

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

## 31.10 PICkit 3 In-Circuit Debugger/ Programmer and PICkit 3 Debug Express

The MPLAB PICkit 3 allows debugging and programming of PIC® and dsPIC® Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB Integrated Development Environment (IDE). The MPLAB PICkit 3 is connected to the design engineer's PC using a full speed USB interface and can be connected to the target via an Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the reset line to implement in-circuit debugging and In-Circuit Serial Programming™.

The PICkit 3 Debug Express include the PICkit 3, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

# 32.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

## Absolute Maximum Ratings

**(See Note 1)**

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... -0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to $V_{SS}$ **(3)** ..... -0.3V to ($V_{DD}$ + 0.3V)
Voltage on any 5V tolerant pin with respect to $V_{SS}$ when $V_{DD} \geq 3.0V$ **(3)** ..... -0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to Vss when $V_{DD} < 3.0V$ **(3)** ..... -0.3V to 3.6V
Voltage on D+ OR D- pin with respect to $V_{USB3V3}$ ..... -0.3V to ($V_{USB3V3}$ +0.3V)
Voltage on $V_{BUS}$ with respect to $V_{SS}$ ..... -0.3V to +5.5V
Maximum current out of $V_{SS}$ pin ..... 320 mA
Maximum current into $V_{DD}$ pin **(2)** ..... 320 mA
Maximum current sourced/sunk by any 4x I/O pin **(4)** ..... 15 mA
Maximum current sourced/sunk by any 8x I/O pin **(4)** ..... 25 mA
Maximum current sunk by all ports ..... 200 mA
Maximum current sourced by all ports **(2)** ..... 200 mA

**Note 1:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**2:** Maximum allowable current is a function of device maximum power dissipation (see Table 32-2).

**3:** See the **“Pin Diagrams”** section for the 5V tolerant pins.

**4:** Characterized but not tested.

**FIGURE 32-2: EXTERNAL CLOCK TIMING**

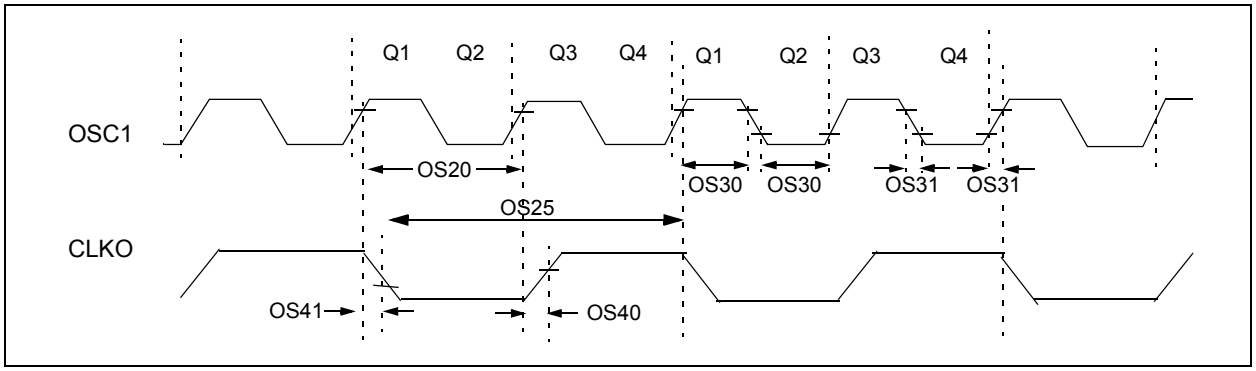



**TABLE 32-16: EXTERNAL CLOCK TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic** | **Min.** | **Typ.(1)** | **Max.** | **Units** | **Conditions** |
| OS10 | FIN | External CLKI Frequency (External clocks allowed only in EC and ECPLL modes) | DC | — | 60 | MHz | EC |
| | | Oscillator Crystal Frequency | 3.5<br>10<br>32.4 | —<br>—<br>32.768 | 10<br>40<br>33.1 | MHz<br>MHz<br>kHz | XT<br>HS<br>SOSC |
| OS20 | TOSC | TOSC = 1/FOSC | 8.33<br>7.14 | —<br>— | DC<br>DC | ns<br>ns | +125ºC<br>+85ºC |
| OS25 | TCY | Instruction Cycle Time(2) | 16.67<br>14.28 | —<br>— | DC<br>DC | ns<br>ns | +125ºC<br>+85ºC |
| OS30 | TosL, TosH | External Clock In (OSC1) High or Low Time | 0.375 x TOSC | — | 0.625 x TOSC | ns | EC |
| OS31 | TosR, TosF | External Clock In (OSC1) Rise or Fall Time | — | — | 20 | ns | EC |
| OS40 | TckR | CLKO Rise Time(3) | — | 5.2 | — | ns | |
| OS41 | TckF | CLKO Fall Time(3) | — | 5.2 | — | ns | |
| OS42 | GM | External Oscillator Transconductance(4) | — | 12 | — | mA/V | HS, VDD = 3.3V, TA = +25ºC |
| | | | — | 6 | — | mA/V | XT, VDD = 3.3V, TA = +25ºC |

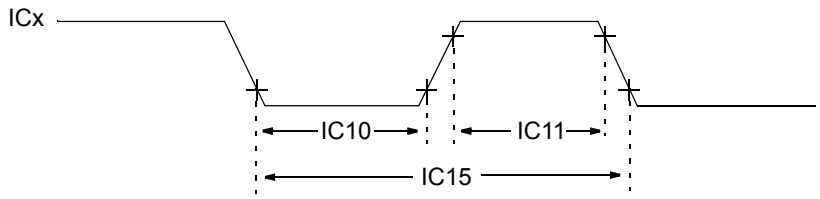
**Note 1:** Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

**2:** Instruction cycle period (TCY) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “Minimum” values with an external clock applied to the OSC1 pin. When an external clock input is used, the “Maximum” cycle time limit is “DC” (no clock) for all devices.

**3:** Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.

**4:** This parameter is characterized, but not tested in manufacturing.

**FIGURE 32-8: INPUT CAPTURE (ICx) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.

**TABLE 32-27: INPUT CAPTURE MODULE (ICx) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristics(1)** | **Min.** | **Max.** | **Units** | **Conditions** | |
| IC10 | TccL | ICx Input Low Time | [Greater of (12.5 or 0.5 TCY)/N] + 25 | — | ns | Must also meet Parameter IC15 | N = prescale value (1, 4, 16) |
| IC11 | TccH | ICx Input High Time | [Greater of (12.5 or 0.5 TCY)/N] + 25 | — | ns | Must also meet Parameter IC15 | |
| IC15 | TccP | ICx Input Period | [Greater of (25 or 1 TCY)/N] + 50 | — | ns | | |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**TABLE A-2: MAJOR SECTION UPDATES (CONTINUED)**

| Section Name | Update Description |
|---|---|
| **Section 21.0 "Enhanced CAN (ECAN™) Module"** | Added the CANCKS bit to the ECAN Control Register 1 (CiCTRL1) (see Register 21-1). |
| **Section 22.0 "USB On-The-Go (OTG) Module"** | Removed the USB 3.3V Regulator logic from the USB Interface Diagram (see Figure 22-1). |
| **Section 23.0 "10-bit/12-bit Analog-to-Digital Converter (ADC)"** | Updated the ADC Conversion Clock Period Block Diagram (see Figure 23-2). |
| **Section 29.0 "Special Features"** | Updated the last paragraph of **Section 29.1 "Configuration Bits"**<br>Added a note box after the last paragraph of **Section 29.3 "BOR: Brown-out Reset (BOR)"**.<br>Added the RTSP Effect column to the Configuration Bits Description (see Table 29-2). |
| **Section 30.0 "Instruction Set Summary"** | Updated all Status Flags Affected to None for the MOV instruction and added Note 2 (see Table 30-2). |
| **Section 32.0 "Electrical Characteristics"** | Updated the Absolute Maximum Ratings (see page 457).<br>Added Note 1 to the Operating MIPS vs. Voltage (see Table 32-1).<br>Added parameter DI31 (ICNPD) to the I/O Pin Input Specifications (see Table 32-9).<br>Updated the Minimum value for parameter DO26 in the I/O Pin Output Specifications (see Table 32-10).<br>Updated the Minimum value for parameter D132b and the Minimum and Maximum values for parameters D136a, D136b, D137a, D137b, D138a, and D138b in the Program Memory specification (see Table 32-12).<br>Updated the Minimum, Typical, and Maximum values for parameter OS10 (Oscillator Crystal Frequency: SOSC) in the External Clock Timing Requirements (see Table 32-16).<br>Added Note 2 to the PLL Clock Timing Specifications (see Table 32-17).<br>Updated all Timer1 External Clock Timing Requirements (see Table 32-23).<br>Replaced Table 32-34 with Timer2, Timer4, Timer6, Timer8 External Clock Timing Requirements and Timer3, Timer5, Timer7, Timer9 External Clock Timing Requirements (see Table 32-24 and Table 32-25, respectively).<br>Updated the Maximum value for parameter OC15 and the Minimum value for parameter OC20 in the OC/PWM Mode Timing Requirements (see Table 32-29).<br>Updated the Operating Temperature in the ECAN Module I/O Timing Requirements and USB OTG Timing Requirements (see Table 32-51 and Table 32-53, respectively).<br>Updated all SPI specifications (see Figure 32-15 through Figure 32-30 and Table 32-33 through Table 32-48).<br>Removed Note 4 from the DCI Module Timing Requirements (see Table 32-59).<br>Updated the Standard Operating Conditions voltage for the Comparator Specifications (see Table 32-61 through Table 32-64). |