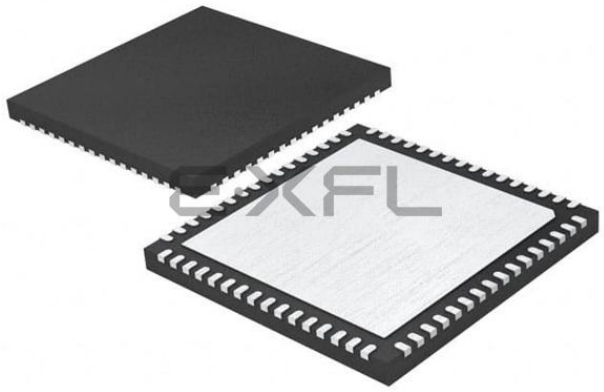
# Microchip Technology - DSPIC33EP512GP806T-I/MR Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 70 MIPs |
| Connectivity | CANbus, I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 53 |
| Program Memory Size | 512KB (170K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 24K x 16 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 24x10/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-VFQFN Exposed Pad |
| Supplier Device Package | 64-VQFN (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512gp806t-i-mr |

## 3.7 CPU Control Registers

**REGISTER 3-1: SR: CPU STATUS REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/C-0 | R/C-0 | R -0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| OA(1) | OB(1) | SA(1,4) | SB(1,4) | OAB(1) | SAB(1) | DA(1) | DC |
| bit 15 | | | | | | | bit 8 |

| R/W-0(2,3) | R/W-0(2,3) | R/W-0(2,3) | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| IPL<2:0> | | | RA | N | OV | Z | C |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | U = Unimplemented bit, read as '0' | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | C = Clearable bit | |
| -n = Value at POR | '1'= Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **OA:** Accumulator A Overflow Status bit(1)
1 = Accumulator A has overflowed
0 = Accumulator A has not overflowed

bit 14 **OB:** Accumulator B Overflow Status bit(1)
1 = Accumulator B has overflowed
0 = Accumulator B has not overflowed

bit 13 **SA:** Accumulator A Saturation 'Sticky' Status bit(1,4)
1 = Accumulator A is saturated or has been saturated at some time
0 = Accumulator A is not saturated

bit 12 **SB:** Accumulator B Saturation 'Sticky' Status bit(1,4)
1 = Accumulator B is saturated or has been saturated at some time
0 = Accumulator B is not saturated

bit 11 **OAB:** OA || OB Combined Accumulator Overflow Status bit(1)
1 = Accumulators A or B have overflowed
0 = Neither Accumulators A or B have overflowed

bit 10 **SAB:** SA || SB Combined Accumulator 'Sticky' Status bit(1)
1 = Accumulators A or B are saturated or have been saturated at some time
0 = Neither Accumulator A or B are saturated

bit 9 **DA:** DO Loop Active bit(1)
1 = DO loop in progress
0 = DO loop not in progress

bit 8 **DC:** MCU ALU Half Carry/$\overline{\text{Borrow}}$ bit
1 = A carry-out from the 4th low order bit (for byte-sized data) or 8th low order bit (for word-sized data) of the result occurred
0 = No carry-out from the 4th low order bit (for byte-sized data) or 8th low order bit (for word-sized data) of the result occurred

**Note 1:** This bit is available on dsPIC33EPXXX(GP/MC/MU)806/810/814 devices only.

**2:** The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1.

**3:** The IPL<2:0> bits are read-only when NSTDIS = 1 (INTCON1<15>).

**4:** A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.


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### 4.2.5 X AND Y DATA SPACES

The dsPIC33EPXXX(GP/MC/MU)806/810/814 core has two data spaces, X and Y. These data spaces can be considered either separate (for some DSP instructions), or as one unified linear address range (for MCU instructions). The data spaces are accessed using two Address Generation Units (AGUs) and separate data paths. This feature allows certain instructions to concurrently fetch two words from RAM, thereby enabling efficient execution of DSP algorithms such as Finite Impulse Response (FIR) filtering and Fast Fourier Transform (FFT).

The PIC24EPXXX(GP/GU)806/810/814 devices do not have a Y data space and a Y AGU. For these devices, the entire data space is treated as X data space.

The X data space is used by all instructions and supports all addressing modes. X data space has separate read and write data buses. The X read data bus is the read data path for all instructions that view data space as combined X and Y address space. It is also the X data prefetch path for the dual operand DSP instructions (`MAC` class).

The Y data space is used in concert with the X data space by the `MAC` class of instructions (`CLR`, `ED`, `EDAC`, `MAC`, `MOVSAC`, `MPY`, `MPY.N` and `MSC`) to provide two concurrent data read paths.

Both the X and Y data spaces support Modulo Addressing mode for all instructions, subject to addressing mode restrictions. Bit-Reversed Addressing mode is only supported for writes to X data space. Modulo Addressing and Bit-Reversed Addressing are not present in PIC24EPXXX(GP/GU)806/810/814 devices.

All data memory writes, including in DSP instructions, view data space as combined X and Y address space. The boundary between the X and Y data spaces is device-dependent and is not user-programmable.

### 4.2.6 DMA RAM

Each dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 device contains 4 Kbytes of dual ported DMA RAM located at the end of Y data RAM and is part of Y data space. Memory locations in the DMA RAM space are accessible simultaneously by the CPU and the DMA Controller module. DMA RAM is utilized by the DMA controller to store data to be transferred to various peripherals using DMA, as well as data transferred from various peripherals using DMA. The DMA RAM can be accessed by the DMA controller without having to steal cycles from the CPU.

When the CPU and the DMA controller attempt to concurrently write to the same DMA RAM location, the hardware ensures that the CPU is given precedence in accessing the DMA RAM location. Therefore, the DMA RAM provides a reliable means of transferring DMA data without ever having to stall the CPU.

**Note 1:** DMA RAM can be used for general purpose data storage if the DMA function is not required in an application.

**2:** On PIC24EPXXX(GP/GU)806/810/814 devices, DMA RAM is located at the end of X data RAM and is part of X data space.

## 4.3 Program Memory Resources

Many useful resources related to the Program Memory are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser:
http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310

### 4.3.1 KEY RESOURCES

- **Section 4. "Program Memory"** (DS70612) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

## 4.4 Special Function Register Maps

Table 4-1 through Table 4-72 provide mapping tables for all Special Function Registers (SFRs).


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**TABLE 4-4: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMU810 DEVICES ONLY (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IPC16 | 0860 | — | CRCIP<2:0> | | | — | U2EIP<2:0> | | | — | U1EIP<2:0> | | | — | — | — | — | 4440 |
| IPC17 | 0862 | — | C2TXIP<2:0> | | | — | C1TXIP<2:0> | | | — | DMA7IP<2:0> | | | — | DMA6IP<2:0> | | | 4444 |
| IPC18 | 0864 | — | QEI2IP<2:0> | | | — | — | — | — | — | PSESMIP<2:0> | | | — | — | — | — | 4040 |
| IPC20 | 0868 | — | U3TXIP<2:0> | | | — | U3RXIP<2:0> | | | — | U3EIP<2:0> | | | — | — | — | — | 4440 |
| IPC21 | 086A | — | U4EIP<2:0> | | | — | USB1IP<2:0> | | | — | — | — | — | — | — | — | — | 4400 |
| IPC22 | 086C | — | SPI3IP<2:0> | | | — | SPI3EIP<2:0> | | | — | U4TXIP<2:0> | | | — | U4RXIP<2:0> | | | 4444 |
| IPC23 | 086E | — | PWM2IP<2:0> | | | — | PWM1IP<2:0> | | | — | IC9IP<2:0> | | | — | OC9IP<2:0> | | | 4444 |
| IPC24 | 0870 | — | PWM6IP<2:0> | | | — | PWM5IP<2:0> | | | — | PWM4IP<2:0> | | | — | PWM3IP<2:0> | | | 4444 |
| IPC29 | 087A | — | DMA9IP<2:0> | | | — | DMA8IP<2:0> | | | — | — | — | — | — | — | — | — | 4400 |
| IPC30 | 087C | — | SPI4IP<2:0> | | | — | SPI4EIP<2:0> | | | — | DMA11IP<2:0> | | | — | DMA10IP<2:0> | | | 4444 |
| IPC31 | 087E | — | IC11IP<2:0> | | | — | OC11IP<2:0> | | | — | IC10IP<2:0> | | | — | OC10IP<2:0> | | | 4444 |
| IPC32 | 0880 | — | DMA13IP<2:0> | | | — | DMA12IP<2:0> | | | — | IC12IP<2:0> | | | — | OC12IP<2:0> | | | 4444 |
| IPC33 | 0882 | — | IC13IP<2:0> | | | — | OC13IP<2:0> | | | — | — | — | — | — | DMA14IP<2:0> | | | 4404 |
| IPC34 | 0884 | — | IC15IP<2:0> | | | — | OC15IP<2:0> | | | — | IC14IP<2:0> | | | — | OC14IP<2:0> | | | 4444 |
| IPC35 | 0886 | — | — | — | — | — | ICDIP<2:0> | | | — | IC16IP<2:0> | | | — | OC16IP<2:0> | | | 0444 |
| INTCON1 | 08C0 | NSTDIS | OVAERR | OVBERR | COVAERR | COVBERR | OVATE | OVBTE | COVTE | SFTACERR | DIV0ERR | DMACERR | MATHERR | ADDRERR | STKERR | OSCFAIL | — | 0000 |
| INTCON2 | 08C2 | GIE | DISI | SWTRAP | — | — | — | — | — | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP | 8000 |
| INTCON3 | 08C4 | — | — | — | — | — | — | — | — | — | UAE | DAE | DOOVR | — | — | — | — | 0000 |
| INTCON4 | 08C6 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SGHT | 0000 |
| INTTREG | 08C8 | — | — | — | — | — | ILR<3:0> | | | | VECNUM<7:0> | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-8: INTERRUPT CONTROLLER REGISTER MAP FOR PIC24EPXXXGU810/814 DEVICES ONLY (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IPC20 | 0868 | — | U3TXIP<2:0> | | | — | U3RXIP<2:0> | | | — | U3EIP<2:0> | | | — | — | — | — | 4440 |
| IPC21 | 086A | — | U4EIP<2:0> | | | — | USB1IP<2:0> | | | — | — | — | — | — | — | — | — | 4400 |
| IPC22 | 086C | — | SPI3IP<2:0> | | | — | SPI3EIP<2:0> | | | — | U4TXIP<2:0> | | | — | U4RXIP<2:0> | | | 4444 |
| IPC23 | 086E | — | — | — | — | — | — | — | — | — | IC9IP<2:0> | | | — | OC9IP<2:0> | | | 0044 |
| IPC29 | 087A | — | DMA9IP<2:0> | | | — | DMA8IP<2:0> | | | — | — | — | — | — | — | — | — | 4400 |
| IPC30 | 087C | — | SPI4IP<2:0> | | | — | SPI4EIP<2:0> | | | — | DMA11IP<2:0> | | | — | DMA10IP<2:0> | | | 4444 |
| IPC31 | 087E | — | IC11IP<2:0> | | | — | OC11IP<2:0> | | | — | IC10IP<2:0> | | | — | OC10IP<2:0> | | | 4444 |
| IPC32 | 0880 | — | DMA13IP<2:0> | | | — | DMA12IP<2:0> | | | — | IC12IP<2:0> | | | — | OC12IP<2:0> | | | 4444 |
| IPC33 | 0882 | — | IC13IP<2:0> | | | — | OC13IP<2:0> | | | — | — | — | — | — | DMA14IP<2:0> | | | 4404 |
| IPC34 | 0884 | — | IC15IP<2:0> | | | — | OC15IP<2:0> | | | — | IC14IP<2:0> | | | — | OC14IP<2:0> | | | 4444 |
| IPC35 | 0886 | — | — | — | — | — | ICDIP<2:0> | | | — | IC16IP<2:0> | | | — | OC16IP<2:0> | | | 4444 |
| INTCON1 | 08C0 | NSTDIS | — | — | — | — | — | — | — | — | DIV0ERR | DMACERR | MATHERR | ADDRERR | STKERR | OSCFAIL | — | 0000 |
| INTCON2 | 08C2 | GIE | DISI | SWTRAP | — | — | — | — | — | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP | 8000 |
| INTCON3 | 08C4 | — | — | — | — | — | — | — | — | — | UAE | DAE | DOOVR | — | — | — | — | 0000 |
| INTCON4 | 08C6 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SGHT | 0000 |
| INTTREG | 08C8 | — | — | — | — | — | ILR<3:0> | | | | VECNUM<7:0> | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-11: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 16 REGISTER MAP (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OC15CON1 | 098C | — | — | OCSIDL | OCTSEL<2:0> | | | ENFLTC | ENFLTB | ENFLTA | OCFLTC | OCFLTB | OCFLTA | TRIGMODE | OCM<2:0> | | | 0000 |
| OC15CON2 | 098E | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL<4:0> | | | | | 000C |
| OC15RS | 0990 | Output Compare 15 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC15R | 0992 | Output Compare 15 Register | | | | | | | | | | | | | | | | xxxx |
| OC15TMR | 0994 | Timer Value 15 Register | | | | | | | | | | | | | | | | xxxx |
| OC16CON1 | 0996 | — | — | OCSIDL | OCTSEL<2:0> | | | ENFLTC | ENFLTB | ENFLTA | OCFLTC | OCFLTB | OCFLTA | TRIGMODE | OCM<2:0> | | | 0000 |
| OC16CON2 | 0998 | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL<4:0> | | | | | 000C |
| OC16RS | 099A | Output Compare 16 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC16R | 099C | Output Compare 16 Register | | | | | | | | | | | | | | | | xxxx |
| OC16TMR | 099E | Timer Value 16 Register | | | | | | | | | | | | | | | | xxxx |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-16: PWM GENERATOR 4 REGISTER MAP FOR dsPIC33EPXXX(MC/MU)806/810/814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PWMCON4 | 0C80 | FLTSTAT | CLSTAT | TRGSTAT | FLTIEN | CLIEN | TRGIEN | ITB | MDCS | DTC<1:0> | | DTCP | — | MTBS | CAM | XPRES | IUE | 0000 |
| IOCON4 | 0C82 | PENH | PENL | POLH | POLL | PMOD<1:0> | | OVRENH | OVRENL | OVRDAT<1:0> | | FLTDAT<1:0> | | CLDAT<1:0> | | SWAP | OSYNC | 0000 |
| FCLCON4 | 0C84 | IFLTMOD | CLSRC<4:0> | | | | | CLPOL | CLMOD | FLTSRC<4:0> | | | | | FLTPOL | FLTMOD<1:0> | | 0000 |
| PDC4 | 0C86 | PDC4<15:0> | | | | | | | | | | | | | | | | 0000 |
| PHASE4 | 0C88 | PHASE4<15:0> | | | | | | | | | | | | | | | | 0000 |
| DTR4 | 0C8A | — | — | DTR4<13:0> | | | | | | | | | | | | | | 0000 |
| ALTDTR4 | 0C8C | — | — | ALTDTR4<13:0> | | | | | | | | | | | | | | 0000 |
| SDC4 | 0C8E | SDC4<15:0> | | | | | | | | | | | | | | | | 0000 |
| SPHASE4 | 0C90 | SPHASE4<15:0> | | | | | | | | | | | | | | | | 0000 |
| TRIG4 | 0C92 | TRGCMP<15:0> | | | | | | | | | | | | | | | | 0000 |
| TRGCON4 | 0C94 | TRGDIV<3:0> | | | | — | — | — | — | — | — | TRGSTRT<5:0> | | | | | | 0000 |
| PWMCAP4 | 0C98 | PWMCAP4<15:0> | | | | | | | | | | | | | | | | 0000 |
| LEBCON4 | 0C9A | PHR | PHF | PLR | PLF | FLTLEBEN | CLLEBEN | — | — | — | — | BCH | BCL | BPHH | BPHL | BPLH | BPLL | 0000 |
| LEBDLY4 | 0C9C | — | — | — | — | LEB<11:0> | | | | | | | | | | | | 0000 |
| AUXCON4 | 0C9E | — | — | — | — | BLANKSEL<3:0> | | | | — | — | CHOPSEL<3:0> | | | | CHOPHEN | CHOPLEN | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-17: PWM GENERATOR 5 REGISTER MAP FOR dsPIC33EPXXX(MC/MU)810/814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PWMCON5 | 0CA0 | FLTSTAT | CLSTAT | TRGSTAT | FLTIEN | CLIEN | TRGIEN | ITB | MDCS | DTC<1:0> | | DTCP | — | MTBS | CAM | XPRES | IUE | 0000 |
| IOCON5 | 0CA2 | PENH | PENL | POLH | POLL | PMOD<1:0> | | OVRENH | OVRENL | OVRDAT<1:0> | | FLTDAT<1:0> | | CLDAT<1:0> | | SWAP | OSYNC | 0000 |
| FCLCON5 | 0CA4 | IFLTMOD | CLSRC<4:0> | | | | | CLPOL | CLMOD | FLTSRC<4:0> | | | | | FLTPOL | FLTMOD<1:0> | | 0000 |
| PDC5 | 0CA6 | PDC5<15:0> | | | | | | | | | | | | | | | | 0000 |
| PHASE5 | 0CA8 | PHASE5<15:0> | | | | | | | | | | | | | | | | 0000 |
| DTR5 | 0CAA | — | — | DTR5<13:0> | | | | | | | | | | | | | | 0000 |
| ALTDTR5 | 0CAC | — | — | ALTDTR5<13:0> | | | | | | | | | | | | | | 0000 |
| SDC5 | 0CAE | SDC5<15:0> | | | | | | | | | | | | | | | | 0000 |
| SPHASE5 | 0CB0 | SPHASE5<15:0> | | | | | | | | | | | | | | | | 0000 |
| TRIG5 | 0CB2 | TRGCMP<15:0> | | | | | | | | | | | | | | | | 0000 |
| TRGCON5 | 0CB4 | TRGDIV<3:0> | | | | — | — | — | — | — | — | TRGSTRT<5:0> | | | | | | 0000 |
| PWMCAP5 | 0CB8 | PWM Capture<15:0> | | | | | | | | | | | | | | | | 0000 |
| LEBCON5 | 0CBA | PHR | PHF | PLR | PLF | FLTLEBEN | CLLEBEN | — | — | — | — | BCH | BCL | BPHH | BPHL | BPLH | BPLL | 0000 |
| LEBDLY5 | 0CBC | — | — | — | — | LEB<11:0> | | | | | | | | | | | | 0000 |
| AUXCON5 | 0CBE | — | — | — | — | BLANKSEL<3:0> | | | | — | — | CHOPSEL<3:0> | | | | CHOPHEN | CHOPLEN | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-61: PORTE REGISTER MAP FOR dsPIC33EPXXXMU810/814 AND PIC24EPXXXGU810/814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISE | 0E40 | — | — | — | — | — | — | TRISE9 | TRISE8 | TRISE7 | TRISE6 | TRISE5 | TRISE4 | TRISE3 | TRISE2 | TRISE1 | TRISE0 | 03FF |
| PORTE | 0E42 | — | — | — | — | — | — | RE9 | RE8 | RE7 | RE6 | RE5 | RE4 | RE3 | RE2 | RE1 | RE0 | xxxx |
| LATE | 0E44 | — | — | — | — | — | — | LATE9 | LATE8 | LATE7 | LATE6 | LATE5 | LATE4 | LATE3 | LATE2 | LATE1 | LATE0 | xxxx |
| ODCE | 0E46 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| CNENE | 0E48 | — | — | — | — | — | — | CNIEE9 | CNIEE8 | CNIEE7 | CNIEE6 | CNIEE5 | CNIEE4 | CNIEE3 | CNIEE2 | CNIEE1 | CNIEE0 | 0000 |
| CNPUE | 0E4A | — | — | — | — | — | — | CNPUE9 | CNPUE8 | CNPUE7 | CNPUE6 | CNPUE5 | CNPUE4 | CNPUE3 | CNPUE2 | CNPUE1 | CNPUE0 | 0000 |
| CNPDE | 0E4C | — | — | — | — | — | — | CNPDE9 | CNPDE8 | CNPDE7 | CNPDE6 | CNPDE5 | CNPDE4 | CNPDE3 | CNPDE2 | CNPDE1 | CNPDE0 | 0000 |
| ANSELE | 0E4E | — | — | — | — | — | — | ANSE9 | ANSE8 | ANSE7 | ANSE6 | ANSE5 | ANSE4 | ANSE3 | ANSE2 | ANSE1 | ANSE0 | 03FF |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-62: PORTE REGISTER MAP FOR dsPIC33EPXXX(GP/MC/MU)806 AND PIC24EPXXXGP806 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISE | 0E40 | — | — | — | — | — | — | — | — | TRISE7 | TRISE6 | TRISE5 | TRISE4 | TRISE3 | TRISE2 | TRISE1 | TRISE0 | 00FF |
| PORTE | 0E42 | — | — | — | — | — | — | — | — | RE7 | RE6 | RE5 | RE4 | RE3 | RE2 | RE1 | RE0 | xxxx |
| LATE | 0E44 | — | — | — | — | — | — | — | — | LATE7 | LATE6 | LATE5 | LATE4 | LATE3 | LATE2 | LATE1 | LATE0 | xxxx |
| ODCE | 0E46 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| CNENE | 0E48 | — | — | — | — | — | — | — | — | CNIEE7 | CNIEE6 | CNIEE5 | CNIEE4 | CNIEE3 | CNIEE2 | CNIEE1 | CNIEE0 | 0000 |
| CNPUE | 0E4A | — | — | — | — | — | — | — | — | CNPUE7 | CNPUE6 | CNPUE5 | CNPUE4 | CNPUE3 | CNPUE2 | CNPUE1 | CNPUE0 | 0000 |
| CNPDE | 0E4C | — | — | — | — | — | — | — | — | CNPDE7 | CNPDE6 | CNPDE5 | CNPDE4 | CNPDE3 | CNPDE2 | CNPDE1 | CNPDE0 | 0000 |
| ANSELE | 0E4E | — | — | — | — | — | — | — | — | ANSE7 | ANSE6 | ANSE5 | ANSE4 | ANSE3 | ANSE2 | ANSE1 | ANSE0 | 00FF |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-63: PORTF REGISTER MAP FOR dsPIC33EPXXXMU810/814 AND PIC24EPXXXGU810/814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISF | 0E50 | — | — | TRISF13 | TRISF12 | — | — | — | TRISF8 | — | — | TRISF5 | TRISF4 | TRISF3 | TRISF2 | TRISF1 | TRISF0 | 313F |
| PORTF | 0E52 | — | — | RF13 | RF12 | — | — | — | RF8 | — | — | RF5 | RF4 | RF3 | RF2 | RF1 | RF0 | xxxx |
| LATF | 0E54 | — | — | LATF13 | LATF12 | — | — | — | LATF8 | — | — | LATF5 | LATF4 | LATF3 | LATF2 | LATF1 | LATF0 | xxxx |
| ODCF | 0E56 | — | — | ODCF13 | ODCF12 | — | — | — | ODCF8 | — | — | ODCF5 | ODCF4 | ODCF3 | ODCF2 | ODCF1 | ODCF0 | 0000 |
| CNENF | 0E58 | — | — | CNIEF13 | CNIEF12 | — | — | — | CNIEF8 | — | — | CNIEF5 | CNIEF4 | CNIEF3 | CNIEF2 | CNIEF1 | CNIEF0 | 0000 |
| CNPUF | 0E5A | — | — | CNPUF13 | CNPUF12 | — | — | — | CNPUF8 | — | — | CNPUF5 | CNPUF4 | CNPUF3 | CNPUF2 | CNPUF1 | CNPUF0 | 0000 |
| CNPDF | 0E5C | — | — | CNPDF13 | CNPDF12 | — | — | — | CNPDF8 | — | — | CNPDF5 | CNPDF4 | CNPDF3 | CNPDF2 | CNPDF1 | CNPDF0 | 0000 |
| ANSELF | 0E5E | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-64: PORTF REGISTER MAP FOR dsPIC33EPXXX(GP/MC)806 AND PIC24EPXXXGP806 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISF | 0E50 | — | — | — | — | — | — | — | — | — | TRISG6 | TRISF5 | TRISF4 | TRISF3 | TRISF2 | TRISF1 | TRISF0 | 003B |
| PORTF | 0E52 | — | — | — | — | — | — | — | — | — | RG6 | RF5 | RF4 | RF3 | RF2 | RF1 | RF0 | xxxx |
| LATF | 0E54 | — | — | — | — | — | — | — | — | — | LATG6 | LATF5 | LATF4 | LATF3 | LATF2 | LATF1 | LATF0 | xxxx |
| ODCF | 0E56 | — | — | — | — | — | — | — | — | — | ODCF6 | ODCF5 | ODCF4 | ODCF3 | ODCF2 | ODCF1 | ODCF0 | 0000 |
| CNENF | 0E58 | — | — | — | — | — | — | — | — | — | CNIEG6 | CNIEF5 | CNIEF4 | CNIEF3 | CNIEF2 | CNIEF1 | CNIEF0 | 0000 |
| CNPUF | 0E5A | — | — | — | — | — | — | — | — | — | CNPUG6 | CNPUF5 | CNPUF4 | CNPUF3 | CNPUF2 | CNPUF1 | CNPUF0 | 0000 |
| CNPDF | 0E5C | — | — | — | — | — | — | — | — | — | CNPDG6 | CNPDF5 | CNPDF4 | CNPDF3 | CNPDF2 | CNPDF1 | CNPDF0 | 0000 |
| ANSELF | 0E5E | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-65: PORTF REGISTER MAP FOR dsPIC33EPXXXMU806 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISF | 0E50 | — | — | — | — | — | — | — | — | — | — | TRISF5 | TRISF4 | TRISF3 | — | TRISF1 | TRISF0 | 003B |
| PORTF | 0E52 | — | — | — | — | — | — | — | — | — | — | RF5 | RF4 | RF3 | — | RF1 | RF0 | xxxx |
| LATF | 0E54 | — | — | — | — | — | — | — | — | — | — | LATF5 | LATF4 | LATF3 | — | LATF1 | LATF0 | xxxx |
| ODCF | 0E56 | — | — | — | — | — | — | — | — | — | — | ODCF5 | ODCF4 | ODCF3 | — | ODCF1 | ODCF0 | 0000 |
| CNENF | 0E58 | — | — | — | — | — | — | — | — | — | — | CNIEF5 | CNIEF4 | CNIEF3 | — | CNIEF1 | CNIEF0 | 0000 |
| CNPUF | 0E5A | — | — | — | — | — | — | — | — | — | — | CNPUF5 | CNPUF4 | CNPUF3 | — | CNPUF1 | CNPUF0 | 0000 |
| CNPDF | 0E5C | — | — | — | — | — | — | — | — | — | — | CNPDF5 | CNPDF4 | CNPDF3 | — | CNPDF1 | CNPDF0 | 0000 |
| ANSELF | 0E5E | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-66: PORTG REGISTER MAP FOR dsPIC33EPXXXMU810/814 AND PIC24EPXXXGU810/814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISG | 0E60 | TRISG15 | TRISG14 | TRISG13 | TRISG12 | — | — | TRISG9 | TRISG8 | TRISG7 | TRISG6 | — | — | — | — | TRISG1 | TRISG0 | F3C3 |
| PORTG | 0E62 | RG15 | RG14 | RG13 | RG12 | — | — | RG9 | RG8 | RG7 | RG6 | — | — | RG3(1) | RG2(1) | RG1 | RG0 | xxxx |
| LATG | 0E64 | LATG15 | LATG14 | LATG13 | LATG12 | — | — | LATG9 | LATG8 | LATG7 | LATG6 | — | — | — | — | LATG1 | LATG0 | xxxx |
| ODCG | 0E66 | ODCG15 | ODCG14 | ODCG13 | ODCG12 | — | — | — | — | — | — | — | — | — | — | ODCG1 | ODCG0 | 0000 |
| CNENG | 0E68 | CNIEG15 | CNIEG14 | CNIEG13 | CNIEG12 | — | — | CNIEG9 | CNIEG8 | CNIEG7 | CNIEG6 | — | — | CNIEG3(1) | CNIEG2(1) | CNIEG1 | CNIEG0 | 0000 |
| CNPUG | 0E6A | CNPUG15 | CNPUG14 | CNPUG13 | CNPUG12 | — | — | CNPUG9 | CNPUG8 | CNPUG7 | CNPUG6 | — | — | — | — | CNPUG1 | CNPUG0 | 0000 |
| CNPDG | 0E6C | CNPDG15 | CNPDG14 | CNPDG13 | CNPDG12 | — | — | CNPDG9 | CNPDG8 | CNPDG7 | CNPDG6 | — | — | — | — | CNPDG1 | CNPDG0 | 0000 |
| ANSELG | 0E6E | — | — | — | — | — | — | ANSG9 | ANSG8 | ANSG7 | ANSG6 | — | — | — | — | — | — | 03C0 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** If RG2 and RG3 are used as general purpose inputs, the $V_{USB3V3}$ pin must be connected to $V_{DD}$.



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**REGISTER 11-39: RPINR39: PERIPHERAL PIN SELECT INPUT REGISTER 39**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | DTCMP3R<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | DTCMP2R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **DTCMP3R<6:0>:** Assign PWM Dead-Time Compensation Input 3 to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **DTCMP2R<6:0>:** Assign PWM Dead-Time Compensation Input 2 to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-51: RPOR7: PERIPHERAL PIN SELECT OUTPUT REGISTER 7**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP97R<5:0> | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP96R<5:0> | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP97R<5:0>:** Peripheral Output Function is Assigned to RP97 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP96R<5:0>:** Peripheral Output Function is Assigned to RP96 Output Pin bits (see Table 11-3 for peripheral function numbers)

**REGISTER 11-52: RPOR8: PERIPHERAL PIN SELECT OUTPUT REGISTER 8**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP99R<5:0> | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP98R<5:0> | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP99R<5:0>:** Peripheral Output Function is Assigned to RP99 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP98R<5:0>:** Peripheral Output Function is Assigned to RP98 Output Pin bits (see Table 11-3 for peripheral function numbers)

**REGISTER 16-22: LEBCONx: LEADING-EDGE BLANKING CONTROL REGISTER x**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| PHR | PHF | PLR | PLF | FLTLEBEN | CLLEBEN | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | BCH(1) | BCL(1) | BPHH | BPHL | BPLH | BPLL |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **PHR:** PWMxH Rising Edge Trigger Enable bit
1 = Rising edge of PWMxH will trigger Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores rising edge of PWMxH

bit 14 **PHF:** PWMxH Falling Edge Trigger Enable bit
1 = Falling edge of PWMxH will trigger Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores falling edge of PWMxH

bit 13 **PLR:** PWMxL Rising Edge Trigger Enable bit
1 = Rising edge of PWMxL will trigger Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores rising edge of PWMxL

bit 12 **PLF:** PWMxL Falling Edge Trigger Enable bit
1 = Falling edge of PWMxL will trigger Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores falling edge of PWMxL

bit 11 **FLTLEBEN:** Fault Input Leading-Edge Blanking Enable bit
1 = Leading-Edge Blanking is applied to selected Fault input
0 = Leading-Edge Blanking is not applied to selected Fault input

bit 10 **CLLEBEN:** Current-Limit Leading-Edge Blanking Enable bit
1 = Leading-Edge Blanking is applied to selected current-limit input
0 = Leading-Edge Blanking is not applied to selected current-limit input

bit 9-6 **Unimplemented:** Read as '0'

bit 5 **BCH:** Blanking in Selected Blanking Signal High Enable bit(1)
1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is high
0 = No blanking when selected blanking signal is high

bit 4 **BCL:** Blanking in Selected Blanking Signal Low Enable bit(1)
1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is low
0 = No blanking when selected blanking signal is low

bit 3 **BPHH:** Blanking in PWMxH High Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is high
0 = No blanking when PWMxH output is high

bit 2 **BPHL:** Blanking in PWMxH Low Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is low
0 = No blanking when PWMxH output is low

bit 1 **BPLH:** Blanking in PWMxL High Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is high
0 = No blanking when PWMxL output is high

bit 0 **BPLL:** Blanking in PWMxL Low Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is low
0 = No blanking when PWMxL output is low

**Note 1:** The blanking signal is selected via the BLANKSELx bits in the AUXCONx register.

**REGISTER 17-15: QEIxGECH: QEIx GREATER THAN OR EQUAL COMPARE HIGH WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEIGEC<31:24> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEIGEC<23:16> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **QEIGEC<31:16>:** QEIx High Word Used to Form 32-Bit Greater Than or Equal Compare Register (QEIxGEC) bits

**REGISTER 17-16: QEIxGECL: QEIx GREATER THAN OR EQUAL COMPARE LOW WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEIGEC<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEIGEC<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **QEIGEC<15:0>:** QEIx Low Word Used to Form 32-Bit Greater Than or Equal Compare Register (QEIxGEC) bits

**REGISTER 17-17: INTxTMRH: INTERVAL TIMER x HIGH WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INTTMR<31:24> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INTTMR<23:16> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **INTTMR<31:16>:** High Word Used to Form 32-Bit Interval Timer Register (INTxTMR) bits


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**REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER**

| R-0, HSC | R-0, HSC | U-0 | U-0 | U-0 | R/C-0, HS | R-0, HSC | R-0, HSC |
|---|---|---|---|---|---|---|---|
| ACKSTAT | TRSTAT | — | — | — | BCL | GCSTAT | ADD10 |
| bit 15 | | | | | | | bit 8 |

| R/C-0, HS | R/C-0, HS | R-0, HSC | R/C-0, HSC | R/C-0, HSC | R-0, HSC | R-0, HSC | R-0, HSC |
|---|---|---|---|---|---|---|---|
| IWCOL | I2COV | D_A | P | S | R_W | RBF | TBF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Clearable bit | U = Unimplemented bit, read as '0' | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | HS = Hardware Settable bit | HSC = Hardware Settable/Clearable bit |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **ACKSTAT:** Acknowledge Status bit
(when operating as $I^2C$™ master, applicable to master transmit operation)
1 = NACK received from slave
0 = ACK received from slave
Hardware is set or clear at the end of a slave Acknowledge.

bit 14 **TRSTAT:** Transmit Status bit (when operating as $I^2C$ master, applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress
Hardware is set at the beginning of a master transmission. Hardware is clear at the end of a slave Acknowledge.

bit 13-11 **Unimplemented:** Read as '0'

bit 10 **BCL:** Master Bus Collision Detect bit
1 = A bus collision has been detected during a master operation
0 = No collision
Hardware is set at detection of a bus collision.

bit 9 **GCSTAT:** General Call Status bit
1 = General call address was received
0 = General call address was not received
Hardware is set when an address matches the general call address. Hardware is clear at a Stop detection.

bit 8 **ADD10:** 10-Bit Address Status bit
1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware is set at a match of the 2nd byte of a matched 10-bit address. Hardware is clear at a Stop detection.

bit 7 **IWCOL:** Write Collision Detect bit
1 = An attempt to write to the I2CxTRN register failed because the $I^2C$ module is busy
0 = No collision
Hardware is set at an occurrence of a write to I2CxTRN while busy (cleared by software).

bit 6 **I2COV:** I2Cx Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register is still holding the previous byte
0 = No overflow
Hardware is set at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

bit 5 **D_A:** Data/Address bit (when operating as $I^2C$ slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was a device address
Hardware is clear at a device address match. Hardware is set by reception of a slave byte.

bit 4 **P:** Stop bit
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last
Hardware is set or clear when a Start, Repeated Start or Stop is detected.


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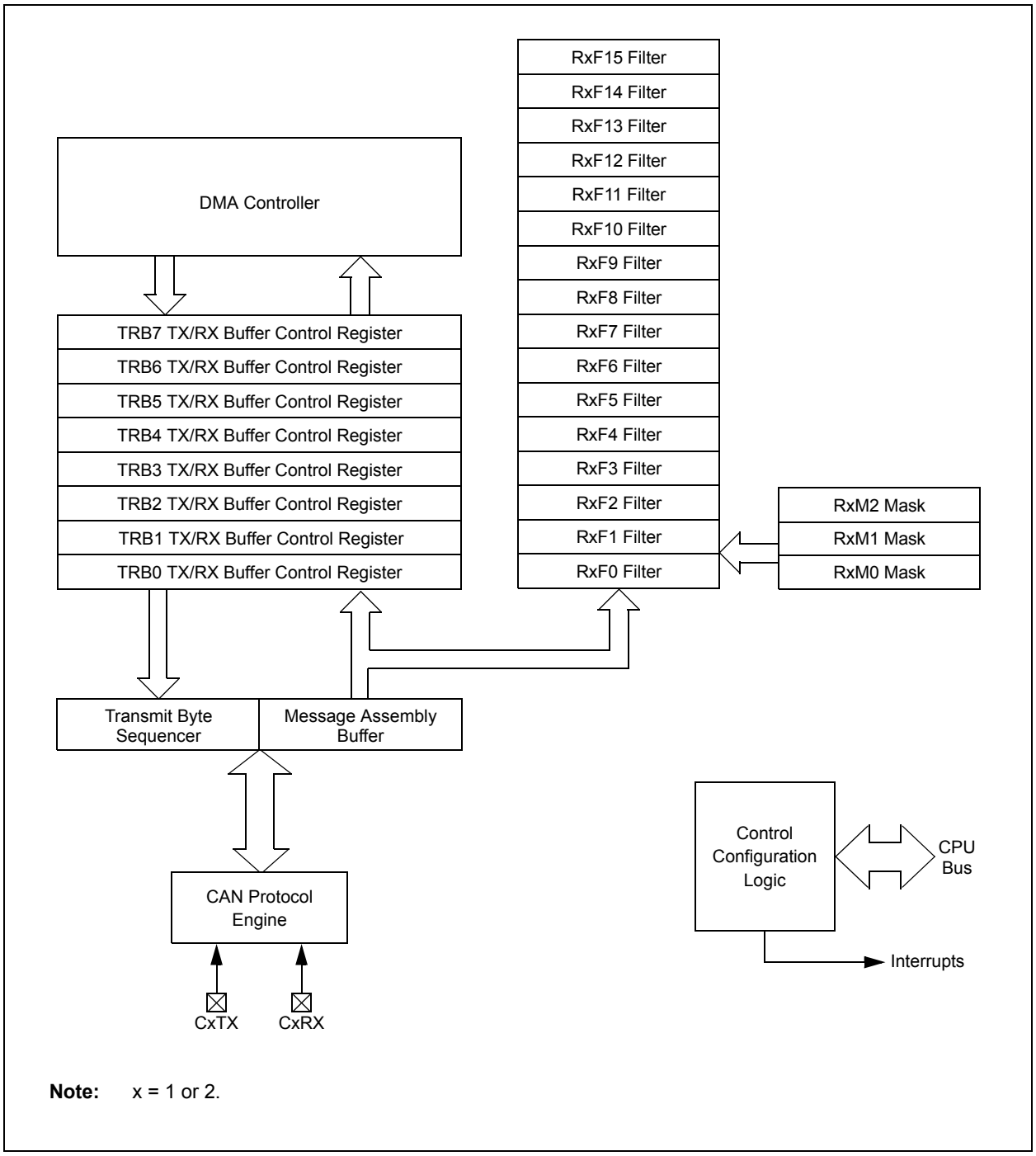
**FIGURE 21-1: ECANx MODULE BLOCK DIAGRAM**




**Note:** x = 1 or 2.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**REGISTER 25-2: CMxCON: COMPARATOR x CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CON | COE | CPOL | — | — | — | CEVT | COUT |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| EVPOL<1:0> | | — | CREF | — | — | CCH<1:0> | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **CON:** Comparator Enable bit
1 = Comparator is enabled
0 = Comparator is disabled

bit 14 **COE:** Comparator Output Enable bit
1 = Comparator output is present on the CxOUT pin
0 = Comparator output is internal only

bit 13 **CPOL:** Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **CEVT:** Comparator Event bit
1 = Comparator event according to EVPOL<1:0> settings occurred; disables future triggers and interrupts until the bit is cleared
0 = Comparator event did not occur

bit 8 **COUT:** Comparator Output bit
When CPOL = 0 (non-inverted polarity):
1 = $V_{IN+} > V_{IN-}$
0 = $V_{IN+} < V_{IN-}$
When CPOL = 1 (inverted polarity):
1 = $V_{IN+} < V_{IN-}$
0 = $V_{IN+} > V_{IN-}$

bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits
11 = Trigger/Event/Interrupt generated on any change of the comparator output (while CEVT = 0)
10 = Trigger/Event/Interrupt generated only on high-to-low transition of the polarity selected comparator output (while CEVT = 0)
If CPOL = 1 (inverted polarity):
Low-to-high transition of the comparator output.
If CPOL = 0 (non-inverted polarity):
High-to-low transition of the comparator output.
01 = Trigger/Event/Interrupt generated only on low-to-high transition of the polarity selected comparator output (while CEVT = 0)
If CPOL = 1 (inverted polarity):
High-to-low transition of the comparator output.
If CPOL = 0 (non-inverted polarity):
Low-to-high transition of the comparator output.
00 = Trigger/Event/Interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

**REGISTER 28-2: PMMODE: PARALLEL MASTER PORT MODE REGISTER**

| R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| BUSY | IRQM<1:0> | | INCM<1:0> | | MODE16 | MODE<1:0> | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| WAITB<1:0>(1,2,3) | | WAITM<3:0> | | | | WAITE<1:0>(1,2,3) | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at Reset | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **BUSY:** Busy bit (Master mode only)
1 = Port is busy
0 = Port is not busy

bit 14-13 **IRQM<1:0>:** Interrupt Request Mode bits
11 = Interrupt is generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode), or on a read/write operation when PMA<1:0> = 11 (Addressable PSP mode only)
10 = Reserved
01 = Interrupt is generated at the end of the read/write cycle
00 = No Interrupt is generated

bit 12-11 **INCM<1:0>:** Increment Mode bits
11 = PSP read and write buffers auto-increment (Legacy PSP mode only)
10 = Decrements ADDR by 1 every read/write cycle
01 = Increments ADDR by 1 every read/write cycle
00 = No increment or decrement of address

bit 10 **MODE16:** Parallel Master Port Mode 8/16-Bit Mode bit
1 = 16-bit mode: data register is 16 bits, a read/write to the data register invokes two 8-bit transfers
0 = 8-bit mode: data register is 8 bits, a read/write to the data register invokes one 8-bit transfer

bit 9-8 **MODE<1:0>:** Parallel Master Port Mode Select bits
11 = Master Mode 1 (PMCSx, PMRD/$\overline{\text{PMWR}}$, PMENB, PMBE, PMA<x:0> and PMD<7:0>)
10 = Master Mode 2 (PMCSx, PMRD, PMWR, PMBE, PMA<x:0> and PMD<7:0>)
01 = Enhanced PSP, controls signals (PMRD, PMWR, PMCSx, PMD<7:0> and PMA<1:0>)
00 = Legacy Parallel Slave Port, controls signals (PMRD, PMWR, PMCSx and PMD<7:0>)

bit 7-6 **WAITB<1:0>:** Data Setup to Read/Write/Address Phase Wait State Configuration bits(1,2,3)
11 = Data wait of 4 TP (demultiplexed/multiplexed); address phase of 4 TP (multiplexed)
10 = Data wait of 3 TP (demultiplexed/multiplexed); address phase of 3 TP (multiplexed)
01 = Data wait of 2 TP (demultiplexed/multiplexed); address phase of 2 TP (multiplexed)
00 = Data wait of 1 TP (demultiplexed/multiplexed); address phase of 1 TP (multiplexed)

bit 5-2 **WAITM<3:0>:** Read to Byte Enable Strobe Wait State Configuration bits
1111 = Wait of additional 15 TP
•
•
•
0001 = Wait of additional 1 TP
0000 = No additional Wait cycles (operation forced into one TP)

**Note 1:** The applied Wait state depends on whether data and address are multiplexed or demultiplexed. See **Section 28.4.1.8. "Wait States"** in **Section 28. "Parallel Master Port (PMP)"** (DS70576) in the *"dsPIC33E/PIC24E Family Reference Manual"* for more information.

**2:** WAITB<1:0> and WAITE<1:0> bits are ignored whenever WAITM<3:0> = 0000.

**3:** TP = 1/FP.

## 29.5 JTAG Interface

dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices implement a JTAG interface, which supports boundary scan device testing. Detailed information on this interface is provided in future revisions of the document.

**Note:** Refer to **Section 24. "Programming and Diagnostics"** (DS70608) of the *"dsPIC33E/PIC24E Family Reference Manual"* for further information on usage, configuration and operation of the JTAG interface.

## 29.6 In-Circuit Serial Programming

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices can be serially programmed while in the end application circuit. This is done with two lines for clock and data, and three other lines for power, ground and the programming sequence. Serial programming allows customers to manufacture boards with unprogrammed devices and then program the digital signal controller just before shipping the product. Serial programming also allows the most recent firmware or a custom firmware to be programmed. Refer to the *"dsPIC33E/PIC24E Flash Programming Specification"* (DS70619) for details about In-Circuit Serial Programming (ICSP).

Any of the three pairs of programming clock/data pins can be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

## 29.7 In-Circuit Debugger

When MPLAB® ICD 3 or REAL ICE™ is selected as a debugger, the in-circuit debugging functionality is enabled. This function allows simple debugging functions when used with MPLAB IDE. Debugging functionality is controlled through the PGECx (Emulation/Debug Clock) and PGEDx (Emulation/Debug Data) pin functions.

Any of the three pairs of debugging clock/data pins can be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

To use the in-circuit debugger function of the device, the design must implement ICSP connections to $\overline{MCLR}$, $V_{DD}$, $V_{SS}$ and the PGECx/PGEDx pin pair. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two I/O pins.

## 29.8 Code Protection and CodeGuard™ Security

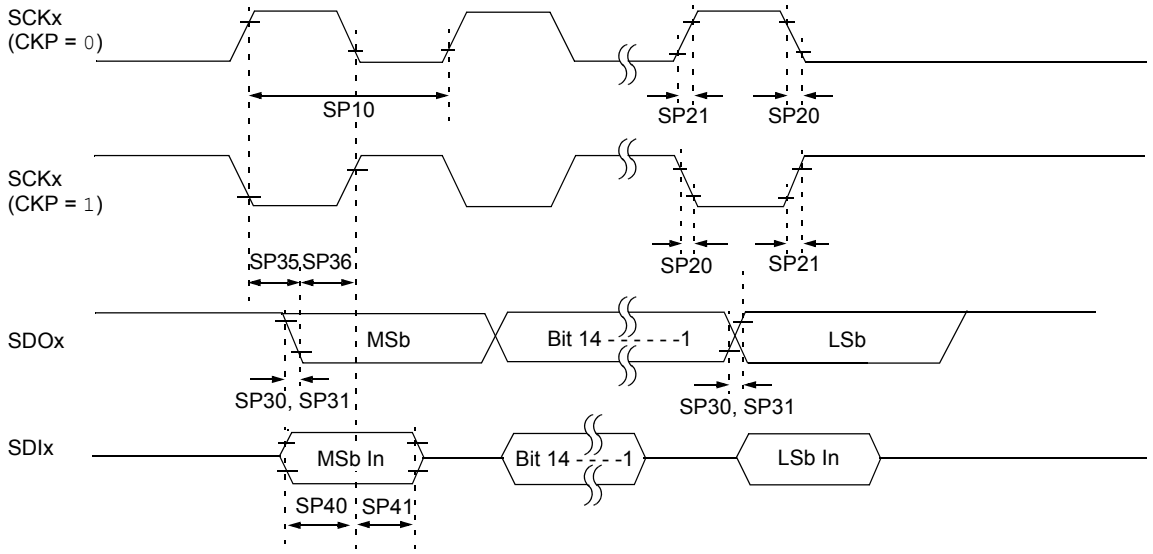
The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices offer basic implementation of CodeGuard Security that supports only General Segment (GS) security. This feature helps protect individual Intellectual Property in collaborative system designs.

When coupled with software encryption libraries, CodeGuard Security can be used to securely update Flash even when multiple IPs reside on the single chip. The code protection features vary depending on the actual dsPIC33E implemented. The following sections provide an overview of these features.

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices do not support Boot Segment (BS), Secure Segment (SS) and RAM protection.

**Note:** Refer to **Section 23. "CodeGuard™ Security"** (DS70634) of the *"dsPIC33E/PIC24E Family Reference Manual"* for further information on usage, configuration and operation of CodeGuard Security.

**FIGURE 32-18: SPI1, SPI3 AND SPI4 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.

**TABLE 32-36: SPI1, SPI3 AND SPI4 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP10 | TscP | Maximum SCKx Frequency | — | — | 9 | MHz | -40ºC to +125ºC and see **Note 3** |
| SP20 | TscF | SCKx Output Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP21 | TscR | SCKx Output Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP30 | TdoF | SDOx Data Output Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP31 | TdoR | SDOx Data Output Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid After SCKx Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDOx Data Output Setup to First SCKx Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 30 | — | — | ns | |

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

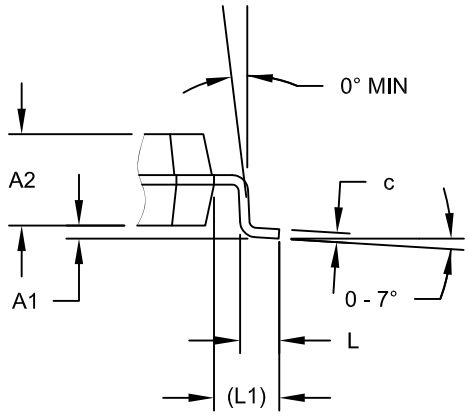
**2:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCKx is 111 ns. The clock generated in Master mode must not violate this specification.

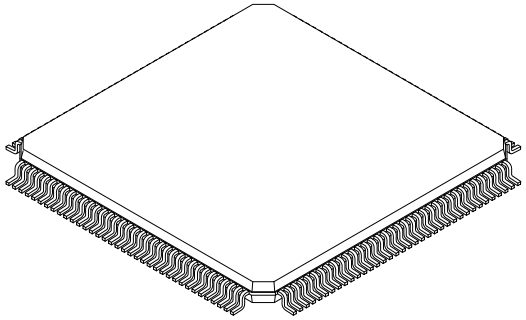
**4:** Assumes 50 pF load on all SPIx pins.

## 144-Lead Plastic Low Profile Quad Flatpack (PL) – 20x20x1.40 mm Body, with 2.00 mm Footprint [LQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




**DETAIL A**



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Leads | N | | 144 | |
| Lead Pitch | e | | 0.50 BSC | |
| Overall Height | A | - | - | 1.60 |
| Molded Package Height | A2 | 1.35 | 1.40 | 1.45 |
| Standoff | A1 | 0.05 | - | 0.15 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 (REF) | |
| Overall Width | E | | 22.00 BSC | |
| Overall Length | D | | 22.00 BSC | |
| Molded Body Width | E1 | | 20.00 BSC | |
| Molded Body Length | D1 | | 20.00 BSC | |
| Lead Thickness | c | 0.09 | - | 0.20 |
| Lead Width | b | 0.17 | 0.22 | 0.27 |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-044B Sheet 2 of 2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**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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