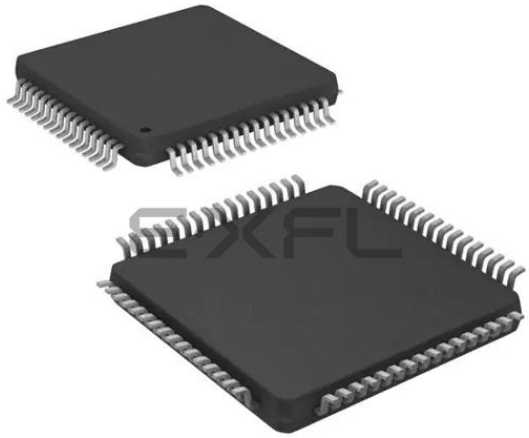
Microchip Technology - DSPIC33EP512GP806T-I/PT Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

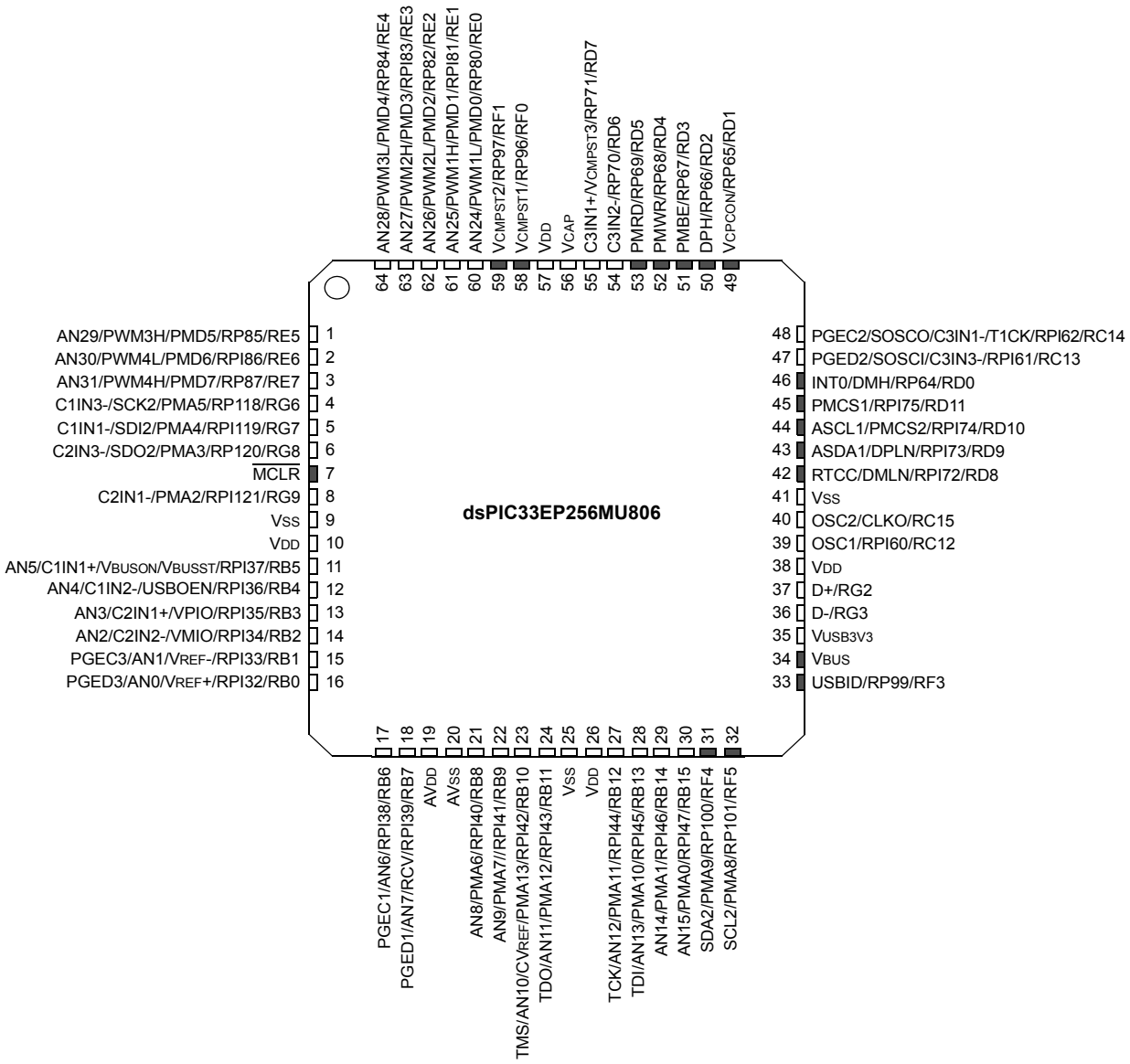
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512gp806t-i-pt

Pin Diagrams

64-Pin QFN

■ = Pins are up to 5V tolerant



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The availability of I^2C™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

Pin Diagrams (Continued)

121-Pin TFBGA(1)

● = Pins are up to 5V tolerant

dsPIC33EP256MU810
dsPIC33EP512MU810

	1	2	3	4	5	6	7	8	9	10	11
A	RE4	RE3	RG13	RE0	RG0	RF1	VDD	NC	RD12	RD2	RD1
B	NC	RG15	RE2	RE1	RA7	RF0	VCAP	RD5	RD3	VSS	RC14
C	RE6	VDD	RG12	RG14	RA6	NC	RD7	RD4	NC	RC13	RD11
D	RC1	RE7	RE5	NC	NC	NC	RD6	RD13	RD0	NC	RD10
E	RC4	RC3	RG6	RC2	NC	RG1	NC	RA15	RD8	RD9	RA14
F	$\overline{MCLR}$	RG8	RG9	RG7	VSS	NC	NC	VDD	RC12	VSS	RC15
G	RE8	RE9	RA0	NC	VDD	VSS	VSS	NC	RA5	RA3	RA4
H	RB5	RB4	NC	NC	NC	VDD	NC	VBUS	VUSB3V3	RG2	RA2
J	RB3	RB2	RB7	AVDD	RB11	RA1	RB12	NC	NC	RF8	RG3
K	RB1	RB0	RA10	RB8	NC	RF12	RB14	VDD	RD15	RF3	RF2
L	RB6	RA9	AVSS	RB9	RB10	RF13	RB13	RB15	RD14	RF4	RF5

Note 1: Refer to Table 2 for full pin names.

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS AND MICROCONTROLLERS

Note 1: This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com)

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

2.1 Basic Connection Requirements

Getting started with the 16-bit DSCs and microcontrollers requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see **Section 2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins (regardless if ADC module is not used) (see **Section 2.2 "Decoupling Capacitors"**)
- VCAP (see **Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)"**)
- $\overline{\text{MCLR}}$ pin (see **Section 2.4 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **Section 2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins when external oscillator source is used (see **Section 2.6 "External Oscillator Pins"**)

Additionally, the following pins may be required:

- VUSB3V3 pin is used when utilizing the USB module. If the USB module is not used, VUSB3V3 must be connected to VDD.
- VREF+/VREF- pin is used when external voltage reference for ADC module is implemented

Note: The AVDD and AVSS pins must be connected independent of the ADC voltage reference source. The voltage difference between AVDD and VDD cannot exceed 300 mV at any time during operation or start-up.

2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, VUSB3V3, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 0.1 µF (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended to use ceramic capacitors.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high frequency noise:** If the board is experiencing high frequency noise, above tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

REGISTER 3-2: CORCON: CORE CONTROL REGISTER (CONTINUED)

bit 2 **SFA:** Stack Frame Active Status bit
- 1 = Stack frame is active; W14 and W15 address 0x0000 to 0xFFFF, regardless of DSRPAG and DSWPAG values
- 0 = Stack frame is not active; W14 and W15 address of EDS or Base Data Space

bit 1 **RND:** Rounding Mode Select bit(1)
- 1 = Biased (conventional) rounding is enabled
- 0 = Unbiased (convergent) rounding is enabled

bit 0 **IF:** Integer or Fractional Multiplier Mode Select bit(1)
- 1 = Integer mode is enabled for DSP multiply
- 0 = Fractional mode is enabled for DSP multiply

Note 1: This bit is available on dsPIC33EPXXX(GP/MC/MU)806/810/814 devices only.

2: This bit is always read as '0'.

3: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

TABLE 4-38: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXMU806 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	—	RP65R<5:0>						—	—	RP64R<5:0>						0000
RPOR1	0682	—	—	RP67R<5:0>						—	—	RP66R<5:0>						0000
RPOR2	0684	—	—	RP69R<5:0>						—	—	RP68R<5:0>						0000
RPOR3	0686	—	—	RP71R<5:0>						—	—	RP70R<5:0>						0000
RPOR4	0688	—	—	RP80R<5:0>						—	—	—	—	—	—	—	—	0000
RPOR5	068A	—	—	RP84R<5:0>						—	—	RP82R<5:0>						0000
RPOR6	068C	—	—	RP87R<5:0>						—	—	RP85R<5:0>						0000
RPOR7	068E	—	—	RP97R<5:0>						—	—	RP96R<5:0>						0000
RPOR8	0690	—	—	RP99R<5:0>						—	—	—	—	—	—	—	—	0000
RPOR9	0692	—	—	RP101R<5:0>						—	—	RP100R<5:0>						0000
RPOR13	069A	—	—	RP118R<5:0>						—	—	—	—	—	—	—	—	0000
RPOR14	069C	—	—	—	—	—	—	—	—	—	—	RP120R<5:0>						0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-39: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXX(GP/MC/MU)806 AND PIC24EPXXXGP806 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	—	RP65R<5:0>						—	—	RP64R<5:0>						0000
RPOR1	0682	—	—	RP67R<5:0>						—	—	RP66R<5:0>						0000
RPOR2	0684	—	—	RP69R<5:0>						—	—	RP68R<5:0>						0000
RPOR3	0686	—	—	RP71R<5:0>						—	—	RP70R<5:0>						0000
RPOR4	0688	—	—	RP80R<5:0>						—	—	—	—	—	—	—	—	0000
RPOR5	068A	—	—	RP84R<5:0>						—	—	RP82R<5:0>						0000
RPOR6	068C	—	—	RP87R<5:0>						—	—	RP85R<5:0>						0000
RPOR7	068E	—	—	RP97R<5:0>						—	—	RP96R<5:0>						0000
RPOR8	0690	—	—	RP99R<5:0>						—	—	RP98R<5:0>						0000
RPOR9	0692	—	—	RP101R<5:0>						—	—	RP100R<5:0>						0000
RPOR10	0694	—	—	—	—	—	—	—	—	—	—	RP102R<5:0>						0000
RPOR13	069A	—	—	RP118R<5:0>						—	—	—	—	—	—	—	—	0000
RPOR14	069C	—	—	—	—	—	—	—	—	—	—	RP120R<5:0>						0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

In addition, DMA transfers can be triggered by timers as well as external interrupts. Each DMA channel is unidirectional. Two DMA channels must be allocated to read and write to a peripheral. If more than one channel receive a request to transfer data, a simple fixed priority scheme, based on channel number, dictates which channel completes the transfer and which channel, or channels, are left pending. Each DMA channel moves a block of data, after which it generates an interrupt to the CPU to indicate that the block is available for processing.

The DMA controller provides these functional capabilities:

- Up to 15 DMA Channels
- Register Indirect With Post-Increment Addressing mode
- Register Indirect Without Post-Increment Addressing mode
- Peripheral Indirect Addressing mode (peripheral generates destination address)
- CPU Interrupt after Half or Full Block Transfer Complete
- Byte or Word Transfers
- Fixed Priority Channel Arbitration
- Manual (software) or Automatic (peripheral DMA requests) Transfer Initiation
- One-Shot or Auto-Repeat Block Transfer modes
- Ping-Pong mode (automatic switch between two DPSRAM start addresses after each block transfer complete)
- DMA Request for Each Channel can be Selected from Any Supported Interrupt Source
- Debug Support Features

The peripherals that can utilize DMA are listed in Table 8-1.

TABLE 8-1: DMA CHANNEL TO PERIPHERAL ASSOCIATIONS

Peripheral to DMA Association	DMAxREQ Register IRQSEL<7:0> Bits	DMAxPAD Register (Values to Read from Peripheral)	DMAxPAD Register (Values to Write to Peripheral)
INT0 – External Interrupt 0	00000000	—	—
IC1 – Input Capture 1	00000001	0x0144 (IC1BUF)	—
IC2 – Input Capture 2	00000101	0x014C (IC2BUF)	—
IC3 – Input Capture 3	00100101	0x0154 (IC3BUF)	—
IC4 – Input Capture 4	00100110	0x015C (IC4BUF)	—
OC1 – Output Compare 1	00000010	—	0x0906 (OC1R) 0x0904 (OC1RS)
OC2 – Output Compare 2	00000110	—	0x0910 (OC2R) 0x090E (OC2RS)
OC3 – Output Compare 3	00011001	—	0x091A (OC3R) 0x0918 (OC3RS)
OC4 – Output Compare 4	00011010	—	0x0924 (OC4R) 0x0922 (OC4RS)
TMR2 – Timer2	00000111	—	—
TMR3 – Timer3	00001000	—	—
TMR4 – Timer4	00011011	—	—
TMR5 – Timer5	00011100	—	—
SPI1 Transfer Done	00001010	0x0248 (SPI1BUF)	0x0248 (SPI1BUF)
SPI2 Transfer Done	00100001	0x0268 (SPI2BUF)	0x0268 (SPI2BUF)
SPI3 Transfer Done	01011011	0x02A8 (SPI3BUF)	0x02A8 (SPI3BUF)
SPI4 Transfer Done	01111011	0x02C8 (SPI4BUF)	0x02C8 (SPI4BUF)
UART1RX – UART1 Receiver	00001011	0x0226 (U1RXREG)	—
UART1TX – UART1 Transmitter	00001100	—	0x0224 (U1TXREG)
UART2RX – UART2 Receiver	00011110	0x0236 (U2RXREG)	—
UART2TX – UART2 Transmitter	00011111	—	0x0234 (U2TXREG)
UART3RX – UART3 Receiver	01010010	0x0256 (U3RXREG)	—
UART3TX – UART3 Transmitter	01010011	—	0x0254 (U3TXREG)

REGISTER 8-2: DMAxREQ: DMA CHANNEL x IRQ SELECT REGISTER

R/S-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
FORCE(1)	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQSEL<7:0>							
bit 7							bit 0

Legend:	S = Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **FORCE:** Force DMA Transfer bit(1)
1 = Forces a single DMA transfer (Manual mode)
0 = Automatic DMA transfer initiation by DMA request

bit 14-8 **Unimplemented:** Read as '0'

bit 7-0 **IRQSEL<7:0>:** DMA Peripheral IRQ Number Select bits
00000000 = INT0 – External Interrupt 0
00000001 = IC1 – Input Capture 1
00000010 = OC1 – Output Compare 1
00000101 = IC2 – Input Capture 2
00000110 = OC2 – Output Compare 2
00000111 = TMR2 – Timer2
00001000 = TMR3 – Timer3
00001010 = SPI1 – Transfer done
00001011 = UART1RX – UART1 Receiver
00001100 = UART1TX – UART1 Transmitter
00001101 = ADC1 – ADC1 convert done
00010101 = ADC2 – ADC2 convert done
00011001 = OC3 – Output Compare 3
00011010 = OC4 – Output Compare 4
00011011 = TMR4 – Timer4
00011100 = TMR5 – Timer5
00011110 = UART2RX – UART2 Receiver
00011111 = UART2TX – UART2 Transmitter
00100001 = SPI2 – Transfer done
00100010 = ECAN1 – RX data ready
00100101 = IC3 – Input Capture 3
00100110 = IC4 – Input Capture 4
00101101 = PMP Data mode
00110111 = ECAN2 – RX data ready
00111100 = DCI – DCI transfer done
01000110 = ECAN1 – TX data request
01000111 = ECAN2 – TX data request
01010010 = UART3RX – UART3 Receiver
01010011 = UART3TX – UART3 Transmitter
01011000 = UART4RX – UART4 Receiver
01011001 = UART4TX – UART4 Transmitter
01011011 = SPI3 – Transfer done
01111011 = SPI4 – Transfer done

Note 1: The FORCE bit cannot be cleared by user software. The FORCE bit is cleared by hardware when the forced DMA transfer is complete or the channel is disabled (CHEN = 0).

REGISTER 8-11: DMAPWC: DMA PERIPHERAL WRITE COLLISION STATUS REGISTER (CONTINUED)

bit 2 **PWCOL2:** Channel 2 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected

bit 1 **PWCOL1:** Channel 1 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected

bit 0 **PWCOL0:** Channel 0 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected

REGISTER 10-5: PMD5: PERIPHERAL MODULE DISABLE CONTROL REGISTER 5 (CONTINUED)

bit 3 **OC12MD:** OC12 Module Disable bit
1 = OC12 module is disabled
0 = OC12 module is enabled

bit 2 **OC11MD:** OC11 Module Disable bit
1 = OC11 module is disabled
0 = OC11 module is enabled

bit 1 **OC10MD:** OC10 Module Disable bit
1 = OC10 module is disabled
0 = OC10 module is enabled

bit 0 **OC9MD:** OC9 Module Disable bit
1 = OC9 module is disabled
0 = OC9 module is enabled

TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES

Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment
000 0000	I	Vss
000 0001	I	C1OUT(1)
000 0010	I	C2OUT(1)
000 0011	I	C3OUT(1)
000 0100	—	Reserved
000 0101	—	Reserved
000 0110	—	Reserved
000 0111	—	Reserved
000 1000	I	FINDX1(1)
000 1001	I	FHOME1(1)
000 1010	I	FINDX2(1)
000 1011	I	FHOME2(1)
000 1100	—	Reserved
000 1101	—	Reserved
000 1110	—	Reserved
000 1111	—	Reserved
001 0000	I	RPI16
001 0001	I	RPI17
001 0010	I	RPI18
001 0011	I	RPI19
001 0100	I	RPI20
001 0101	I	RPI21
001 0110	I	RPI22
001 0111	I	RPI23
001 1000	—	Reserved
001 1001	—	Reserved
001 1010	—	Reserved
001 1011	—	Reserved
001 1100	—	Reserved
001 1101	—	Reserved
001 1110	I	RPI30
001 1111	I	RPI31
010 0000	I	RPI32
010 0001	I	RPI33
010 0010	I	RPI34
010 0011	I	RPI35
010 0100	I	RPI36
010 0101	I	RPI37
010 0110	I	RPI38
010 0111	I	RPI39
010 1000	I	RPI40
010 1001	I	RPI41
010 1010	I	RPI42
010 1101	I	RPI45
010 1110	I	RPI46
010 1111	I	RPI47
011 0000	—	Reserved
011 0001	I	RPI49
011 0010	I	RPI50
011 0011	I	RPI51
011 0100	I	RPI52
011 0101	—	Reserved
011 0110	—	Reserved
011 0111	—	Reserved
011 1000	—	Reserved
011 1001	—	Reserved
011 1010	—	Reserved
011 1011	—	Reserved
011 1100	I	RPI60
011 1101	I	RPI61
011 1110	I	RPI62
011 1111	—	Reserved
100 0000	I/O	RP64
100 0001	I/O	RP65
100 0010	I/O	RP66
100 0011	I/O	RP67
100 0100	I/O	RP68
100 0101	I/O	RP69
100 0110	I/O	RP70
100 0111	I/O	RP71
100 1000	I	RPI72
100 1001	I	RPI73
100 1010	I	RPI74
100 1011	I	RPI75
100 1100	I	RPI76
100 1101	I	RPI77
100 1110	I	RPI78
100 1111	I/O	RP79
101 0000	I/O	RP80
101 0001	I	RPI81
101 0010	I/O	RP82
101 0011	I	RPI83
101 0100	I/O	RP84
101 0101	I/O	RP85
101 0110	I	RPI86
101 0111	I/O	RP87

Note 1: See **Section 11.4.4.2 “Virtual Connections”** for more information on selecting this pin assignment.

REGISTER 15-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2 (CONTINUED)

bit 4-0 **SYNCSEL<4:0>:** Trigger/Synchronization Source Selection bits

11111 = No Sync or Trigger source for OCx
11110 = INT2 pin synchronizes or triggers OCx
11101 = INT1 pin synchronizes or triggers OCx
11100 = Reserved
11011 = ADC1 module synchronizes or triggers OCx
11010 = CMP3 module synchronizes or triggers OCx
11001 = CMP2 module synchronizes or triggers OCx
11000 = CMP1 module synchronizes or triggers OCx
10111 = IC8 module synchronizes or triggers OCx
10110 = IC7 module synchronizes or triggers OCx
10101 = IC6 module synchronizes or triggers OCx
10100 = IC5 module synchronizes or triggers OCx
10011 = IC4 module synchronizes or triggers OCx
10010 = IC3 module synchronizes or triggers OCx
10001 = IC2 module synchronizes or triggers OCx
10000 = IC1 module synchronizes or triggers OCx
01111 = Timer5 synchronizes or triggers OCx
01110 = Timer4 synchronizes or triggers OCx
01101 = Timer3 synchronizes or triggers OCx
01100 = Timer2 synchronizes or triggers OCx (default)
01011 = Timer1 synchronizes or triggers OCx
01010 = No Sync or Trigger source for OCx
01001 = OC9 module synchronizes or triggers OCx(1,2)
01000 = OC8 module synchronizes or triggers OCx(1,2)
00111 = OC7 module synchronizes or triggers OCx(1,2)
00110 = OC6 module synchronizes or triggers OCx(1,2)
00101 = OC5 module synchronizes or triggers OCx(1,2)
00100 = OC4 module synchronizes or triggers OCx(1,2)
00011 = OC3 module synchronizes or triggers OCx(1,2)
00010 = OC2 module synchronizes or triggers OCx(1,2)
00001 = OC1 module synchronizes or triggers OCx(1,2)
00000 = No Sync or Trigger source for OCx

Note 1: Do not use the OCx module as its own Sync or Trigger source.

2: When the OCy module is turned OFF, it sends a trigger out signal. If the OCx module uses the OCy module as a Trigger source, the OCy module must be unselected as a Trigger source prior to disabling it.

21.4 ECANx Control Registers

REGISTER 21-1: CxCTRL1: ECANx CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
—	—	CSIDL	ABAT	CANCKS	REQOP<2:0>		
bit 15							bit 8

R-1	R-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0
OPMODE<2:0>			—	CANCAP	—	—	WIN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **CSIDL:** ECANx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **ABAT:** Abort All Pending Transmissions bit
1 = Signals all transmit buffers to abort transmission
0 = Module will clear this bit when all transmissions are aborted

bit 11 **CANCKS:** ECANx Module Clock (FCAN) Source Select bit
1 = FCAN is equal to twice FP
0 = FCAN is equal to FP

bit 10-8 **REQOP<2:0>:** Request Operation Mode bits
111 = Set Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Set Configuration mode
011 = Set Listen Only Mode
010 = Set Loopback mode
001 = Set Disable mode
000 = Set Normal Operation mode

bit 7-5 **OPMODE<2:0>:** Operation Mode bits
111 = Module is in Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Module is in Configuration mode
011 = Module is in Listen Only mode
010 = Module is in Loopback mode
001 = Module is in Disable mode
000 = Module is in Normal Operation mode

bit 4 **Unimplemented:** Read as '0'

bit 3 **CANCAP:** CAN Message Receive Timer Capture Event Enable bit
1 = Enables input capture based on CAN message receive
0 = Disables CAN capture

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **WIN:** SFR Map Window Select bit
1 = Uses filter window
0 = Uses buffer window

REGISTER 21-5: CxFIFO: ECANx FIFO STATUS REGISTER

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	FBP<5:0>					
bit 15							bit 8

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	FNRB<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **FBP<5:0>:** FIFO Buffer Pointer bits

011111 = RB31 buffer
011110 = RB30 buffer
•
•
•
000001 = TRB1 buffer
000000 = TRB0 buffer

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **FNRB<5:0>:** FIFO Next Read Buffer Pointer bits

011111 = RB31 buffer
011110 = RB30 buffer
•
•
•
000001 = TRB1 buffer
000000 = TRB0 buffer

28.0 PARALLEL MASTER PORT (PMP)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 28. "Parallel Master Port (PMP)"** (DS70576) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

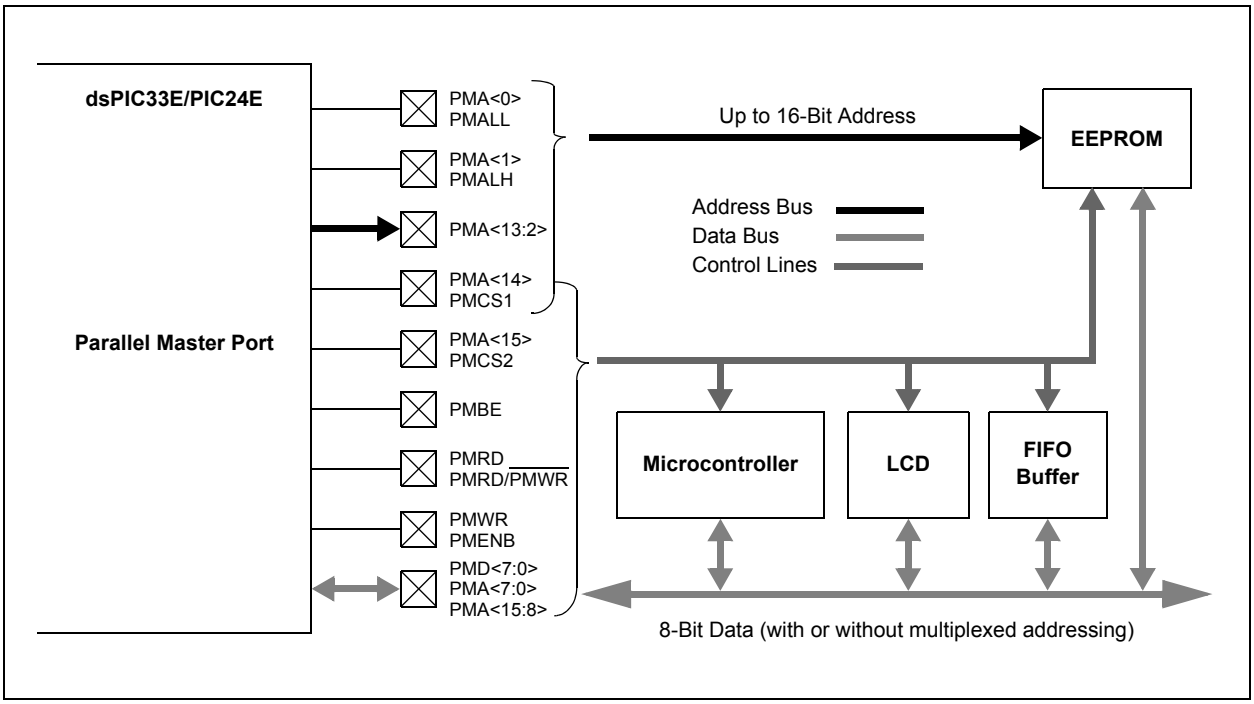
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Parallel Master Port (PMP) module is a parallel 8-bit I/O module, specifically designed to communicate with a wide variety of parallel devices, such as communication peripherals, LCDs, external memory devices and microcontrollers. Because the interface to parallel peripherals varies significantly, the PMP is highly configurable.

Key features of the PMP module include:

- Eight Data Lines
- Up to 16 Programmable Address Lines
- Up to 2 Chip Select Lines
- Programmable Strobe Options:
  - Individual read and write strobes, or
  - Read/$\overline{\text{Write}}$ strobe with enable strobe
- Address Auto-Increment/Auto-Decrement
- Programmable Address/Data Multiplexing
- Programmable Polarity on Control Signals
- Legacy Parallel Slave Port (PSP) Support
- Enhanced Parallel Slave Support:
  - Address support
  - 4-byte deep auto-incrementing buffer
- Programmable Wait States

FIGURE 28-1: PMP MODULE PINOUT AND CONNECTIONS TO EXTERNAL DEVICES



REGISTER 28-4: PMAEN: PARALLEL MASTER PORT ADDRESS ENABLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN15	PTEN14	PTEN13	PTEN12	PTEN11	PTEN10	PTEN9	PTEN8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN7	PTEN6	PTEN5	PTEN4	PTEN3	PTEN2	PTEN1	PTEN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at Reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PTEN15:** PMCS2 Strobe Enable bit
1 = PMA15 functions as either PMA<15> or PMCS2
0 = PMA15 functions as port I/O

bit 14 **PTEN14:** PMCS1 Strobe Enable bit
1 = PMA14 functions as either PMA<14> or PMCS1
0 = PMA14 functions as port I/O

bit 13-2 **PTEN<13:2>:** PMP Address Port Enable bits
1 = PMA<13:2> function as PMP address lines
0 = PMA<13:2> function as port I/O

bit 1-0 **PTEN<1:0>:** PMALH/PMALL Strobe Enable bits
1 = PMA1 and PMA0 function as either PMA<1:0> or PMALH and PMALL
0 = PMA1 and PMA0 function as port I/O

TABLE 32-56: ADC MODULE SPECIFICATIONS (10-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (see Note 1) (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
ADC Accuracy (10-Bit Mode) – Measurements with External VREF+/VREF-							
AD20b	Nr	Resolution	10 data bits			bits	
AD21b	INL	Integral Nonlinearity	-1	—	+1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
AD22b	DNL	Differential Nonlinearity	>-1	—	<1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
AD23b	GERR	Gain Error	1	3	6	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
AD24b	EOFF	Offset Error	1	2	3	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
AD25b	—	Monotonicity	—	—	—	—	Guaranteed(2)
ADC Accuracy (10-Bit Mode) – Measurements with Internal VREF+/VREF-							
AD20b	Nr	Resolution	10 data bits			bits	
AD21b	INL	Integral Nonlinearity	-1.5	—	+1.5	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD22b	DNL	Differential Nonlinearity	>-1	—	<1	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD23b	GERR	Gain Error	1	5	6	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD24b	EOFF	Offset Error	1	2	5	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD25b	—	Monotonicity	—	—	—	—	Guaranteed(2)
Dynamic Performance (10-Bit Mode)							
AD30b	THD	Total Harmonic Distortion	—	—	-64	dB	
AD31b	SINAD	Signal to Noise and Distortion	57	58.5	—	dB	
AD32b	SFDR	Spurious Free Dynamic Range	72	—	—	dB	
AD33b	FNYQ	Input Signal Bandwidth	—	—	550	kHz	
AD34b	ENOB	Effective Number of Bits	9.16	9.4	—	bits	

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.

2: The Analog-to-Digital conversion result never decreases with an increase in input voltage and has no missing codes.

TABLE 32-57: ADC CONVERSION (12-BIT MODE) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (see Note 4) (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
Clock Parameters							
AD50	TAD	ADC Clock Period	117.6	—	—	ns	
AD51	tRC	ADC Internal RC Oscillator Period	—	250	—	ns	
Conversion Rate							
AD55	tCONV	Conversion Time	—	14 TAD		ns	
AD56	FCNV	Throughput Rate	—	—	500	Ksps	
AD57	TSAMP	Sample Time	3 TAD	—	—	—	
Timing Parameters							
AD60	tPCS	Conversion Start from Sample Trigger(1)	2 TAD	—	3 TAD	—	Auto-Convert Trigger not selected
AD61	tPSS	Sample Start from Setting Sample (SAMP) bit(1)	2 TAD	—	3 TAD	—	
AD62	tCSS	Conversion Completion to Sample Start (ASAM = 1)(1)	—	0.5 TAD	—	—	
AD63	tDPU	Time to Stabilize Analog Stage from ADC Off to ADC On(1)	—	—	20	μs	See **Note 3**

Note 1: Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.

2: These parameters are characterized but not tested in manufacturing.

3: The tDPU parameter is the time required for the ADC module to stabilize at the appropriate level when the module is turned on (ADON (ADxCON1<15>) = 1). During this time, the ADC result is indeterminate.

4: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.

FIGURE 33-5: TYPICAL IPD CURRENT @ VDD = 3.3V

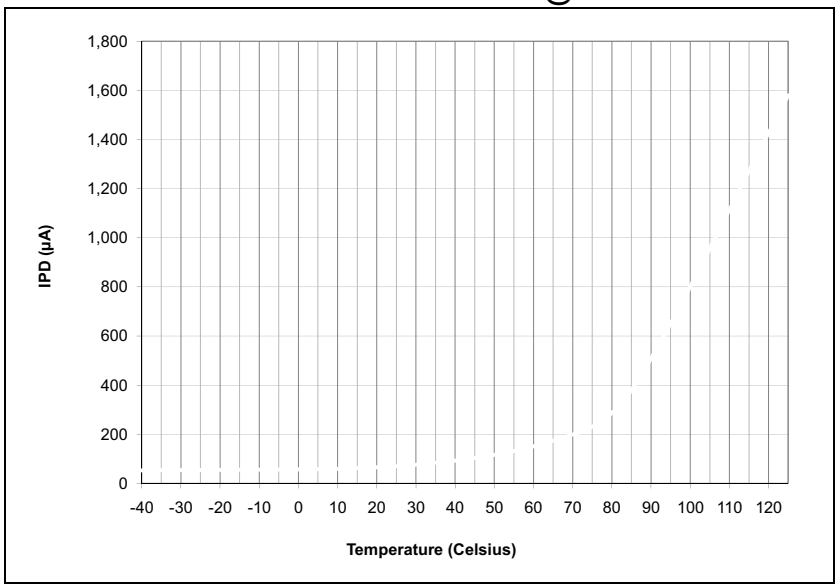


FIGURE 33-6: TYPICAL IDD CURRENT – VDD = 3.3V @ +85ºC

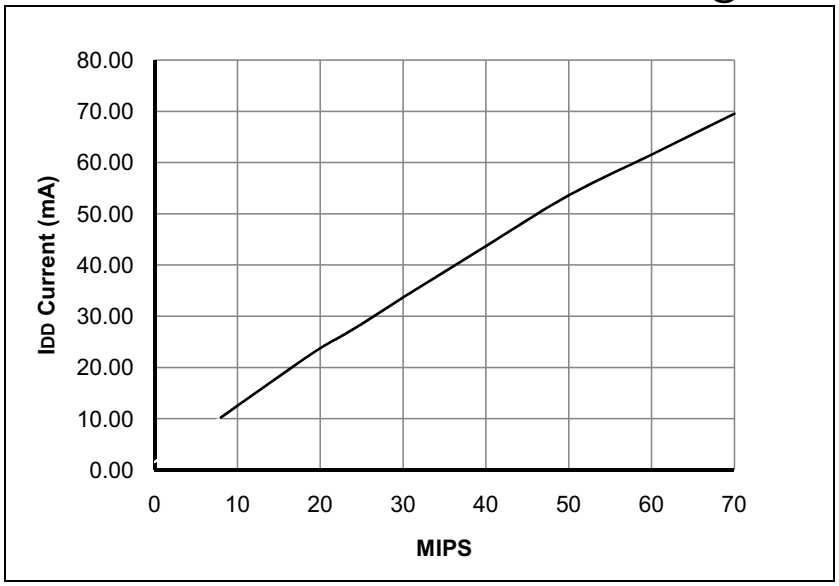


FIGURE 33-7: TYPICAL IDOZE CURRENT @ VDD = 3.3V

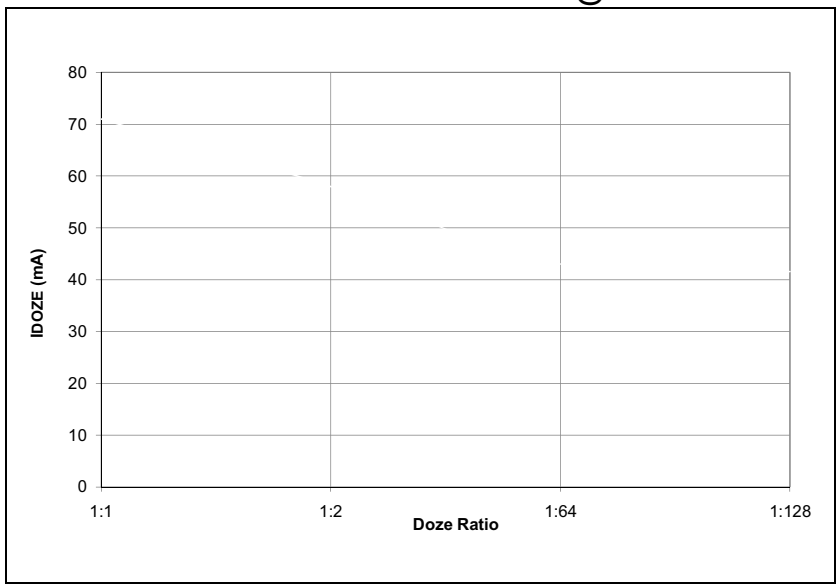
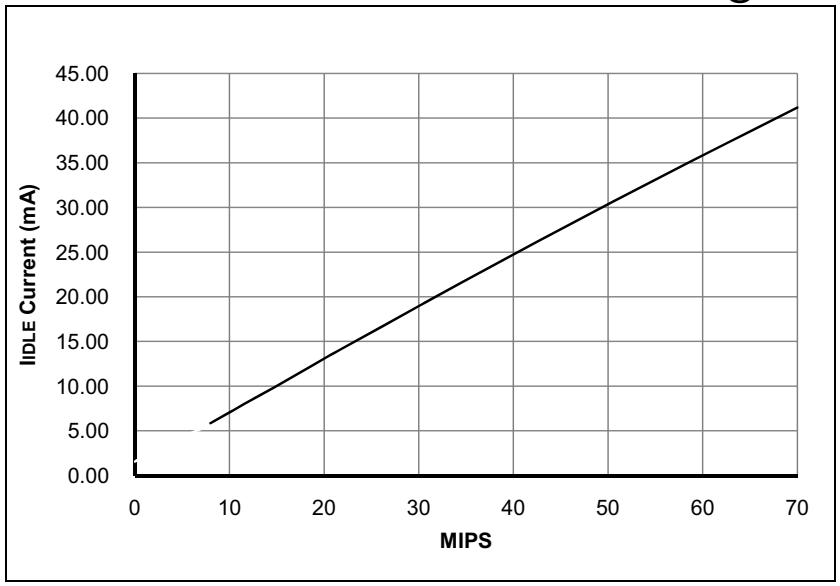


FIGURE 33-8: TYPICAL IIDLE CURRENT – VDD = 3.3V @ +85ºC



APPENDIX A: REVISION HISTORY

Revision A (December 2009)

This is the initial released version of this document.

Revision B (July 2010)

This revision includes minor typographical and formatting changes throughout the data sheet text.

The major changes are referenced by their respective section in Table A-1.

TABLE A-1: MAJOR SECTION UPDATES

Section Name	Update Description
"High-Performance, 16-bit Digital Signal Controllers and Microcontrollers"	Removed reference to dual triggers for Motor Control Peripherals. Relocated the VBUSST pin in all pin diagrams (see **"Pin Diagrams"**, Table 2 and Table 3). Added SCK2, SDI2, SDO2 pins in pin location 4,5 and 6 respectively in 64-pin QFN. Added SCK2, SDI2, SDO2 pins in pin location 4,5 and 6 respectively in 64-pin TQFP. Added SCK2, SDI2, SDO2 pins in pin location 10,11 and 12 respectively in 100-pin TQFP. Added SCK2, SDI2, SDO2 pins in Table 2 and Table 3. Moved the RP30 pin to pin location 95, and the RP31 pin to pin location 96 in the 144-pin TQFP and 144-pin LQFP pin diagrams.
Section 1.0 "Device Overview"	Removed the SCL1 and SDA1 pins from the Pinout I/O Descriptions (see Table 1-1).
Section 2.0 "Guidelines for Getting Started with 16-bit Digital Signal Controllers and Microcontrollers"	Removed Section 2.8 "Configuration of Analog and Digital Pins During ICSP Operations"
Section 3.0 "CPU"	Added Note 4 to the CPU Status Register (SR) in Register 3-1. Added the VAR bit (CORCON<15>) to Register 3-2.

TABLE A-2: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 21.0 "Enhanced CAN (ECAN™) Module"	Added the CANCKS bit to the ECAN Control Register 1 (CiCTRL1) (see Register 21-1).
Section 22.0 "USB On-The-Go (OTG) Module"	Removed the USB 3.3V Regulator logic from the USB Interface Diagram (see Figure 22-1).
Section 23.0 "10-bit/12-bit Analog-to-Digital Converter (ADC)"	Updated the ADC Conversion Clock Period Block Diagram (see Figure 23-2).
Section 29.0 "Special Features"	Updated the last paragraph of **Section 29.1 "Configuration Bits"** Added a note box after the last paragraph of **Section 29.3 "BOR: Brown-out Reset (BOR)"**. Added the RTSP Effect column to the Configuration Bits Description (see Table 29-2).
Section 30.0 "Instruction Set Summary"	Updated all Status Flags Affected to None for the MOV instruction and added Note 2 (see Table 30-2).
Section 32.0 "Electrical Characteristics"	Updated the Absolute Maximum Ratings (see page 457). Added Note 1 to the Operating MIPS vs. Voltage (see Table 32-1). Added parameter DI31 (ICNPD) to the I/O Pin Input Specifications (see Table 32-9). Updated the Minimum value for parameter DO26 in the I/O Pin Output Specifications (see Table 32-10). Updated the Minimum value for parameter D132b and the Minimum and Maximum values for parameters D136a, D136b, D137a, D137b, D138a, and D138b in the Program Memory specification (see Table 32-12). Updated the Minimum, Typical, and Maximum values for parameter OS10 (Oscillator Crystal Frequency: SOSC) in the External Clock Timing Requirements (see Table 32-16). Added Note 2 to the PLL Clock Timing Specifications (see Table 32-17). Updated all Timer1 External Clock Timing Requirements (see Table 32-23). Replaced Table 32-34 with Timer2, Timer4, Timer6, Timer8 External Clock Timing Requirements and Timer3, Timer5, Timer7, Timer9 External Clock Timing Requirements (see Table 32-24 and Table 32-25, respectively). Updated the Maximum value for parameter OC15 and the Minimum value for parameter OC20 in the OC/PWM Mode Timing Requirements (see Table 32-29). Updated the Operating Temperature in the ECAN Module I/O Timing Requirements and USB OTG Timing Requirements (see Table 32-51 and Table 32-53, respectively). Updated all SPI specifications (see Figure 32-15 through Figure 32-30 and Table 32-33 through Table 32-48). Removed Note 4 from the DCI Module Timing Requirements (see Table 32-59). Updated the Standard Operating Conditions voltage for the Comparator Specifications (see Table 32-61 through Table 32-64).