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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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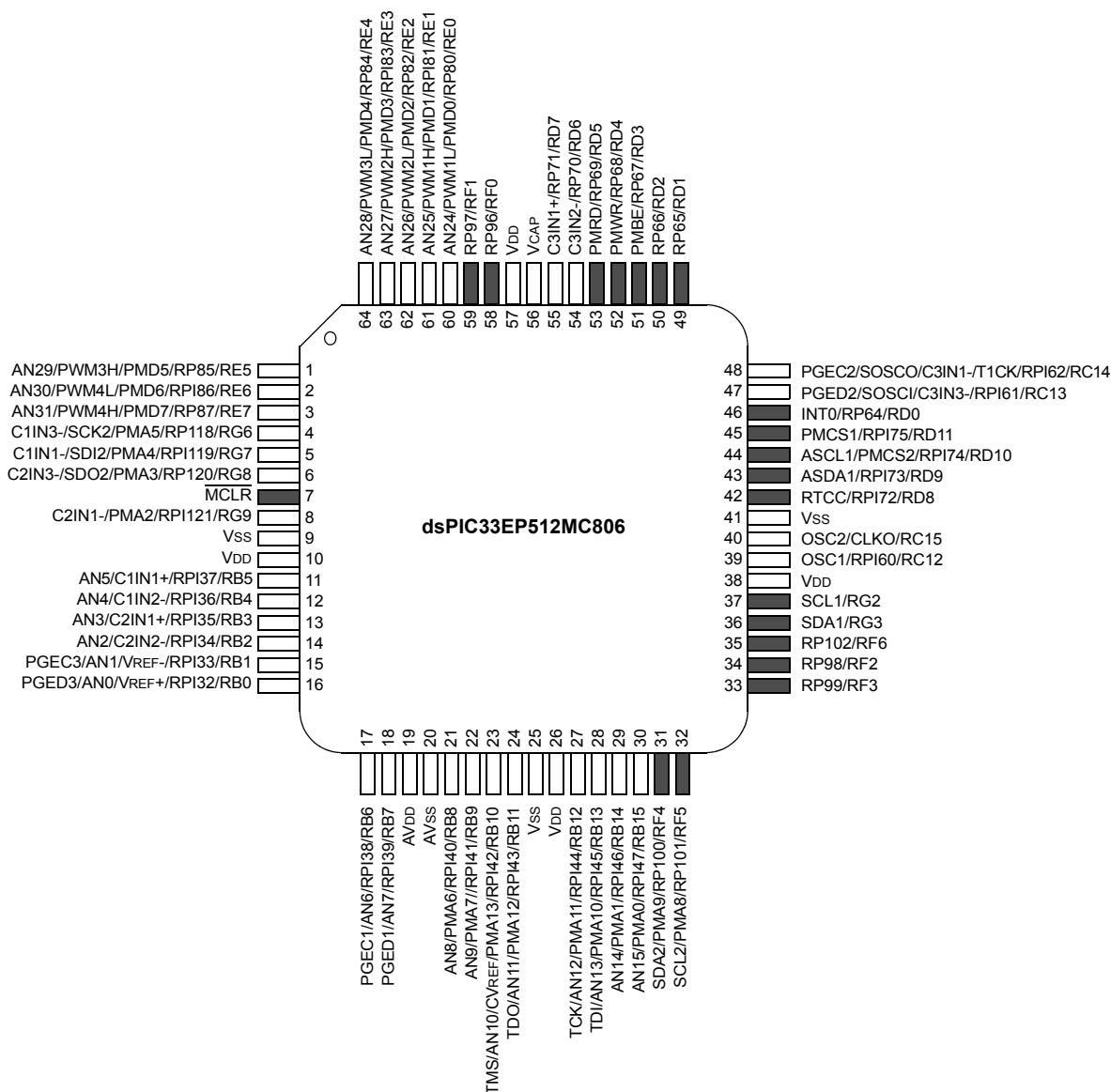
Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512mc806-e-mr

Pin Diagrams (Continued)

64-Pin TQFP

■ = Pins are up to 5V tolerant



Note 1: The RPN/RPIN pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select”** for available peripherals and for information on limitations.

2: Every I/O port pin (RAX-RGx) can be used as change notification (CNAX-CNGx). See **Section 11.0 “I/O Ports”** for more information.

3: The availability of I²C™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 “Special Features”** for more information.

Pin Diagrams (Continued)

121-Pin TFBGA⁽¹⁾

● = Pins are up to 5V tolerant

PIC24EP256GU810
PIC24EP512GU810

	1	2	3	4	5	6	7	8	9	10	11
A	○ RE4	○ RE3	● RG13	○ RE0	● RG0	● RF1	○ VDD	● NC	● RD12	● RD2	● RD1
B	● NC	● RG15	○ RE2	○ RE1	○ RA7	● RF0	○ VCAP	● RD5	● RD3	○ VSS	○ RC14
C	○ RE6	○ VDD	● RG12	● RG14	○ RA6	● NC	○ RD7	● RD4	● NC	○ RC13	● RD11
D	○ RC1	○ RE7	○ RE5	● NC	● NC	● NC	○ RD6	● RD13	● RD0	● NC	● RD10
E	○ RC4	○ RC3	○ RG6	○ RC2	● NC	● RG1	● NC	● RA15	● RD8	● RD9	● RA14
F	● MCLR	○ RG8	○ RG9	○ RG7	○ VSS	● NC	● NC	○ VDD	○ RC12	○ VSS	○ RC15
G	○ RE8	○ RE9	● RA0	● NC	○ VDD	○ VSS	○ VSS	● NC	● RA5	● RA3	● RA4
H	○ RB5	○ RB4	● NC	● NC	● NC	○ VDD	● NC	● VBUS	○ VUSB3V3	○ RG2	● RA2
J	○ RB3	○ RB2	○ RB7	○ AVDD	○ RB11	● RA1	○ RB12	● NC	● NC	● RF8	○ RG3
K	○ RB1	○ RB0	○ RA10	○ RB8	● NC	● RF12	○ RB14	○ VDD	● RD15	● RF3	● RF2
L	○ RB6	○ RA9	○ AVSS	○ RB9	○ RB10	● RF13	○ RB13	○ RB15	● RD14	● RF4	● RF5

Note 1: Refer to Table 3 for full pin names.

Referenced Sources

This device data sheet is based on the following individual chapters of the “*dsPIC33E/PIC24E Family Reference Manual*”. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note: To access the documents listed below, browse to the documentation section of the dsPIC33EP512MU814 product page on the Microchip web site (www.microchip.com).

In the event you are not able to access the product page using the link above, enter this URL in your browser:
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310#1>

- **Section 1. “Introduction”** (DS70573)
- **Section 2. “CPU”** (DS70359)
- **Section 3. “Data Memory”** (DS70595)
- **Section 4. “Program Memory”** (DS70613)
- **Section 5. “Flash Programming”** (DS70609)
- **Section 6. “Interrupts”** (DS70600)
- **Section 7. “Oscillator”** (DS70580)
- **Section 8. “Reset”** (DS70602)
- **Section 9. “Watchdog Timer and Power-Saving Modes”** (DS70615)
- **Section 10. “I/O Ports”** (DS70598)
- **Section 11. “Timers”** (DS70362)
- **Section 12. “Input Capture”** (DS70352)
- **Section 13. “Output Compare”** (DS70358)
- **Section 14. “High-Speed PWM”** (DS70645)
- **Section 15. “Quadrature Encoder Interface (QEI)”** (DS70601)
- **Section 16. “Analog-to-Digital Converter (ADC)”** (DS70621)
- **Section 17. “UART”** (DS70582)
- **Section 18. “Serial Peripheral Interface (SPI)”** (DS70569)
- **Section 19. “Inter-Integrated Circuit™ (I²C™)”** (DS70330)
- **Section 20. “Data Converter Interface (DCI)”** (DS70356)
- **Section 21. “Enhanced Controller Area Network (ECAN™)”** (DS70353)
- **Section 22. “Direct Memory Access (DMA)”** (DS70348)
- **Section 23. “CodeGuard™ Security”** (DS70634)
- **Section 24. “Programming and Diagnostics”** (DS70608)
- **Section 25. “USB On-The-Go (OTG)”** (DS70571)
- **Section 26. “Op Amp/Comparator”** (DS70357)
- **Section 27. “Programmable Cyclic Redundancy Check (CRC)”** (DS70346)
- **Section 28. “Parallel Master Port (PMP)”** (DS70576)
- **Section 29. “Real-Time Clock and Calendar (RTCC)”** (DS70584)
- **Section 30. “Device Configuration”** (DS70618)

TABLE 4-54: DMAC REGISTER MAP (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
DMA4STAL	0B44	STA<15:0>																0000
DMA4STAH	0B46	—	—	—	—	—	—	—	—	STA<23:16>								0000
DMA4STBL	0B48	STB<15:0>																0000
DMA4STBH	0B4A	—	—	—	—	—	—	—	—	STB<23:16>								0000
DMA4PAD	0B4C	PAD<15:0>																0000
DMA4CNT	0B4E	—	—	CNT<13:0>														0000
DMA5CON	0B50	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000
DMA5REQ	0B52	FORCE	—	—	—	—	—	—	—	IRQSEL<7:0>								00FF
DMA5STAL	0B54	STA<15:0>																0000
DMA5STAH	0B56	—	—	—	—	—	—	—	—	STA<23:16>								0000
DMA5STBL	0B58	STB<15:0>																0000
DMA5STBH	0B5A	—	—	—	—	—	—	—	—	STB<23:16>								0000
DMA5PAD	0B5C	PAD<15:0>																0000
DMA5CNT	0B5E	—	—	CNT<13:0>														0000
DMA6CON	0B60	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000
DMA6REQ	0B62	FORCE	—	—	—	—	—	—	—	IRQSEL<7:0>								00FF
DMA6STAL	0B64	STA<15:0>																0000
DMA6STAH	0B66	—	—	—	—	—	—	—	—	STA<23:16>								0000
DMA6STBL	0B68	STB<15:0>																0000
DMA6STBH	0B6A	—	—	—	—	—	—	—	—	STB<23:16>								0000
DMA6PAD	0B6C	PAD<15:0>																0000
DMA6CNT	0B6E	—	—	CNT<13:0>														0000
DMA7CON	0B70	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000
DMA7REQ	0B72	FORCE	—	—	—	—	—	—	—	IRQSEL<7:0>								00FF
DMA7STAL	0B74	STA<15:0>																0000
DMA7STAH	0B76	—	—	—	—	—	—	—	—	STA<23:16>								0000
DMA7STBL	0B78	STB<15:0>																0000
DMA7STBH	0B7A	—	—	—	—	—	—	—	—	STB<23:16>								0000
DMA7PAD	0B7C	PAD<15:0>																0000
DMA7CNT	0B7E	—	—	CNT<13:0>														0000
DMA8CON	0B80	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000
DMA8REQ	0B82	FORCE	—	—	—	—	—	—	—	IRQSEL<7:0>								00FF
DMA8STAL	0B84	STA<15:0>																0000
DMA8STAH	0B86	—	—	—	—	—	—	—	—	STA<23:16>								0000
DMA8STBL	0B88	STB<15:0>																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 7-1: INTERRUPT VECTOR DETAILS (CONTINUED)

Interrupt Source	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
				Flag	Enable	Priority
USB1 – USB OTG Interrupt ⁽²⁾	94	86	0x0000C0	IFS5<6>	IEC5<6>	IPC21<10:8>
U4E – UART4 Error Interrupt	95	87	0x0000C2	IFS5<7>	IEC5<7>	IPC21<14:12>
U4RX – UART4 Receiver	96	88	0x0000C4	IFS5<8>	IEC5<8>	IPC22<2:0>
U4TX – UART4 Transmitter	97	89	0x0000C6	IFS5<9>	IEC5<9>	IPC22<6:4>
SPI3E – SPI3 Error	98	90	0x0000C8	IFS5<10>	IEC5<10>	IPC22<10:8>
SPI3 – SPI3 Transfer Done	99	91	0x0000CA	IFS5<11>	IEC5<11>	IPC22<14:12>
OC9 – Output Compare 9	100	92	0x0000CC	IFS5<12>	IEC5<12>	IPC23<2:0>
IC9 – Input Capture 9	101	93	0x0000CE	IFS5<13>	IEC5<13>	IPC23<6:4>
PWM1 – PWM Generator 1 ⁽¹⁾	102	94	0x0000D0	IFS5<14>	IEC5<14>	IPC23<10:8>
PWM2 – PWM Generator 2 ⁽¹⁾	103	95	0x0000D2	IFS5<15>	IEC5<15>	IPC23<14:12>
PWM3 – PWM Generator 3 ⁽¹⁾	104	96	0x0000D4	IFS6<0>	IEC6<0>	IPC24<2:0>
PWM4 – PWM Generator 4 ⁽¹⁾	105	97	0x0000D6	IFS6<1>	IEC6<1>	IPC24<6:4>
PWM5 – PWM Generator 5 ⁽¹⁾	106	98	0x0000D8	IFS6<2>	IEC6<2>	IPC24<10:8>
PWM6 – PWM Generator 6 ⁽¹⁾	107	99	0x0000DA	IFS6<3>	IEC6<3>	IPC24<14:12>
PWM7 – PWM Generator 7 ⁽¹⁾	108	100	0x0000DC	IFS6<4>	IEC6<4>	IPC25<2:0>
Reserved	109-125	101-117	0x0000DE-0x0000FC	—	—	—
DMA8 – DMA Channel 8	126	118	0x000100	IFS7<6>	IEC7<6>	IPC29<10:8>
DMA9 – DMA Channel 9	127	119	0x000102	IFS7<7>	IEC7<7>	IPC29<14:12>
DMA10 – DMA Channel 10	128	120	0x000104	IFS7<8>	IEC7<8>	IPC30<2:0>
DMA11 – DMA Channel 11	129	121	0x000106	IFS7<9>	IEC7<9>	IPC30<6:4>
SPI4E – SPI4 Error	130	122	0x000108	IFS7<10>	IEC7<10>	IPC30<10:8>
SPI4 – SPI4 Transfer Done	131	123	0x00010A	IFS7<11>	IEC7<11>	IPC30<14:12>
OC10 – Output Compare 10	132	124	0x00010C	IFS7<12>	IEC7<12>	IPC31<2:0>
IC10 – Input Capture 10	133	125	0x00010E	IFS7<13>	IEC7<13>	IPC31<6:4>
OC11 – Output Compare 11	134	126	0x000110	IFS7<14>	IEC7<14>	IPC31<10:8>
IC11 – Input Capture 11	135	127	0x000112	IFS7<15>	IEC7<15>	IPC31<14:12>
OC12 – Output Compare 12	136	128	0x000114	IFS8<0>	IEC8<0>	IPC32<2:0>
IC12 – Input Capture 12	137	129	0x000116	IFS8<1>	IEC8<1>	IPC32<6:4>
DMA12 – DMA Channel 12	138	130	0x000118	IFS8<2>	IEC8<2>	IPC32<10:8>
DMA13 – DMA Channel 13	139	131	0x00011A	IFS8<3>	IEC8<3>	IPC32<14:12>
DMA14 – DMA Channel 14	140	132	0x00011C	IFS8<4>	IEC8<4>	IPC33<2:0>
Reserved	141	133	0x00011E	—	—	—
OC13 – Output Compare 13	142	134	0x000120	IFS8<6>	IEC8<6>	IPC33<10:8>
IC13 – Input Capture 13	143	135	0x000122	IFS8<7>	IEC8<7>	IPC33<14:12>
OC14 – Output Compare 14	144	136	0x000124	IFS8<8>	IEC8<8>	IPC34<2:0>
IC14 – Input Capture 14	145	137	0x000126	IFS8<9>	IEC8<9>	IPC34<6:4>
OC15 – Output Compare 15	146	138	0x000128	IFS8<10>	IEC8<10>	IPC34<10:8>
IC15 – Input Capture 15	147	139	0x00012A	IFS8<11>	IEC8<11>	IPC34<14:12>
OC16 – Output Compare 16	148	140	0x00012C	IFS8<12>	IEC8<12>	IPC35<2:0>
IC16 – Input Capture 16	149	141	0x00012E	IFS8<13>	IEC8<13>	IPC35<6:4>
ICD – ICD Application	150	142	0x000130	IFS8<14>	IEC8<14>	IPC35<10:8>
Reserved	151-245	142-237	0x000130-0x0001FE	—	—	—
Lowest Natural Order Priority						

Note 1: This interrupt source is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

Note 2: This interrupt source is available on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices only.

REGISTER 8-11: DMAPWC: DMA PERIPHERAL WRITE COLLISION STATUS REGISTER

U-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
—	PWCOL14	PWCOL13	PWCOL12	PWCOL11	PWCOL10	PWCOL9	PWCOL8
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
PWCOL7	PWCOL6	PWCOL5	PWCOL4	PWCOL3	PWCOL2	PWCOL1	PWCOL0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **Unimplemented:** Read as '0'
- bit 14 **PWCOL14:** Channel 14 Peripheral Write Collision Flag bit
 1 = Write collision detected
 0 = No write collision detected
- bit 13 **PWCOL13:** Channel 13 Peripheral Write Collision Flag bit
 1 = Write collision detected
 0 = No write collision detected
- bit 12 **PWCOL12:** Channel 12 Peripheral Write Collision Flag bit
 1 = Write collision detected
 0 = No write collision detected
- bit 11 **PWCOL11:** Channel 11 Peripheral Write Collision Flag bit
 1 = Write collision detected
 0 = No write collision detected
- bit 10 **PWCOL10:** Channel 10 Peripheral Write Collision Flag bit
 1 = Write collision detected
 0 = No write collision detected
- bit 9 **PWCOL9:** Channel 9 Peripheral Write Collision Flag bit
 1 = Write collision detected
 0 = No write collision detected
- bit 8 **PWCOL8:** Channel 8 Peripheral Write Collision Flag bit
 1 = Write collision detected
 0 = No write collision detected
- bit 7 **PWCOL7:** Channel 7 Peripheral Write Collision Flag bit
 1 = Write collision detected
 0 = No write collision detected
- bit 6 **PWCOL6:** Channel 6 Peripheral Write Collision Flag bit
 1 = Write collision detected
 0 = No write collision detected
- bit 5 **PWCOL5:** Channel 5 Peripheral Write Collision Flag bit
 1 = Write collision detected
 0 = No write collision detected
- bit 4 **PWCOL4:** Channel 4 Peripheral Write Collision Flag bit
 1 = Write collision detected
 0 = No write collision detected
- bit 3 **PWCOL3:** Channel 3 Peripheral Write Collision Flag bit
 1 = Write collision detected
 0 = No write collision detected

TABLE 11-1: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION) (CONTINUED)

Input Name ⁽¹⁾	Function Name	Register	Configuration Bits
DCI Data Input	CSDI	RPINR24	CSDIR<6:0>
DCI Clock Input	CCKIN	RPINR24	CCKR<6:0>
DCI FSYNC Input	COFSIN	RPINR25	COFSR<6:0>
CAN1 Receive	C1RX	RPINR26	C1RXR<6:0>
CAN2 Receive	C2RX	RPINR26	C2RXR<6:0>
UART3 Receive	U3RX	RPINR27	U3RXR<6:0>
UART3 Clear-to-Send	U3CTS	RPINR27	U3CTSR<6:0>
UART4 Receive	U4RX	RPINR28	U4RXR<6:0>
UART4 Clear-to-Send	U4CTS	RPINR28	U4CTSR<6:0>
SPI3 Data Input	SDI3	RPINR29	SDI3R<6:0>
SPI3 Clock Input	SCK3	RPINR29	SCK3R<6:0>
SPI3 Slave Select	SS3	RPINR30	SS3R<6:0>
SPI4 Data Input	SDI4	RPINR31	SDI4R<6:0>
SPI4 Clock Input	SCK4	RPINR31	SCK4R<6:0>
SPI4 Slave Select	SS4	RPINR32	SS4R<6:0>
Input Capture 9	IC9	RPINR33	IC9R<6:0>
Input Capture 10	IC10	RPINR33	IC10R<6:0>
Input Capture 11	IC11	RPINR34	IC11R<6:0>
Input Capture 12	IC12	RPINR34	IC12R<6:0>
Input Capture 13	IC13	RPINR35	IC13R<6:0>
Input Capture 14	IC14	RPINR35	IC14R<6:0>
Input Capture 15	IC15	RPINR36	IC15R<6:0>
Input Capture 16	IC16	RPINR36	IC16R<6:0>
Output Compare Fault C	OCFC	RPINR37	OCFCR<6:0>
PWM Fault 5 ⁽²⁾	FLT5	RPINR42	FLT5R<6:0>
PWM Fault 6 ⁽²⁾	FLT6	RPINR42	FLT6R<6:0>
PWM Fault 7 ⁽²⁾	FLT7	RPINR43	FLT7R<6:0>
PWM Dead-Time Compensation 1 ⁽²⁾	DTCMP1	RPINR38	DTCMP1R<6:0>
PWM Dead-Time Compensation 2 ⁽²⁾	DTCMP2	RPINR39	DTCMP2R<6:0>
PWM Dead-Time Compensation 3 ⁽²⁾	DTCMP3	RPINR39	DTCMP3R<6:0>
PWM Dead-Time Compensation 4 ⁽²⁾	DTCMP4	RPINR40	DTCMP4R<6:0>
PWM Dead-Time Compensation 5 ⁽²⁾	DTCMP5	RPINR40	DTCMP5R<6:0>
PWM Dead-Time Compensation 6 ⁽²⁾	DTCMP6	RPINR41	DTCMP6R<6:0>
PWM Dead-Time Compensation 7 ⁽²⁾	DTCMP7	RPINR41	DTCMP7R<6:0>
PWM Synch Input 1 ⁽²⁾	SYNCI1	RPINR37	SYNCI1R<6:0>
PWM Synch Input 2 ⁽²⁾	SYNCI2	RPINR38	SYNCI2R<6:0>

Note 1: Unless otherwise noted, all inputs use the Schmitt Trigger input buffers.

2: This input source is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

REGISTER 11-6: RPINR5: PERIPHERAL PIN SELECT INPUT REGISTER 5

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	T7CKR<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	T6CKR<6:0>						
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'bit 14-8 **T7CKR<6:0>:** Assign Timer7 External Clock (T7CK) to the Corresponding RPN/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'bit 6-0 **T6CKR<6:0>:** Assign Timer6 External Clock (T6CK) to the Corresponding RPN/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

REGISTER 11-53: RPOR9: PERIPHERAL PIN SELECT OUTPUT REGISTER 9

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP101R<5:0>					
bit 15							
							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP100R<5:0>					
bit 7							
							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13-8 **RP101R<5:0>:** Peripheral Output Function is Assigned to RP101 Output Pin bits
 (see Table 11-3 for peripheral function numbers)
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **RP100R<5:0>:** Peripheral Output Function is Assigned to RP100 Output Pin bits
 (see Table 11-3 for peripheral function numbers)

REGISTER 11-54: RPOR10: PERIPHERAL PIN SELECT OUTPUT REGISTER 10

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							
							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP102R<5:0>					
bit 7							
							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-6 **Unimplemented:** Read as '0'
- bit 5-0 **RP102R<5:0>:** Peripheral Output Function is Assigned to RP102 Output Pin bits
 (see Table 11-3 for peripheral function numbers)

NOTES:

REGISTER 16-11: PWMCONx: PWMx CONTROL REGISTER (CONTINUED)

bit 7-6	DTC<1:0> : Dead-Time Control bits 11 = Dead-Time Compensation mode 10 = Dead-time function is disabled 01 = Negative dead time actively applied for Complementary Output mode 00 = Positive dead time actively applied for all output modes
bit 5	DTCP : Dead-Time Compensation Polarity bit ⁽³⁾ <u>When set to '1':</u> If DTCMPx = 0, PWMxL is shortened and PWMxH is lengthened. If DTCMPx = 1, PWMxH is shortened and PWMxL is lengthened. <u>When set to '0':</u> If DTCMPx = 0, PWMxH is shortened and PWMxL is lengthened. If DTCMPx = 1, PWMxL is shortened and PWMxH is lengthened.
bit 4	Unimplemented : Read as '0'
bit 3	MTBS : Master Time Base Select bit 1 = PWM generator uses the secondary master time base for synchronization and as the clock source for the PWM generation logic (if secondary time base is available) 0 = PWM generator uses the primary master time base for synchronization and as the clock source for the PWM generation logic
bit 2	CAM : Center-Aligned Mode Enable bit ^(2,4) 1 = Center-Aligned mode is enabled 0 = Edge-Aligned mode is enabled
bit 1	XPRES : External PWM Reset Control bit ⁽⁵⁾ 1 = Current-limit source resets the time base for this PWM generator if it is in Independent Time Base mode 0 = External pins do not affect PWM time base
bit 0	IUE : Immediate Update Enable bit ⁽²⁾ 1 = Updates to the active MDC/PDCx/SDCx registers are immediate 0 = Updates to the active PDCx registers are synchronized to the PWM time base

- Note 1:** Software must clear the interrupt status here and in the corresponding IFS bit in the interrupt controller.
- 2:** These bits should not be changed after the PWM is enabled (PTEN = 1).
- 3:** DTC<1:0> = 11 for DTCP to be effective; otherwise, DTCP is ignored.
- 4:** The Independent Time Base (ITB = 1) mode must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
- 5:** To operate in External Period Reset mode, the ITB bit must be '1' and the CLMOD bit in the FCLCONx register must be '0'.

REGISTER 16-16: DTRx: PWMx DEAD-TIME REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DTRx<13:8>					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTRx<7:0>							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'bit 13-0 **DTRx<13:0>:** Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits**REGISTER 16-17: ALTDTRx: PWMx ALTERNATE DEAD-TIME REGISTER**

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	ALTDTRx<13:8>					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ALTDTRx<7:0>							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'bit 13-0 **ALTDTRx<13:0>:** Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

REGISTER 16-19: IOCONx: PWMx I/O CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PENH	PENL	POLH	POLL	PMOD<1:0> ⁽¹⁾		OVRENH	OVRENL
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

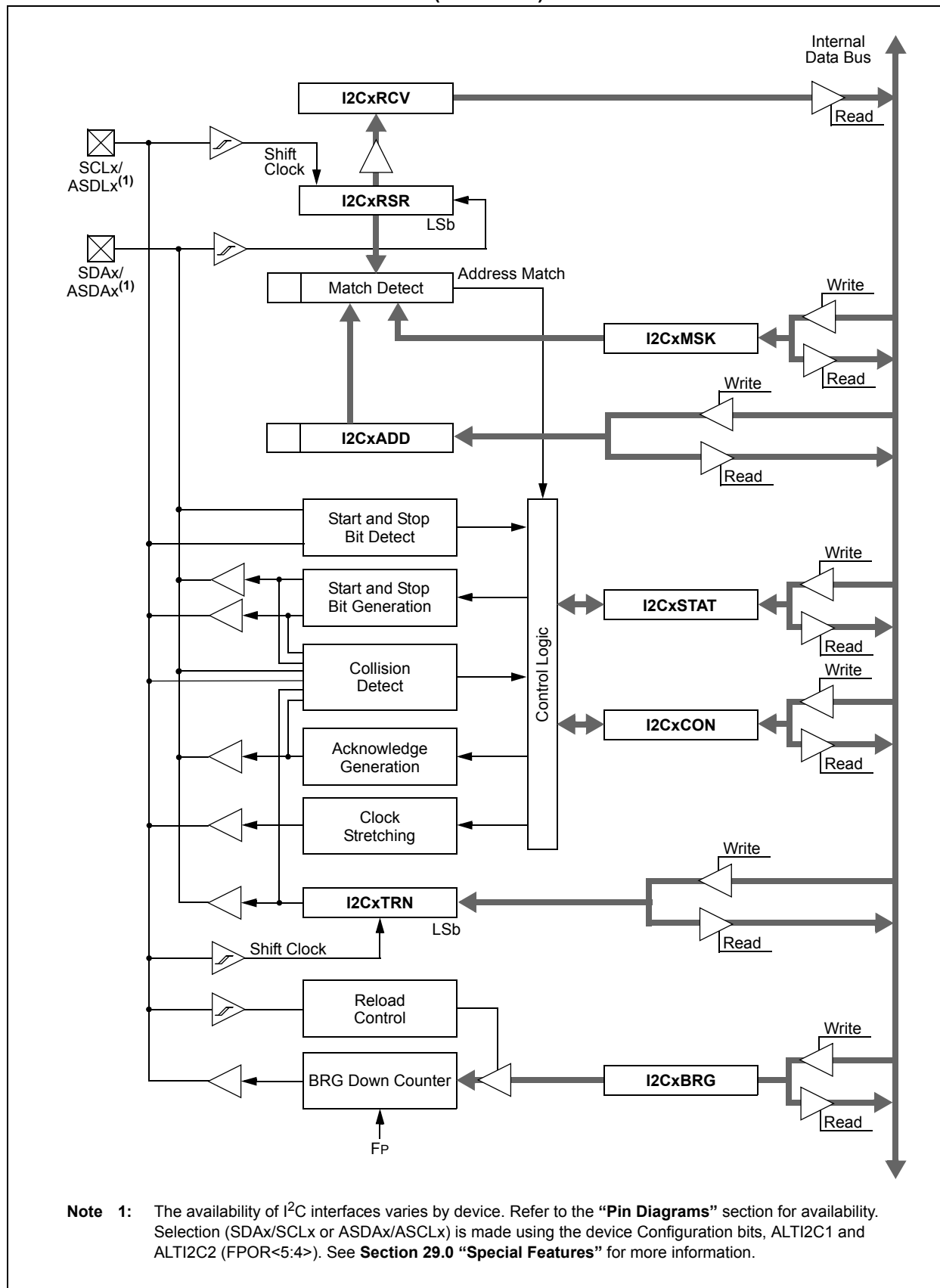
'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **PENH:** PWMxH Output Pin Ownership bit
 1 = PWM module controls PWMxH pin
 0 = GPIO module controls PWMxH pin
- bit 14 **PENL:** PWMxL Output Pin Ownership bit
 1 = PWM module controls PWMxL pin
 0 = GPIO module controls PWMxL pin
- bit 13 **POLH:** PWMxH Output Pin Polarity bit
 1 = PWMxH pin is active-low
 0 = PWMxH pin is active-high
- bit 12 **POLL:** PWMxL Output Pin Polarity bit
 1 = PWMxL pin is active-low
 0 = PWMxL pin is active-high
- bit 11-10 **PMOD<1:0>:** PWM # I/O Pin Mode bits⁽¹⁾
 11 = PWM I/O pin pair is in the True Independent Output mode
 10 = PWM I/O pin pair is in the Push-Pull Output mode
 01 = PWM I/O pin pair is in the Redundant Output mode
 00 = PWM I/O pin pair is in the Complementary Output mode
- bit 9 **OVRENH:** Override Enable for PWMxH Pin bit
 1 = OVRDAT<1> controls output on PWMxH pin
 0 = PWM generator controls PWMxH pin
- bit 8 **OVRENL:** Override Enable for PWMxL Pin bit
 1 = OVRDAT<0> controls output on PWMxL pin
 0 = PWM generator controls PWMxL pin
- bit 7-6 **OVRDAT<1:0>:** Data for PWMxH, PWMxL Pins if Override is Enabled bits
 If OVERENH = 1, PWMxH is driven to the state specified by OVRDAT<1>.
 If OVERENL = 1, PWMxL is driven to the state specified by OVRDAT<0>.
- bit 5-4 **FLTDAT<1:0>:** Data for PWMxH and PWMxL Pins if FLTMOD is Enabled bits
 If FLTMOD (FCLCONx<15>) = 0: Normal Fault mode:
 If Fault is active, PWMxH is driven to the state specified by FLTDAT<1>.
 If Fault is active, PWMxL is driven to the state specified by FLTDAT<0>.
 If FLTMOD (FCLCONx<15>) = 1: Independent Fault mode:
 If current limit is active, PWMxH is driven to the state specified by FLTDAT<1>.
 If Fault is active, PWMxL is driven to the state specified by FLTDAT<0>.

Note 1: These bits should not be changed after the PWM module is enabled (PTEN = 1).

FIGURE 19-1: I²C™ BLOCK DIAGRAM (x = 1 OR 2)

REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

- bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled; if 9-bit mode is not selected, this does not take effect
0 = Address Detect mode is disabled
- bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Receiver is active
- bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character (character at the top of the receive FIFO)
0 = Parity error has not been detected
- bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character (character at the top of the receive FIFO)
0 = Framing error has not been detected
- bit 1 **OERR:** Receive Buffer Overrun Error Status bit (read/clear only)
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed; clearing a previously set OERR bit (1 → 0 transition) resets the receiver buffer and the UxRSR to the empty state
- bit 0 **URXDA:** Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

Note 1: Refer to **Section 17. “UART”** (DS70582) in the “*dsPIC33E/PIC24E Family Reference Manual*” for information on enabling the UARTx module for transmit operation.

REGISTER 23-4: ADxCON3: ADCx CONTROL REGISTER 3

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADRC	—	—	SAMC<4:0> ⁽¹⁾				
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS<7:0> ^(2,3)							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **ADRC:** ADC Conversion Clock Source bit

1 = ADC internal RC clock

0 = Clock Derived From System Clock

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits⁽¹⁾

11111 = 31 TAD

•

•

•

00001 = 1 TAD

00000 = 0 TAD

bit 7-0 **ADCS<7:0>:** ADC Conversion Clock Select bits^(2,3)

11111111 = $T_P \cdot (ADCS<7:0> + 1) = 256 \cdot T_{CY} = T_{AD}$

•

•

•

00000010 = $T_P \cdot (ADCS<7:0> + 1) = 3 \cdot T_{CY} = T_{AD}$

00000001 = $T_P \cdot (ADCS<7:0> + 1) = 2 \cdot T_{CY} = T_{AD}$

00000000 = $T_P \cdot (ADCS<7:0> + 1) = 1 \cdot T_{CY} = T_{AD}$

Note 1: This bit is only used if ADxCON1<7:5> (SSRC<2:0>) = 111 and ADxCON1<4> (SSRCG) = 0.

2: This bit is not used if ADxCON3<15> (ADRC) = 1.

3: $T_P = 1/F_P$.

25.2 Comparator Control Registers

REGISTER 25-1: CMSTAT: COMPARATOR STATUS REGISTER

R/W-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
CMSIDL	—	—	—	—	C3EVT	C2EVT	C1EVT
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
—	—	—	—	—	C3OUT	C2OUT	C1OUT
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **CMSIDL:** Comparator Stop in Idle Mode bit
1 = Discontinues operation of all comparators when device enters Idle mode
0 = Continues operation of all comparators in Idle mode
- bit 14-11 **Unimplemented:** Read as '0'
- bit 10 **C3EVT:** Comparator 3 Event Status bit
1 = Comparator event occurred
0 = Comparator event did not occur
- bit 9 **C2EVT:** Comparator 2 Event Status bit
1 = Comparator event occurred
0 = Comparator event did not occur
- bit 8 **C1EVT:** Comparator 1 Event Status bit
1 = Comparator event occurred
0 = Comparator event did not occur
- bit 7-3 **Unimplemented:** Read as '0'
- bit 2 **C3OUT:** Comparator 3 Output Status bit
When CPOL = 0:
1 = $V_{IN+} > V_{IN-}$
0 = $V_{IN+} < V_{IN-}$
When CPOL = 1:
1 = $V_{IN+} < V_{IN-}$
0 = $V_{IN+} > V_{IN-}$
- bit 1 **C2OUT:** Comparator 2 Output Status bit
When CPOL = 0:
1 = $V_{IN+} > V_{IN-}$
0 = $V_{IN+} < V_{IN-}$
When CPOL = 1:
1 = $V_{IN+} < V_{IN-}$
0 = $V_{IN+} > V_{IN-}$
- bit 0 **C1OUT:** Comparator 1 Output Status bit
When CPOL = 0:
1 = $V_{IN+} > V_{IN-}$
0 = $V_{IN+} < V_{IN-}$
When CPOL = 1:
1 = $V_{IN+} < V_{IN-}$
0 = $V_{IN+} > V_{IN-}$

31.7 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

31.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC® Flash MCUs and dsPIC® Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

31.9 MPLAB ICD 3 In-Circuit Debugger System

MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost effective high-speed hardware debugger/programmer for Microchip Flash Digital Signal Controller (DSC) and microcontroller (MCU) devices. It debugs and programs PIC® Flash microcontrollers and dsPIC® DSCs with the powerful, yet easy-to-use graphical user interface of MPLAB Integrated Development Environment (IDE).

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

31.10 PICKit 3 In-Circuit Debugger/Programmer and PICKit 3 Debug Express

The MPLAB PICKit 3 allows debugging and programming of PIC® and dsPIC® Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB Integrated Development Environment (IDE). The MPLAB PICKit 3 is connected to the design engineer's PC using a full speed USB interface and can be connected to the target via an Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the reset line to implement in-circuit debugging and In-Circuit Serial Programming™.

The PICKit 3 Debug Express include the PICKit 3, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

TABLE 32-17: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T _A ≤ +85°C for Industrial -40°C ≤ T _A ≤ +125°C for Extended				
Param.	Symbol	Characteristic	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
OS50	FPLLI	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range	0.8	—	8.0	MHz	ECPLL, XTPLL modes
OS51	FSYS	On-Chip VCO System Frequency	120	—	340	MHz	
OS52	TLOCK	PLL Start-up Time (Lock Time)	0.9	1.5	3.1	mS	
OS53	DCLK	CLKO Stability (Jitter) ⁽²⁾	-5	0.5	5	%	

Note 1: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: This jitter specification is based on clock cycle-by-clock cycle measurements. To get the effective jitter for individual time bases or communication clocks used by the application, use the following formula:

$$\text{Effective Jitter} = \frac{DCLK}{\sqrt{\frac{FOSC}{\text{Time Base or Communication Clock}}}}$$

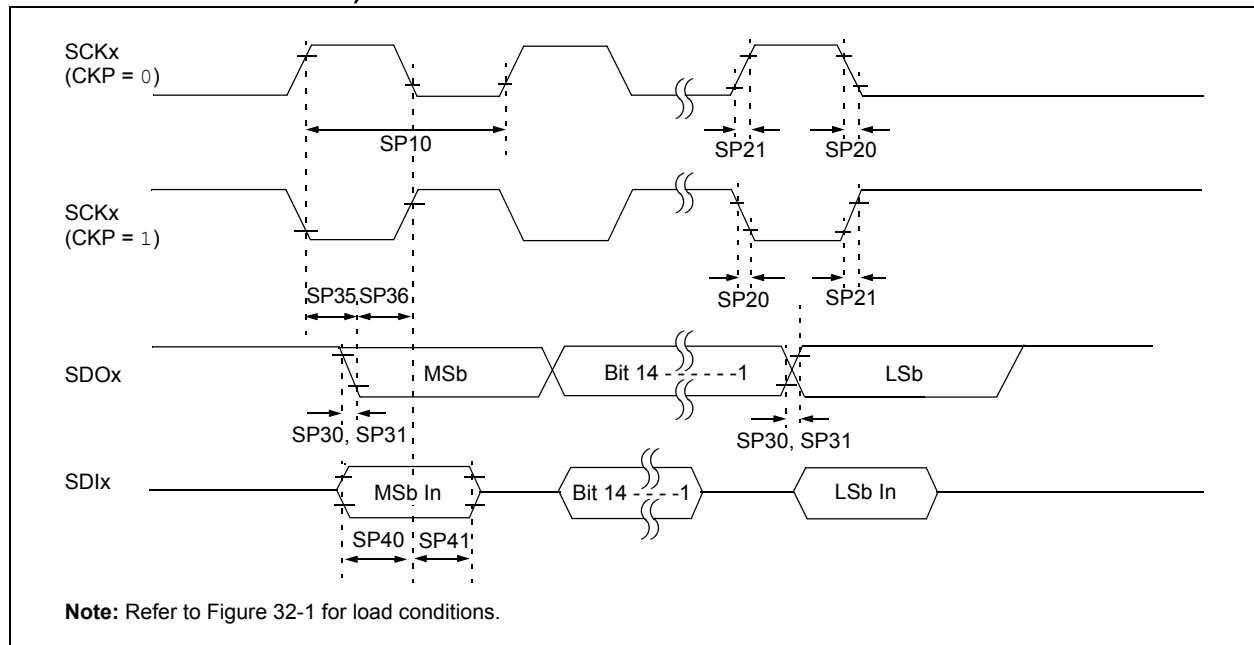
For example, if Fosc = 120 MHz and the SPI bit rate = 10 MHz, the effective jitter is as follows:

$$\text{Effective Jitter} = \frac{DCLK}{\sqrt{\frac{120}{10}}} = \frac{DCLK}{\sqrt{12}} = \frac{DCLK}{3.464}$$

TABLE 32-18: AUXILIARY PLL CLOCK TIMING SPECIFICATIONS
(dsPIC33EPXXXMU8XX AND PIC24EPXXXGU8XX DEVICES ONLY)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T _A ≤ +85°C for Industrial -40°C ≤ T _A ≤ +125°C for Extended				
Param.	Symbol	Characteristic	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
OS54	AFPLLI	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range	3	—	5.5	MHz	ECPLL, XTPLL modes
OS55	AFSYS	On-Chip VCO System Frequency	60	—	120	MHz	
OS56	ATLOCK	PLL Start-up Time (Lock Time)	0.9	1.5	3.1	mS	
OS57	ADCLK	CLKO Stability (Jitter)	-2	0.25	2	%	

Note 1: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 32-18: SPI1, SPI3 AND SPI4 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS**TABLE 32-36: SPI1, SPI3 AND SPI4 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP10	TscP	Maximum SCKx Frequency	—	—	9	MHz	-40°C to +125°C and see Note 3
SP20	TscF	SCKx Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP21	TscR	SCKx Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid After SCKx Edge	—	6	20	ns	
SP36	TdoV2sch, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2sch, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

Note 2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

Note 3: The minimum clock period for SCKx is 111 ns. The clock generated in Master mode must not violate this specification.

Note 4: Assumes 50 pF load on all SPIx pins.