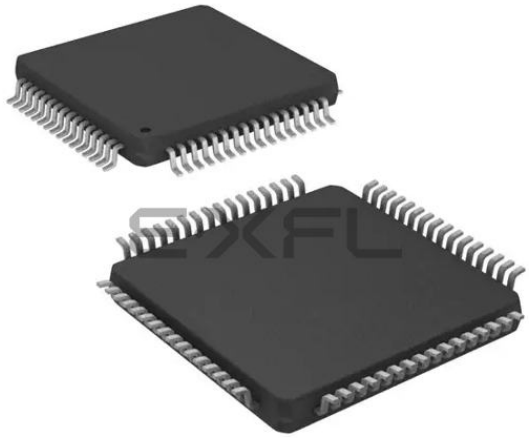
Microchip Technology - DSPIC33EP512MC806-I/PT Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

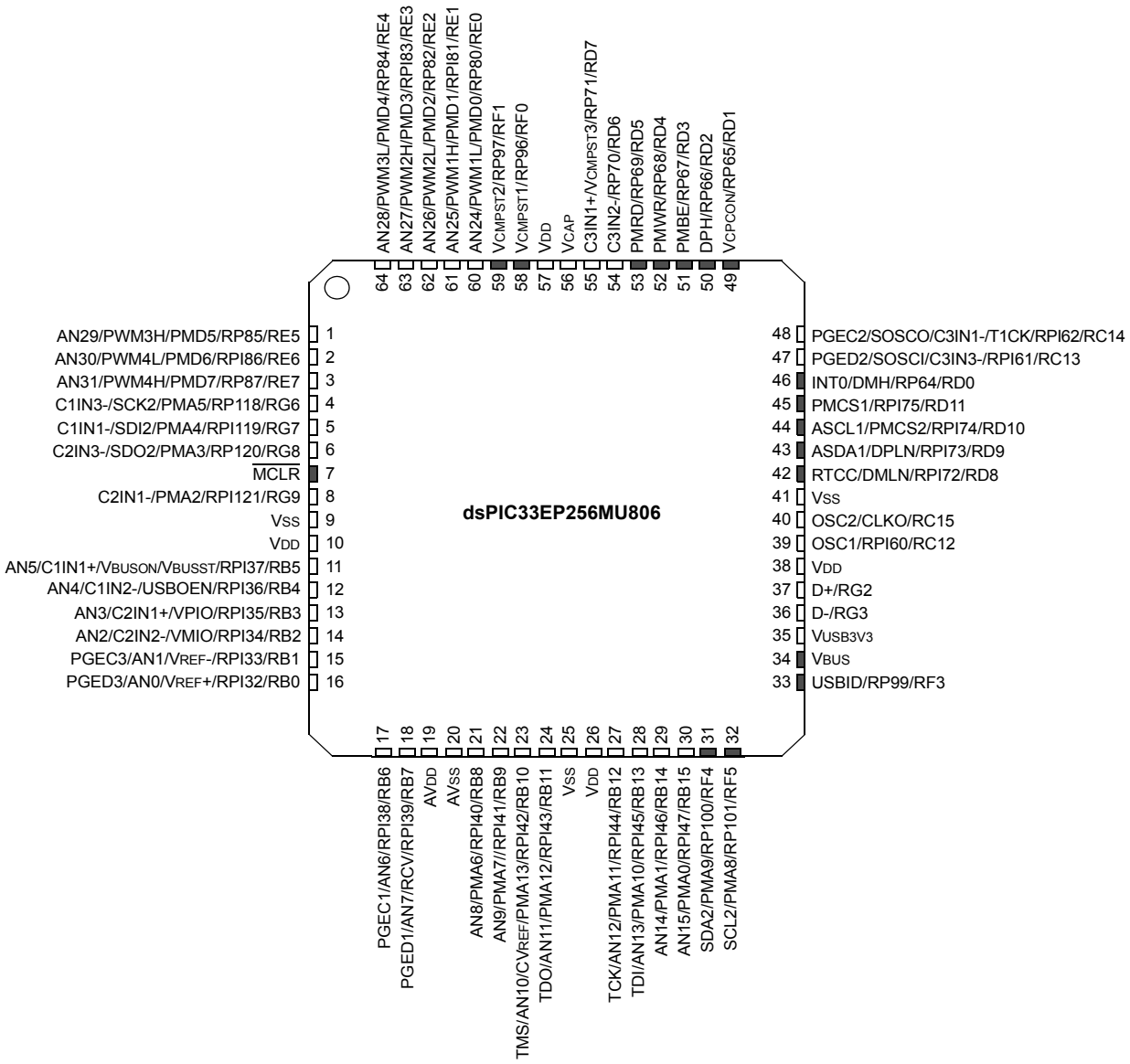
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512mc806-i-pt

Pin Diagrams

64-Pin QFN

■ = Pins are up to 5V tolerant



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The availability of I^2C™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

Pin Diagrams (Continued)

100-Pin TQFP

■ = Pins are up to 5V tolerant

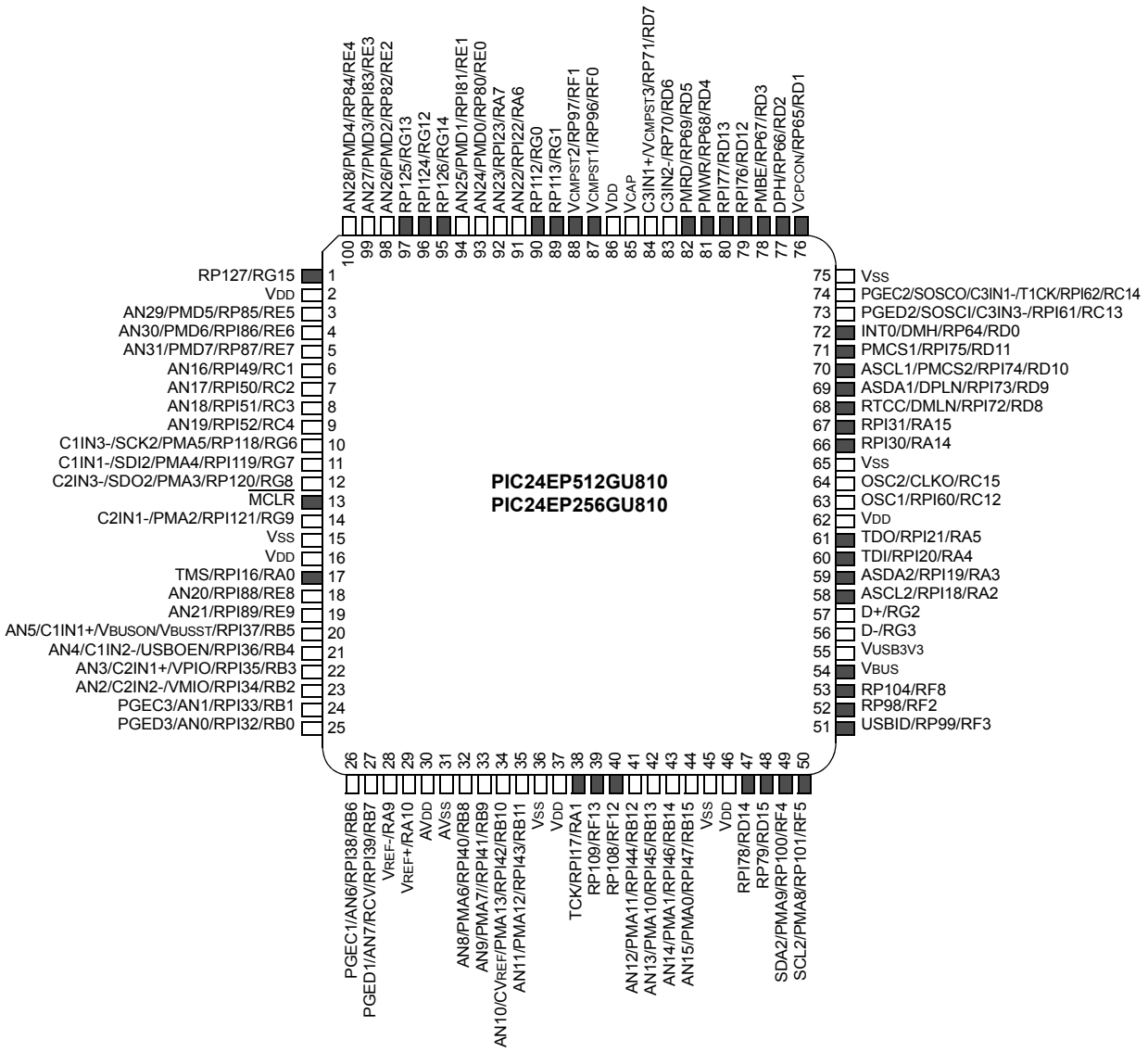


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TABLE 3: PIN NAMES: PIC24EP256GU810 AND PIC24EP512GU810 DEVICES(1,2) (CONTINUED)

Pin Number	Full Pin Name
E1	AN19/RPI52/RC4
E2	AN18/RPI51/RC3
E3	C1IN3-/SCK2/PMA5/RP118/RG6
E4	AN17/RPI50/RC2
E5	No Connect
E6	RP113/RG1
E7	No Connect
K4	AN8/PMA6/RPI40/RB8
K5	No Connect
K6	RP108/RF12
K7	AN14/PMA1/RPI46/RB14
K8	VDD
K9	RP79/RD15
K10	USBID/RP99/RF3
K11	RP98/RF2
L1	PGEC1/AN6/RPI38/RB6
L2	VREF-/RA9

Pin Number	Full Pin Name
J8	No Connect
J9	No Connect
J10	RP104/RF8
J11	D-/RG3(5)
K1	PGEC3/AN1/RPI33/RB1
K2	PGED3/AN0/RPI32/RB0
K3	VREF+/RA10
L3	AVSS
L4	AN9/PMA7/RPI41/RB9
L5	AN10/CVREF/PMA13/RPI42/RB10
L6	RP109/RF13
L7	AN13/PMA10/RPI45/RB13
L8	AN15/PMA0/RPI47/RB15
L9	RPI78/RD14
L10	SDA2(3)/PMA9/RP100/RF4
L11	SCL2(3)/PMA8/RP101/RF5

Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The availability of I^2C™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

4: The pin name is SCL1/RG2 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.

5: The pin name is SDA1/RG3 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	PPS	Description
C2IN1+, C2IN2-, C2IN1-, C2IN3-	I	Analog	No	Comparator 2 inputs.
C2OUT	O	—	Yes	Comparator 2 output.
C3IN1+, C3IN2-, C2IN1-, C3IN3-	I	Analog	No	Comparator 3 inputs.
C3OUT	O	—	Yes	Comparator 3 output.
PMA0	I/O	TTL/ST	No	Parallel Master Port Address Bit 0 input (Buffered Slave modes) and output (Master modes).
PMA1	I/O	TTL/ST	No	Parallel Master Port Address Bit 1 input (Buffered Slave modes) and output (Master modes).
PMA2 -PMA13	O	—	No	Parallel Master Port Address Bits 2-13 (Demultiplexed Master modes).
PMBE	O	—	No	Parallel Master Port byte enable strobe.
PMCS1, PMCS2	O	—	No	Parallel Master Port Chip Select 1 and 2 strobe.
PMD0-PMD7	I/O	TTL/ST	No	Parallel Master Port data (Demultiplexed Master mode) or address/data (Multiplexed Master modes).
PMRD	O	—	No	Parallel Master Port read strobe.
PMWR	O	—	No	Parallel Master Port write strobe.
$\overline{FLT1}$-$\overline{FLT7}$**(1)**	I	ST	Yes	PWM Fault Input 1 through 7.
DTCMP1-DTCMP7**(1)**	I	ST	Yes	PWM dead-time compensation input.
PWM1L-PWM7L**(1)**	O	—	No	PWM Low Output 1 through 7.
PWM1H-PWM7H**(1)**	O	—	No	PWM High Output 1 through 7.
SYNCI1, SYNCI2**(1)**	I	ST	Yes	PWM Synchronization Inputs 1 and 2.
SYNCO1, SYNCO2**(1)**	O	—	Yes	PWM Synchronization Outputs 1 and 2.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

Note 1: This pin is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

2: AVDD must be connected at all times.

3: These pins are input only on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices.

4: These pins are only available on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices.

5: The availability of I^2C™ interfaces varies by device. Refer to the **"Pin Diagrams"** section for availability. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

6: Analog functionality is activated by enabling the USB module and is not controlled by the ANSEL register.

REGISTER 8-3: DMAxSTAH: DMA CHANNEL x START ADDRESS REGISTER A (HIGH)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STA<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **STA<23:16>:** Primary Start Address bits (source or destination)

REGISTER 8-4: DMAxSTAL: DMA CHANNEL x START ADDRESS REGISTER A (LOW)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STA<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STA<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **STA<15:0>:** Primary Start Address bits (source or destination)

REGISTER 8-5: DMAxSTBH: DMA CHANNEL x START ADDRESS REGISTER B (HIGH)

U-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **STB<23:16>:** Secondary Start Address bits (source or destination)

REGISTER 8-6: DMAxSTBL: DMA CHANNEL x START ADDRESS REGISTER B (LOW)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **STB<15:0>:** Secondary Start Address bits (source or destination)

11.4 Peripheral Pin Select

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin-count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code or a complete redesign may be the only option.

Peripheral Pin Select configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to any one of these I/O pins. Peripheral Pin Select is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

11.4.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the designation “RPn” or “RPIn” in their full pin designation, where “RP” designates a remappable function for input or output and “RPI” designates a remappable functions for input only, and “n” is the remappable pin number.

11.4.2 AVAILABLE PERIPHERALS

The peripherals managed by the Peripheral Pin Select are all digital only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs.

In comparison, some digital-only peripheral modules are never included in the Peripheral Pin Select feature. This is because the peripheral’s function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I^2C and the PWM. A similar requirement excludes all modules with analog inputs, such as the ADC Converter.

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

11.4.3 CONTROLLING PERIPHERAL PIN SELECT

Peripheral Pin Select features are controlled through two sets of SFRs: one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral’s input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

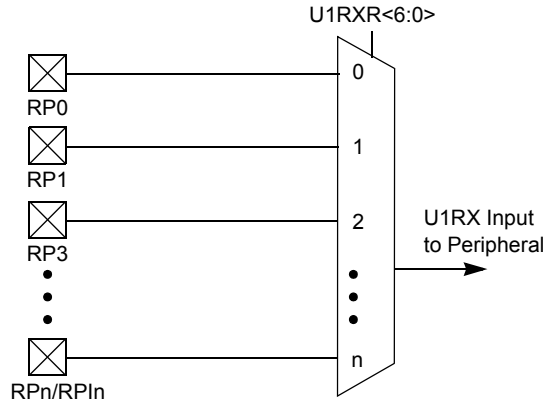
The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

11.4.4 INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see Register 11-1 through Register 11-22). Each register contains sets of 7-bit fields, with each set associated with one of the remappable peripherals (see Table 11-1). Programming a given peripheral’s bit field with an appropriate 7-bit value maps the RPn/RPIn pin with the corresponding value to that peripheral (see Table 11-2). For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

For example, Figure 11-2 illustrates remappable pin selection for the U1RX input.

FIGURE 11-2: U1RX REMAPPABLE INPUT



Note: For input only, Peripheral Pin Select functionality does not have priority over TRISx settings. Therefore, when configuring RPn/RPIn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to ‘1’).

TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES

Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment
000 0000	I	Vss
000 0001	I	C1OUT(1)
000 0010	I	C2OUT(1)
000 0011	I	C3OUT(1)
000 0100	—	Reserved
000 0101	—	Reserved
000 0110	—	Reserved
000 0111	—	Reserved
000 1000	I	FINDX1(1)
000 1001	I	FHOME1(1)
000 1010	I	FINDX2(1)
000 1011	I	FHOME2(1)
000 1100	—	Reserved
000 1101	—	Reserved
000 1110	—	Reserved
000 1111	—	Reserved
001 0000	I	RPI16
001 0001	I	RPI17
001 0010	I	RPI18
001 0011	I	RPI19
001 0100	I	RPI20
001 0101	I	RPI21
001 0110	I	RPI22
001 0111	I	RPI23
001 1000	—	Reserved
001 1001	—	Reserved
001 1010	—	Reserved
001 1011	—	Reserved
001 1100	—	Reserved
001 1101	—	Reserved
001 1110	I	RPI30
001 1111	I	RPI31
010 0000	I	RPI32
010 0001	I	RPI33
010 0010	I	RPI34
010 0011	I	RPI35
010 0100	I	RPI36
010 0101	I	RPI37
010 0110	I	RPI38
010 0111	I	RPI39
010 1000	I	RPI40
010 1001	I	RPI41
010 1010	I	RPI42
010 1101	I	RPI45
010 1110	I	RPI46
010 1111	I	RPI47
011 0000	—	Reserved
011 0001	I	RPI49
011 0010	I	RPI50
011 0011	I	RPI51
011 0100	I	RPI52
011 0101	—	Reserved
011 0110	—	Reserved
011 0111	—	Reserved
011 1000	—	Reserved
011 1001	—	Reserved
011 1010	—	Reserved
011 1011	—	Reserved
011 1100	I	RPI60
011 1101	I	RPI61
011 1110	I	RPI62
011 1111	—	Reserved
100 0000	I/O	RP64
100 0001	I/O	RP65
100 0010	I/O	RP66
100 0011	I/O	RP67
100 0100	I/O	RP68
100 0101	I/O	RP69
100 0110	I/O	RP70
100 0111	I/O	RP71
100 1000	I	RPI72
100 1001	I	RPI73
100 1010	I	RPI74
100 1011	I	RPI75
100 1100	I	RPI76
100 1101	I	RPI77
100 1110	I	RPI78
100 1111	I/O	RP79
101 0000	I/O	RP80
101 0001	I	RPI81
101 0010	I/O	RP82
101 0011	I	RPI83
101 0100	I/O	RP84
101 0101	I/O	RP85
101 0110	I	RPI86
101 0111	I/O	RP87

Note 1: See **Section 11.4.4.2 “Virtual Connections”** for more information on selecting this pin assignment.

REGISTER 11-18: RPINR17: PERIPHERAL PIN SELECT INPUT REGISTER 17 (dsPIC33EPXXXMU806/810/814 DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	HOME2R<6:0>(1)						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	INDX2R<6:0>(1)						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **HOME2R<6:0>:** Assign QEI2 HOME2 (HOME2) to the Corresponding RPn/RPIn Pin bits(1) (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **INDX2R<6:0>:** Assign QEI2 INDEX2 (INDX2) to the Corresponding RPn/RPIn Pin bits(1) (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

Note 1: These bits are available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

REGISTER 11-36: RPINR36: PERIPHERAL PIN SELECT INPUT REGISTER 36

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IC16R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IC15R<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **IC16R<6:0>:** Assign Input Capture 16 (IC16) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **IC15R<6:0>:** Assign Input Capture 15 (IC15) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

REGISTER 11-38: RPINR38: PERIPHERAL PIN SELECT INPUT REGISTER 38

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	DTCMP1R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SYNCI2R<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **DTCMP1R<6:0>:** Assign PWM Dead-Time Compensation Input 1 to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **SYNCI2R<6:0>:** Assign PWM Synchronization Input 2 to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

REGISTER 16-14: PHASEx: PWMx PRIMARY PHASE SHIFT REGISTER(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PHASEx<15:0>:** PWM Phase Shift Value or Independent Time Base Period for the PWM Generator bits

Note 1: If ITB (PWMCONx<9>) = 0, the following applies based on the mode of operation:
- Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCON<11:10>) = 00, 01 or 10), PHASEx<15:0> = Phase shift value for PWMxH and PWMxL outputs.
- True Independent Output mode (PMOD<1:0> (IOCONx<11:10>) = 11), PHASEx<15:0> = Phase shift value for PWMxH only.

2: If ITB (PWMCONx<9>) = 1, the following applies based on the mode of operation:
- Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10), PHASEx<15:0> = Independent time base period value for PWMxH and PWMxL.
- True Independent Output mode (PMOD<1:0> (IOCONx<11:10>) = 11), PHASEx<15:0> = Independent time base period value for PWMxH only.

REGISTER 19-3: I2CxMSK: I2Cx SLAVE MODE ADDRESS MASK REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	AMSK9	AMSK8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
AMSK7	AMSK6	AMSK5	AMSK4	AMSK3	AMSK2	AMSK1	AMSK0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **AMSKx:** Mask for Address bit x Select bit

For 10-Bit Address:

1 = Enables masking for bit Ax of incoming message address; bit match is not required in this position

0 = Disables masking for bit Ax; bit match is required in this position

For 7-Bit Address (I2CxMSK<6:0> only):

1 = Enables masking for bit Ax + 1 of incoming message address; bit match is not required in this position

0 = Disable masking for bit Ax + 1; bit match is required in this position

REGISTER 21-13: CxBUFPNT2: ECANx FILTER 4-7 BUFFER POINTER REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7BP<3:0>				F6BP<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F5BP<3:0>				F4BP<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **F7BP<3:0>:** RX Buffer Mask for Filter 7 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F6BP<3:0>:** RX Buffer Mask for Filter 6 bits (same values as bit 15-12)

bit 7-4 **F5BP<3:0>:** RX Buffer Mask for Filter 5 bits (same values as bit 15-12)

bit 3-0 **F4BP<3:0>:** RX Buffer Mask for Filter 4 bits (same values as bit 15-12)

REGISTER 21-14: CxBUFPNT3: ECANx FILTER 8-11 BUFFER POINTER REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F11BP<3:0>				F10BP<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F9BP<3:0>				F8BP<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **F11BP<3:0>:** RX Buffer Mask for Filter 11 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F10BP<3:0>:** RX Buffer Mask for Filter 10 bits (same values as bit 15-12)

bit 7-4 **F9BP<3:0>:** RX Buffer Mask for Filter 9 bits (same values as bit 15-12)

bit 3-0 **F8BP<3:0>:** RX Buffer Mask for Filter 8 bits (same values as bit 15-12)

REGISTER 21-15: CxBUFPNT4: ECANx FILTER 12-15 BUFFER POINTER REGISTER 4

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F15BP<3:0>				F14BP<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F13BP<3:0>				F12BP<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **F15BP<3:0>:** RX Buffer Mask for Filter 15 bits

1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F14BP<3:0>:** RX Buffer Mask for Filter 14 bits (same values as bit 15-12)

bit 7-4 **F13BP<3:0>:** RX Buffer Mask for Filter 13 bits (same values as bit 15-12)

bit 3-0 **F12BP<3:0>:** RX Buffer Mask for Filter 12 bits (same values as bit 15-12)

REGISTER 21-22: CxRXFUL1: ECANx RECEIVE BUFFER FULL REGISTER 1

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXFUL15	RXFUL14	RXFUL13	RXFUL12	RXFUL11	RXFUL10	RXFUL9	RXFUL8
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXFUL7	RXFUL6	RXFUL5	RXFUL4	RXFUL3	RXFUL2	RXFUL1	RXFUL0
bit 7							bit 0

Legend:	C = Writable bit, but only '0' can be written to clear the bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **RXFUL<15:0>:** Receive Buffer n Full bits

1 = Buffer is full (set by module)

0 = Buffer is empty (cleared by user software)

REGISTER 21-23: CxRXFUL2: ECANx RECEIVE BUFFER FULL REGISTER 2

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXFUL31	RXFUL30	RXFUL29	RXFUL28	RXFUL27	RXFUL26	RXFUL25	RXFUL24
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXFUL23	RXFUL22	RXFUL21	RXFUL20	RXFUL19	RXFUL18	RXFUL17	RXFUL16
bit 7							bit 0

Legend:	C = Writable bit, but only '0' can be written to clear the bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **RXFUL<31:16>:** Receive Buffer n Full bits

1 = Buffer is full (set by module)

0 = Buffer is empty (cleared by user software)

27.3 Programmable CRC Registers

REGISTER 27-1: CRCCON1: CRC CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R-0	R-0	R-0	R-0	R-0
CRCEN	—	CSIDL	VWORD<4:0>				
bit 15							bit 8

R-0	R-1	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CRCEN:** CRC Enable bit
1 = CRC module is enabled
0 = CRC module is disabled, all state machines, pointers and CRCWDAT/CRCDAT are reset; other SFRs are not reset

bit 14 **Unimplemented:** Read as '0'

bit 13 **CSIDL:** CRC Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-8 **VWORD<4:0>:** Pointer Value bits
Indicates the number of valid words in the FIFO. Has a maximum value of 8 when PLEN<4:0> > 7 or 16 when PLEN<4:0> ≤ 7.

bit 7 **CRCFUL:** FIFO Full bit
1 = FIFO is full
0 = FIFO is not full

bit 6 **CRCMPT:** FIFO Empty Bit
1 = FIFO is empty
0 = FIFO is not empty

bit 5 **CRCISEL:** CRC Interrupt Selection bit
1 = Interrupt on FIFO is empty; final word of data is still shifting through CRC
0 = Interrupt on shift is complete and CRCWDAT results are ready

bit 4 **CRCGO:** Start CRC bit
1 = Starts CRC serial shifter
0 = CRC serial shifter is turned off

bit 3 **LENDIAN:** Data Word Little-Endian Configuration bit
1 = Data word is shifted into the CRC starting with the LSb (little endian)
0 = Data word is shifted into the CRC starting with the MSb (big endian)

bit 2-0 **Unimplemented:** Read as '0'

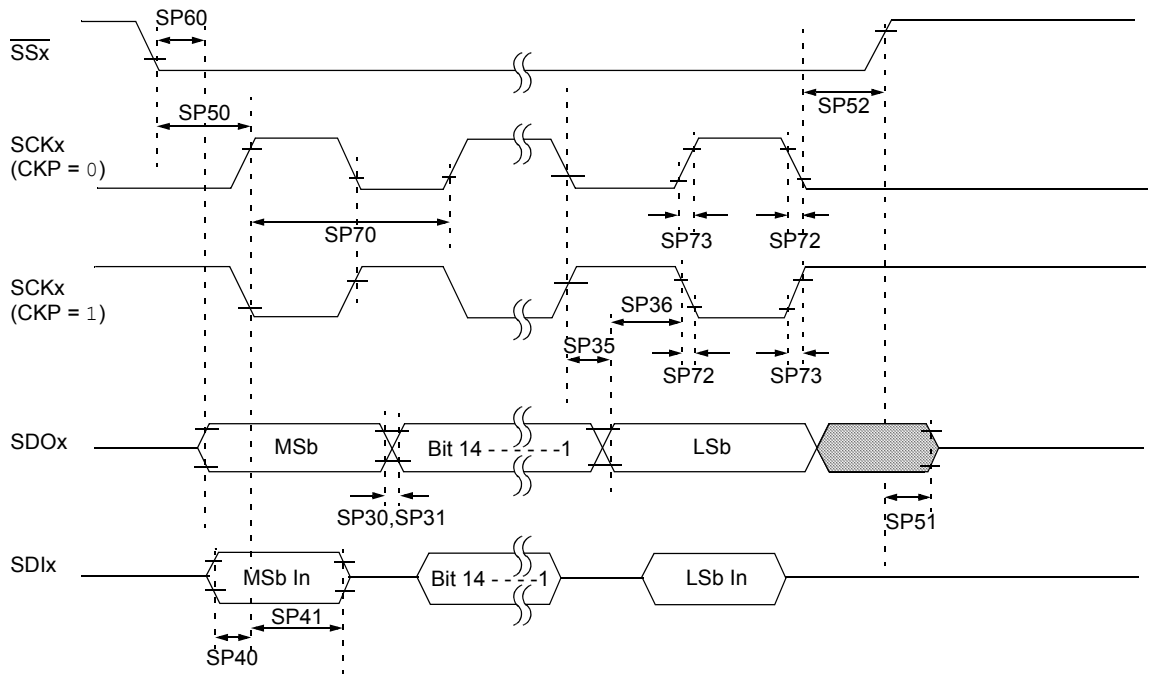
TABLE 29-2: CONFIGURATION BITS DESCRIPTION

Bit Field	Register	RTSP Effect	Description
GSSK<1:0>	FGS	Immediate	General Segment Key bits These bits must be set to '00' if GWRP = 1 and GSS = 1. These bits must be set to '11' for any other value of the GWRP and GSS bits. Any mismatch between either the GWRP or GSS bits, and the GSSK bits (as described above), will result in code protection becoming enabled for the General Segment. A Flash bulk erase will be required to unlock the device.
GSS	FGS	Immediate	General Segment Code-Protect bit 1 = User program memory is not code-protected 0 = User program memory is code-protected
GWRP	FGS	Immediate	General Segment Write-Protect bit 1 = User program memory is not write-protected 0 = User program memory is write-protected
IESO	FOSCSEL	Immediate	Two-Speed Oscillator Start-up Enable bit 1 = Start-up device with FRC, then automatically switch to the user-selected oscillator source when ready 0 = Start-up device with user-selected oscillator source
FNOSC<2:0>	FOSCSEL	If clock switch is enabled, the RTSP effect is on any device Reset; otherwise, immediate	Initial Oscillator Source Selection bits 111 = Internal Fast RC (FRC) Oscillator with Postscaler 110 = Internal Fast RC (FRC) Oscillator with Divide-by-16 101 = LPRC Oscillator 100 = Secondary (LP) Oscillator 011 = Primary (XT, HS, EC) Oscillator with PLL 010 = Primary (XT, HS, EC) Oscillator 001 = Internal Fast RC (FRC) Oscillator with PLL 000 = FRC Oscillator
FCKSM<1:0>	FOSC	Immediate	Clock Switching Mode bits 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
IOL1WAY	FOSC	Immediate	Peripheral Pin Select Configuration bit 1 = Allows only one reconfiguration 0 = Allows multiple reconfigurations
OSCIOFNC	FOSC	Immediate	OSC2 Pin Function bit (except in XT and HS modes) 1 = OSC2 is the clock output 0 = OSC2 is the general purpose digital I/O pin
POSCMD<1:0>	FOSC	Immediate	Primary Oscillator Mode Select bits 11 = Primary Oscillator is disabled 10 = HS Crystal Oscillator mode 01 = XT Crystal Oscillator mode 00 = EC (External Clock) mode
FWDTEN	FWDT	Immediate	Watchdog Timer Enable bit 1 = Watchdog Timer is always enabled (LPRC Oscillator cannot be disabled. Clearing the SWDTEN bit in the RCON register has no effect.) 0 = Watchdog Timer is enabled/disabled by user software (LPRC can be disabled by clearing the SWDTEN bit in the RCON register.)

Note 1: BOR should always be enabled for proper operation (BOREN = 1).

2: This register can only be modified when code protection and write protection are disabled for both the General and Auxiliary Segments (APL = 1, AWRP = 1, APLK = 0, GSS = 1, GWRP = 1 and GSSK = 0).

FIGURE 32-19: SPI1, SPI3 AND SPI4 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 32-1 for load conditions.

FIGURE 33-9: TYPICAL FRC FREQUENCY @ VDD = 3.3V

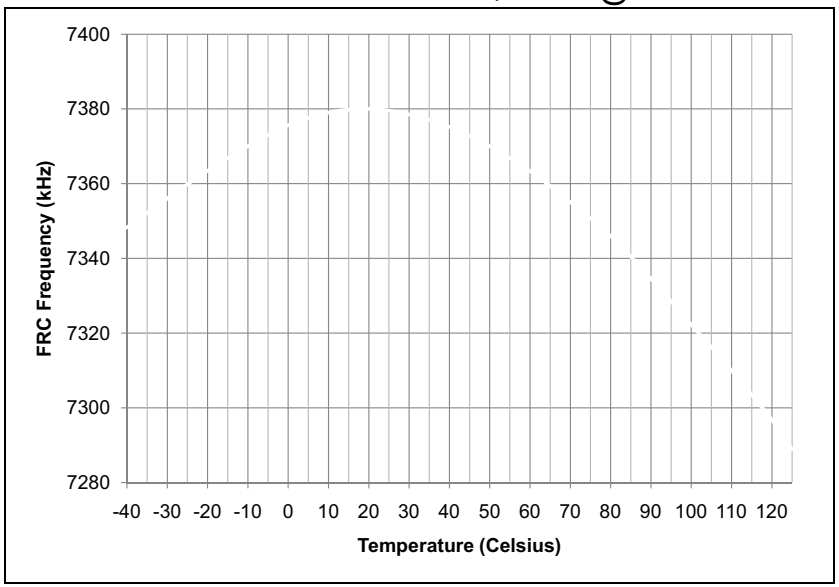


FIGURE 33-10: TYPICAL LPRC FREQUENCY @ VDD = 3.3V