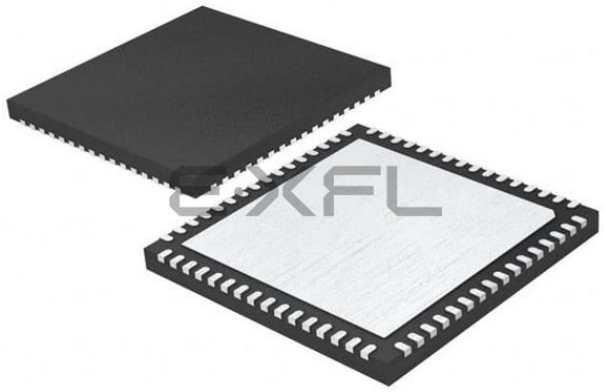
Microchip Technology - DSPIC33EP512MC806T-E/MR Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512mc806t-e-mr

REGISTER 3-2: CORCON: CORE CONTROL REGISTER (CONTINUED)

bit 2 **SFA:** Stack Frame Active Status bit
- 1 = Stack frame is active; W14 and W15 address 0x0000 to 0xFFFF, regardless of DSRPAG and DSWPAG values
- 0 = Stack frame is not active; W14 and W15 address of EDS or Base Data Space

bit 1 **RND:** Rounding Mode Select bit(1)
- 1 = Biased (conventional) rounding is enabled
- 0 = Unbiased (convergent) rounding is enabled

bit 0 **IF:** Integer or Fractional Multiplier Mode Select bit(1)
- 1 = Integer mode is enabled for DSP multiply
- 0 = Fractional mode is enabled for DSP multiply

Note 1: This bit is available on dsPIC33EPXXX(GP/MC/MU)806/810/814 devices only.

2: This bit is always read as '0'.

3: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

NOTES:

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15.2 Output Compare Control Registers

REGISTER 15-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	OCSIDL	OCTSEL<2:0>			ENFLTC	ENFLTB
bit 15							bit 8

R/W-0	R/W-0, HSC	R/W-0, HSC	R/W-0, HSC	R/W-0	R/W-0	R/W-0	R/W-0
ENFLTA	OCFLTC	OCFLTB	OCFLTA	TRIGMODE	OCM<2:0>		
bit 7							bit 0

Legend:	HCS = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **OCSIDL:** Stop Output Compare x in Idle Mode Control bit
1 = Output Compare x Halts in CPU Idle mode
0 = Output Compare x continues to operate in CPU Idle mode

bit 12-10 **OCTSEL<2:0>:** Output Compare x Clock Select bits
111 = Peripheral clock (FP)
110 = Reserved
101 = Reserved
100 = Clock source of T1CLK is the clock source of OCx (only the synchronous clock is supported)
011 = Clock source of T5CLK is the clock source of OCx
010 = Clock source of T4CLK is the clock source of OCx
001 = Clock source of T3CLK is the clock source of OCx
000 = Clock source of T2CLK is the clock source of OCx

bit 9 **ENFLTC:** Fault C Input Enable bit
1 = Output Compare Fault C input (OCFC) is enabled
0 = Output Compare Fault C input (OCFC) is disabled

bit 8 **ENFLTB:** Fault B Input Enable bit
1 = Output Compare Fault B input (OCFB) is enabled
0 = Output Compare Fault B input (OCFB) is disabled

bit 7 **ENFLTA:** Fault A Input Enable bit
1 = Output Compare Fault A input (OCFA) is enabled
0 = Output Compare Fault A input (OCFA) is disabled

bit 6 **OCFLTC:** PWM Fault C Condition Status bit
1 = PWM Fault C condition on OCFC pin has occurred
0 = No PWM Fault C condition on OCFC pin has occurred

bit 5 **OCFLTB:** PWM Fault B Condition Status bit
1 = PWM Fault B condition on OCFB pin has occurred
0 = No PWM Fault B condition on OCFB pin has occurred

bit 4 **OCFLTA:** PWM Fault A Condition Status bit
1 = PWM Fault A condition on OCFA pin has occurred
0 = No PWM Fault A condition on OCFA pin has occurred

bit 3 **TRIGMODE:** Trigger Status Mode Select bit
1 = TRIGSTAT (OCxCON2<6>) is cleared when OCxRS = OCxTMR or in software
0 = TRIGSTAT is cleared only by software

Note 1: OCxR and OCxRS are double-buffered in PWM mode only.

REGISTER 17-4: POSxCNTH: POSITION COUNTER x HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSCNT<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSCNT<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **POSCNT<31:16>:** High Word Used to Form 32-Bit Position Counter Register (POSxCNT) bits

REGISTER 17-5: POSxCNTL: POSITION COUNTER x LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSCNT<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSCNT<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **POSCNT<15:0>:** Low Word Used to Form 32-Bit Position Counter Register (POSxCNT) bits

REGISTER 17-6: POSxHLD: POSITION COUNTER x HOLD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSHLD<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSHLD<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **POSHLD<15:0>:** Hold Register for Reading and Writing POSxCNTH bits

REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER (CONTINUED)

bit 3 **S:** Start bit

1 = Indicates that a Start (or Repeated Start) bit has been detected last
0 = Start bit was not detected last
Hardware is set or clear when a Start, Repeated Start or Stop is detected.

bit 2 **R_W:** Read/Write Information bit (when operating as I^2C slave)

1 = Read – indicates data transfer is output from a slave
0 = Write – indicates data transfer is input to a slave
Hardware is set or clear after reception of an I^2C device address byte.

bit 1 **RBF:** Receive Buffer Full Status bit

1 = Receive is complete, I2CxRCV is full
0 = Receive is not complete, I2CxRCV is empty
Hardware is set when I2CxRCV is written with a received byte. Hardware is clear when software reads I2CxRCV.

bit 0 **TBF:** Transmit Buffer Full Status bit

1 = Transmit is in progress, I2CxTRN is full
0 = Transmit is complete, I2CxTRN is empty
Hardware is set when software writes to I2CxTRN. Hardware is clear at completion of a data transmission.

REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R/W-0	R-0	R-1
UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN(1)	UTXBF	TRMT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/C-0	R-0
URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	C = Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15,13 **UTXISEL<1:0>:** UARTx Transmission Interrupt Mode Selection bits
- 11 = Reserved; do not use
- 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR) and as a result, the transmit buffer becomes empty
- 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
- 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)

bit 14 **UTXINV:** UARTx Transmit Polarity Inversion bit

If IREN = 0:
- 1 = UxTX Idle state is '0'
- 0 = UxTX Idle state is '1'

If IREN = 1:
- 1 = IrDA encoded, UxTX Idle state is '1'
- 0 = IrDA encoded, UxTX Idle state is '0'

bit 12 **Unimplemented:** Read as '0'

bit 11 **UTXBRK:** UARTx Transmit Break bit
- 1 = Sends Sync Break on next transmission – Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
- 0 = Sync Break transmission is disabled or completed

bit 10 **UTXEN:** UARTx Transmit Enable bit(1)
- 1 = Transmit is enabled, UxTX pin is controlled by UARTx
- 0 = Transmit is disabled, any pending transmission is aborted and the buffer is reset; UxTX pin controlled by port

bit 9 **UTXBF:** UARTx Transmit Buffer Full Status bit (read-only)
- 1 = Transmit buffer is full
- 0 = Transmit buffer is not full, at least one more character can be written

bit 8 **TRMT:** Transmit Shift Register Empty bit (read-only)
- 1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
- 0 = Transmit Shift Register is not empty, a transmission is in progress or queued

bit 7-6 **URXISEL<1:0>:** UARTx Receive Interrupt Mode Selection bits
- 11 = Interrupt is set on UxRSR transfer making the receive buffer full (i.e., has 4 data characters)
- 10 = Interrupt is set on UxRSR transfer making the receive buffer 3/4 full (i.e., has 3 data characters)
- 0x = Interrupt is set when any character is received and transferred from the UxRSR to the receive buffer; receive buffer has one or more characters

Note 1: Refer to **Section 17. "UART"** (DS70582) in the *"dsPIC33E/PIC24E Family Reference Manual"* for information on enabling the UARTx module for transmit operation.

REGISTER 21-13: CxBUFPNT2: ECANx FILTER 4-7 BUFFER POINTER REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7BP<3:0>				F6BP<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F5BP<3:0>				F4BP<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **F7BP<3:0>:** RX Buffer Mask for Filter 7 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F6BP<3:0>:** RX Buffer Mask for Filter 6 bits (same values as bit 15-12)

bit 7-4 **F5BP<3:0>:** RX Buffer Mask for Filter 5 bits (same values as bit 15-12)

bit 3-0 **F4BP<3:0>:** RX Buffer Mask for Filter 4 bits (same values as bit 15-12)

REGISTER 21-14: CxBUFPNT3: ECANx FILTER 8-11 BUFFER POINTER REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F11BP<3:0>				F10BP<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F9BP<3:0>				F8BP<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **F11BP<3:0>:** RX Buffer Mask for Filter 11 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F10BP<3:0>:** RX Buffer Mask for Filter 10 bits (same values as bit 15-12)

bit 7-4 **F9BP<3:0>:** RX Buffer Mask for Filter 9 bits (same values as bit 15-12)

bit 3-0 **F8BP<3:0>:** RX Buffer Mask for Filter 8 bits (same values as bit 15-12)

REGISTER 21-24: CxRXOVF1: ECANx RECEIVE BUFFER OVERFLOW REGISTER 1

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0
bit 7							bit 0

Legend:	C = Writable bit, but only ‘0’ can be written to clear the bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **RXOVF<15:0>:** Receive Buffer n Overflow bits
1 = Module attempted to write to a full buffer (set by module)
0 = No overflow condition (cleared by user software)

REGISTER 21-25: CxRXOVF2: ECANx RECEIVE BUFFER OVERFLOW REGISTER 2

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16
bit 7							bit 0

Legend:	C = Writable bit, but only ‘0’ can be written to clear the bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **RXOVF<31:16>:** Receive Buffer n Overflow bits
1 = Module attempted to write to a full buffer (set by module)
0 = No overflow condition (cleared by user software)

REGISTER 22-12: UxOTGIR: USB OTG INTERRUPT STATUS REGISTER (HOST MODE ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/K-0, HS	R/K-0, HS	R/K-0, HS	R/K-0, HS	R/K-0, HS	R/K-0, HS	U-0	R/K-0, HS
IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—	VBUSVDIF
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	K = Write '1' to clear bit	HS = Hardware Settable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **IDIF:** ID State Change Indicator bit
1 = Change in ID state is detected
0 = No ID state change

bit 6 **T1MSECIF:** 1 Millisecond Timer bit
1 = The 1 millisecond timer has expired
0 = The 1 millisecond timer has not expired

bit 5 **LSTATEIF:** Line State Stable Indicator bit
1 = USB line state (as defined by the SE0 and JSTATE bits) has been stable for 1 ms, but different from last time
0 = USB line state has not been stable for 1 ms

bit 4 **ACTVIF:** Bus Activity Indicator bit
1 = Activity on the D+/D- lines or VBUS is detected
0 = No activity on the D+/D- lines or VBUS is detected

bit 3 **SESVDIF:** Session Valid Change Indicator bit
1 = VBUS has crossed VA_SESS_VLD (as defined in the USB OTG Specification)(1)
0 = VBUS has not crossed VA_SESS_VLD

bit 2 **SESENDIF:** B-Device VBUS Change Indicator bit
1 = VBUS change on B-device is detected; VBUS has crossed VB_SESS_END (as defined in the USB OTG Specification)(1)
0 = VBUS has not crossed VA_SESS_END

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIF:** A-Device VBUS Change Indicator bit
1 = VBUS change on A-device is detected; VBUS has crossed VA_VBUS_VLD (as defined in the USB OTG Specification)(1)
0 = No VBUS change on A-device is detected

Note 1: VBUS threshold crossings may be either rising or falling.

REGISTER 22-16: UxIE: USB INTERRUPT ENABLE REGISTER (DEVICE MODE)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STALLIE	—	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE	URSTIE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **STALLIE:** STALL Handshake Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 6 **Unimplemented:** Read as '0'

bit 5 **RESUMEIE:** Resume Interrupt bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 4 **IDLEIE:** Idle Detect Interrupt bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 3 **TRNIE:** Token Processing Complete Interrupt bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 2 **SOFIE:** Start-of-Frame Token Interrupt bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 1 **UERRIE:** USB Error Condition Interrupt bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 0 **URSTIE:** USB Reset Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

REGISTER 25-2: CMxCON: COMPARATOR x CONTROL REGISTER (CONTINUED)

bit 4 **CREF:** Comparator Reference Select bit (VIN+ input)
1 = VIN+ input connects to internal CVREFIN voltage
0 = VIN+ input connects to CxIN1+ pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Comparator Channel Select bits
11 = VIN- input of comparator connects to IVREF
10 = VIN- input of comparator connects to CXIN3- pin
01 = VIN- input of comparator connects to CXIN1- pin
00 = VIN- input of comparator connects to CXIN2- pin

26.1 Writing to the RTCC Timer

Note: To allow the RTCC module to be clocked by the secondary crystal oscillator, the Secondary Oscillator Enable (LPOSCEN) bit in the Oscillator Control (OSCCON<1>) register must be set. For further details, refer to **Section 7. "Oscillator"** (DS70580) in the *"dsPIC33E/PIC24E Family Reference Manual"*.

The user application can configure the time and calendar by writing the desired seconds, minutes, hours, weekday, date, month and year to the RTCC registers. Under normal operation, writes to the RTCC Timer registers are not allowed. Attempted writes will appear to execute normally, but the contents of the registers will remain unchanged. To write to the RTCC register, the RTCWREN bit (RCFGCAL<13>) must be set. Setting the RTCWREN bit allows writes to the RTCC registers. Conversely, clearing the RTCWREN bit prevents writes.

To set the RTCWREN bit, the following procedure must be executed. The RTCWREN bit can be cleared at any time:

1. Write 0x55 to NVMKEY.
2. Write 0xAA to NVMKEY.
3. Set the RTCWREN bit using a single-cycle instruction.

The RTCC module is enabled by setting the RTCEN bit (RCFGCAL<15>). To set or clear the RTCEN bit, the RTCWREN bit (RCFGCAL<13>) must be set.

If the entire clock (hours, minutes and seconds) needs to be corrected, it is recommended that the RTCC module should be disabled to avoid coincidental write operation when the timer increments. Therefore, it stops the clock from counting while writing to the RTCC Timer register.

26.2 RTCC Resources

Many useful resources related to RTCC are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310

26.2.1 KEY RESOURCES

- **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS70584) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

TABLE 29-2: CONFIGURATION BITS DESCRIPTION (CONTINUED)

Bit Field	Register	RTSP Effect	Description
WINDIS	FWDT	Immediate	Watchdog Timer Window Enable bit 1 = Watchdog Timer is in Non-Window mode 0 = Watchdog Timer is in Window mode
PLLKEN	FWDT	Immediate	PLL Lock Wait Enable bit 1 = Clock switches to the PLL source will wait until the PLL lock signal is valid 0 = Clock switch will not wait for PLL lock
WDTPRE	FWDT	Immediate	Watchdog Timer Prescaler bit 1 = 1:128 0 = 1:32
APLK<1:0>	FAS(2)	Immediate	Auxiliary Segment Key bits These bits must be set to '00' if AWRP = 1 and APL = 1. These bits must be set to '11' for any other value of the AWRP and APL bits. Any mismatch between either the AWRP or APL bits and the APLK bits (as described above), will result in code protection becoming enabled for the Auxiliary Segment. A Flash bulk erase will be required to unlock the device.
APL	FAS(2)	Immediate	Auxiliary Segment Code-Protect bit 1 = Auxiliary program memory is not code-protected 0 = Auxiliary program memory is code-protected
AWRP	FAS(2)	Immediate	Auxiliary Segment Write-Protect bit 1 = Auxiliary program memory is not write-protected 0 = Auxiliary program memory is write-protected
WDTPOST<3:0>	FWDT	Immediate	Watchdog Timer Postscaler bits 1111 = 1:32,768 1110 = 1:16,384 • • • 0001 = 1:2 0000 = 1:1
FPWRT<2:0>	FPOR	Immediate	Power-on Reset Timer Value Select bits 111 = PWRT = 128 ms 110 = PWRT = 64 ms 101 = PWRT = 32 ms 100 = PWRT = 16 ms 011 = PWRT = 8 ms 010 = PWRT = 4 ms 001 = PWRT = 2 ms 000 = PWRT = Disabled
BOREN(1)	FPOR	Immediate	Brown-out Reset (BOR) Detection Enable bit 1 = BOR is enabled 0 = BOR is disabled
ALTI2C2	FPOR	Immediate	Alternate I^2C™ pins for I2C2 bit 1 = I2C2 is mapped to the SDA2/SCL2 pins 0 = I2C2 is mapped to the ASDA2/ASCL2 pins
ALTI2C1	FPOR	Immediate	Alternate I^2C pins for I2C1 bit 1 = I2C1 is mapped to the SDA1/SCL1 pins 0 = I2C1 is mapped to the ASDA1/ASCL1 pins

Note 1: BOR should always be enabled for proper operation (BOREN = 1).

2: This register can only be modified when code protection and write protection are disabled for both the General and Auxiliary Segments (APL = 1, AWRP = 1, APLK = 0, GSS = 1, GWRP = 1 and GSSK = 0).

TABLE 32-8: DC CHARACTERISTICS: DOZE CURRENT (I_{DOZE})(1)

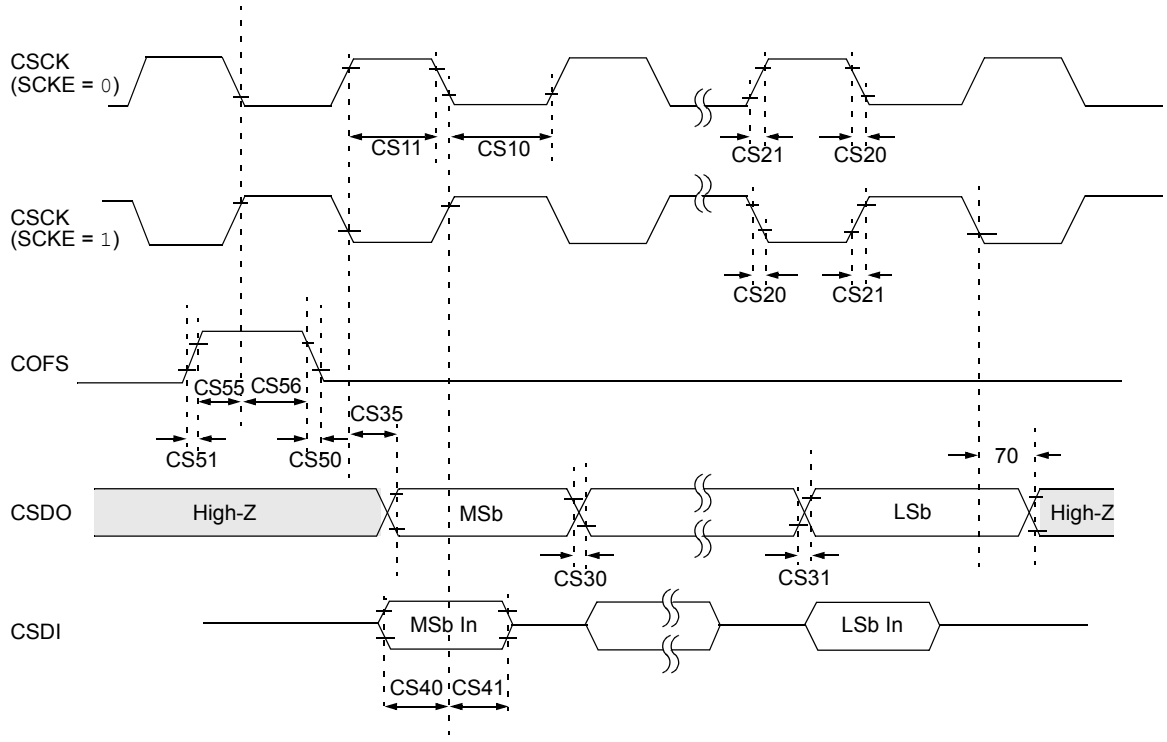
DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Parameter	**Typ.(2)**	**Max.**	**Doze Ratio**	**Units**	**Conditions**		
DC73a	57	86	1:2	mA	-40°C	3.3V	70 MIPS
DC73g	40	60	1:128	mA			
DC70a	58	87	1:2	mA	+25°C	3.3V	70 MIPS
DC70g	41	62	1:128	mA			
DC71a	58	87	1:2	mA	+85°C	3.3V	70 MIPS
DC71g	42	63	1:128	mA			
DC72a	53	80	1:2	mA	+125°C	3.3V	60 MIPS
DC72g	38	57	1:128	mA			

Note 1: I_{DOZE} is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all I_{DOZE} measurements are as follows:

- Oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail with Overshoot/Undershoot < 250 mV
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to V_{SS}
- $\overline{MCLR}$ = V_{DD}, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (defined PMDx bits are set to zero and unimplemented PMDx bits are set to one)
- CPU executing `while(1)` statement
- JTAG is disabled

2: Data in the “Typ” column is at 3.3V, +25ºC unless otherwise stated.

FIGURE 32-40: DCI MODULE (MULTI-CHANNEL, I²S MODES) TIMING CHARACTERISTICS



Note: Refer to Figure 32-1 for load conditions.

FIGURE 32-44: PARALLEL MASTER PORT WRITE TIMING DIAGRAM

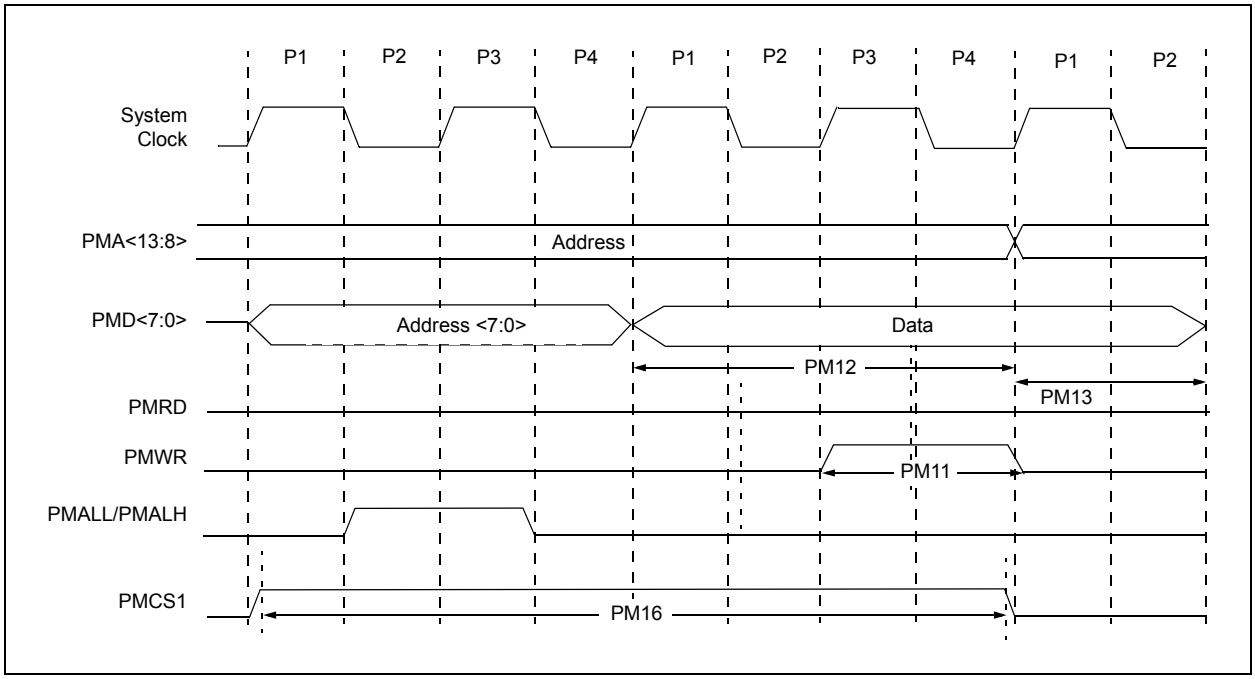


TABLE 32-67: PARALLEL MASTER PORT WRITE TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Characteristic(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
PM11	PMWR Pulse Width	—	0.5 TCY	—	ns	
PM12	Data Out Valid Before PMWR or PMENB goes Inactive (data setup time)	—	1 TCY	—	ns	
PM13	PMWR or PMEMB Invalid to Data Out Invalid (data hold time)	—	0.5 TCY	—	ns	
PM16	PMCSx Pulse Width	TCY - 5	—	—	ns	ADRMUX<1:0> = 00 (demultiplexed address)

Note 1: These parameters are characterized, but not tested in manufacturing.

TABLE 32-68: DMA MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Characteristic(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
DM1	DMA Byte/Word Transfer Latency	1 TCY	—	—	ns	

Note 1: These parameters are characterized, but not tested in manufacturing.

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