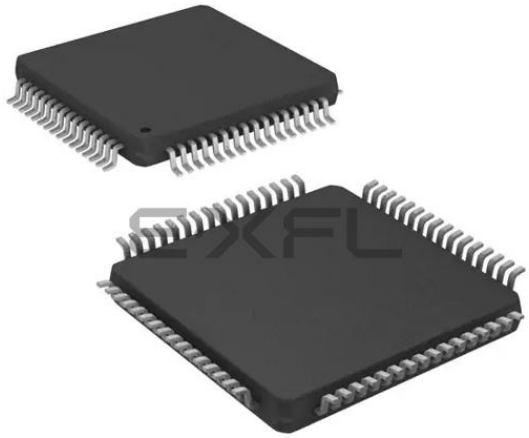

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Details	
Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512mc806t-e-pt

TABLE 2: PIN NAMES: dsPIC33EP256MU810 AND dsPIC33EP512MU810 DEVICES(1,2)

Pin Number	Full Pin Name
A1	AN28/PWM3L/PMD4/RP84/RE4
A2	AN27/PWM2H/PMD3/RPI83/RE3
A3	RP125/RG13
A4	AN24/PWM1L/PMD0/RP80/RE0
A5	RP112/RG0
A6	VCMPST2/RP97/RF1
A7	VDD
A8	No Connect
A9	RPI76/RD12
A10	DPH/RP66/RD2
A11	VCPCON/RP65/RD1
B1	No Connect
B2	RP127/RG15
B3	AN26/PWM2L/PMD2/RP82/RE2
B4	AN25/PWM1H/PMD1/RPI81/RE1
B5	AN23/RPI23/RA7
B6	VCMPST1/RP96/RF0
B7	VCAP
B8	PMRD/RP69/RD5
B9	PMBE/RP67/RD3
B10	VSS
B11	PGEC2/SOSCO/C3IN1-/T1CK/RPI62/RC14
C1	AN30/PWM4L/PMD6/RPI86/RE6
C2	VDD
C3	RPI124/RG12
C4	RP126/RG14
C5	AN22/RPI22/RA6
C6	No Connect
C7	C3IN1+/VCMPST3/RP71/RD7
C8	PMWR/RP68/RD4
C9	No Connect
C10	PGED2/SOSCI/C3IN3-/RPI61/RC13
C11	PMCS1/RPI75/RD11
D1	AN16/PWM5L/RPI49/RC1
D2	AN31/PWM4H/PMD7/RP87/RE7
D3	AN29/PWM3H/PMD5/RP85/RE5
D4	No Connect
D5	No Connect
D6	No Connect
D7	C3IN2-/RP70/RD6
D8	RPI77/RD13
D9	INT0/DMH/RP64/RD0
D10	No Connect
D11	ASCL1(3)/PMCS2/RPI74/RD10

Pin Number	Full Pin Name
E8	RPI31/RA15
E9	RTCC/DMLN/RPI72/RD8
E10	ASDA1(3)/DPLN/RPI73/RD9
E11	RPI30/RA14
F1	$\overline{\text{MCLR}}$
F2	C2IN3-/SDO2/PMA3/RP120/RG8
F3	C2IN1-/PMA2/RPI121/RG9
F4	C1IN1-/SDI2/PMA4/RPI119/RG7
F5	VSS
F6	No Connect
F7	No Connect
F8	VDD
F9	OSC1/RPI60/RC12
F10	VSS
F11	OSC2/CLKO/RC15
G1	AN20/RPI88/RE8
G2	AN21/RPI89/RE9
G3	TMS/RPI16/RA0
G4	No Connect
G5	VDD
G6	VSS
G7	VSS
G8	No Connect
G9	TDO/RPI21/RA5
G10	ASDA2(3)/RPI19/RA3
G11	TDI/RPI20/RA4
H1	AN5/C1IN1+/VBUSON/VBUSST/RPI37/RB5
H2	AN4/C1IN2-/USBOEN/RPI36/RB4
H3	No Connect
H4	No Connect
H5	No Connect
H6	VDD
H7	No Connect
H8	VBUS
H9	VUSB3V3
H10	D+/RG2(4)
H11	ASCL2(3)/RPI18/RA2
J1	AN3/C2IN1+/VPIO/RPI35/RB3
J2	AN2/C2IN2-/VMIO/RPI34/RB2
J3	PGED1/AN7/RCV/RPI39/RB7
J4	AVDD
J5	AN11/PMA12/RPI43/RB11
J6	TCK/RPI17/RA1
J7	AN12/PMA11/RPI44/RB12

Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The availability of I^2C™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

4: The pin name is SCL1/RG2 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.

5: The pin name is SDA1/RG3 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.

TABLE 4-1: CPU CORE REGISTER MAP FOR dsPIC33EPXXX(GP/MC/MU)806/810/814 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
W0	0000	W0 (WREG)																0000
W1	0002	W1																0000
W2	0004	W2																0000
W3	0006	W3																0000
W4	0008	W4																0000
W5	000A	W5																0000
W6	000C	W6																0000
W7	000E	W7																0000
W8	0010	W8																0000
W9	0012	W9																0000
W10	0014	W10																0000
W11	0016	W11																0000
W12	0018	W12																0000
W13	001A	W13																0000
W14	001C	W14																0000
W15	001E	W15																1000
SPLIM	0020	SPLIM																0000
ACCAL	0022	ACCAL																0000
ACCAH	0024	ACCAH																0000
ACCAU	0026	Sign-Extension of ACCA<39>								ACCAU								0000
ACCBL	0028	ACCBL																0000
ACCBH	002A	ACCBH																0000
ACCBU	002C	Sign-Extension of ACCB<39>								ACCBU								0000
PCL	002E	PCL															—	0000
PCH	0030	—	—	—	—	—	—	—	—	—	PCH							0000
DSRPAG	0032	—	—	—	—	—	—	DSRPAG										0001
DSWPAG	0034	—	—	—	—	—	—	—	DSWPAG									0001
RCOUNT	0036	RCOUNT																0000
DCOUNT	0038	DCOUNT																0000
DOSTARTL	003A	DOSTARTL															—	0000
DOSTARTH	003C	—	—	—	—	—	—	—	—	—	—	DOSTARTH						0000
DOENDL	003E	DOENDL															—	0000
DOENDH	0040	—	—	—	—	—	—	—	—	—	—	DOENDH						0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-33: ECAN2 REGISTER MAP WHEN WIN (C2CTRL<0>) = 1

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
—	0500-051E	See Table 4-31																—
C2BUFPNT1	0520	F3BP<3:0>				F2BP<3:0>				F1BP<3:0>				F0BP<3:0>				0000
C2BUFPNT2	0522	F7BP<3:0>				F6BP<3:0>				F5BP<3:0>				F4BP<3:0>				0000
C2BUFPNT3	0524	F11BP<3:0>				F10BP<3:0>				F9BP<3:0>				F8BP<3:0>				0000
C2BUFPNT4	0526	F15BP<3:0>				F14BP<3:0>				F13BP<3:0>				F12BP<3:0>				0000
C2RXM0SID	0530	SID<10:3>								SID<2:0>			—	MIDE	—	EID<17:16>		xxxx
C2RXM0EID	0532	EID<15:8>								EID<7:0>								xxxx
C2RXM1SID	0534	SID<10:3>								SID<2:0>			—	MIDE	—	EID<17:16>		xxxx
C2RXM1EID	0536	EID<15:8>								EID<7:0>								xxxx
C2RXM2SID	0538	SID<10:3>								SID<2:0>			—	MIDE	—	EID<17:16>		xxxx
C2RXM2EID	053A	EID<15:8>								EID<7:0>								xxxx
C2RXF0SID	0540	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C2RXF0EID	0542	EID<15:8>								EID<7:0>								xxxx
C2RXF1SID	0544	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C2RXF1EID	0546	EID<15:8>								EID<7:0>								xxxx
C2RXF2SID	0548	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C2RXF2EID	054A	EID<15:8>								EID<7:0>								xxxx
C2RXF3SID	054C	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C2RXF3EID	054E	EID<15:8>								EID<7:0>								xxxx
C2RXF4SID	0550	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C2RXF4EID	0552	EID<15:8>								EID<7:0>								xxxx
C2RXF5SID	0554	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C2RXF5EID	0556	EID<15:8>								EID<7:0>								xxxx
C2RXF6SID	0558	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C2RXF6EID	055A	EID<15:8>								EID<7:0>								xxxx
C2RXF7SID	055C	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C2RXF7EID	055E	EID<15:8>								EID<7:0>								xxxx
C2RXF8SID	0560	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C2RXF8EID	0562	EID<15:8>								EID<7:0>								xxxx
C2RXF9SID	0564	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C2RXF9EID	0566	EID<15:8>								EID<7:0>								xxxx
C2RXF10SID	0568	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C2RXF10EID	056A	EID<15:8>								EID<7:0>								xxxx
C2RXF11SID	056C	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-49: PMD REGISTER MAP FOR dsPIC33EPXXXMU806 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	QEI1MD	PWMMD	DCIMD	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	C2MD	C1MD	AD1MD	0000
PMD2	0762	IC8MD	IC7MD	IC6MD	IC5MD	IC4MD	IC3MD	IC2MD	IC1MD	OC8MD	OC7MD	OC6MD	OC5MD	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	T9MD	T8MD	T7MD	T6MD	—	CMPMD	RTCCMD	PMPMD	CRCMD	—	QEI2MD	—	U3MD	—	I2C2MD	AD2MD	0000
PMD4	0766	—	—	—	—	—	—	—	—	—	—	U4MD	—	REFOMD	—	—	USB1MD	0000
PMD5	0768	IC16MD	IC15MD	IC14MD	IC13MD	IC12MD	IC11MD	IC10MD	IC9MD	OC16MD	OC15MD	OC14MD	OC13MD	OC12MD	OC11MD	OC10MD	OC9MD	0000
PMD6	076A	—	—	—	—	PWM4MD	PWM3MD	PWM2MD	PWM1MD	—	—	—	—	—	—	SPI4MD	SPI3MD	0000
PMD7	076C	—	—	—	—	—	—	—	—	DMA12MD	DMA8MD	DMA4MD	DMA0MD	—	—	—	—	0000
		—	—	—	—	—	—	—	—	DMA13MD	DMA9MD	DMA5MD	DMA1MD	—	—	—	—	0000
		—	—	—	—	—	—	—	—	DMA14MD	DMA10MD	DMA6MD	DMA2MD	—	—	—	—	0000
		—	—	—	—	—	—	—	—	—	DMA11MD	DMA7MD	DMA3MD	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-50: PMD REGISTER MAP FOR dsPIC33EPXXXMC806 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	QEI1MD	PWMMD	DCIMD	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	C2MD	C1MD	AD1MD	0000
PMD2	0762	IC8MD	IC7MD	IC6MD	IC5MD	IC4MD	IC3MD	IC2MD	IC1MD	OC8MD	OC7MD	OC6MD	OC5MD	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	T9MD	T8MD	T7MD	T6MD	—	CMPMD	RTCCMD	PMPMD	CRCMD	—	QEI2MD	—	U3MD	—	I2C2MD	AD2MD	0000
PMD4	0766	—	—	—	—	—	—	—	—	—	—	U4MD	—	REFOMD	—	—	—	0000
PMD5	0768	IC16MD	IC15MD	IC14MD	IC13MD	IC12MD	IC11MD	IC10MD	IC9MD	OC16MD	OC15MD	OC14MD	OC13MD	OC12MD	OC11MD	OC10MD	OC9MD	0000
PMD6	076A	—	—	—	—	PWM4MD	PWM3MD	PWM2MD	PWM1MD	—	—	—	—	—	—	SPI4MD	SPI3MD	0000
PMD7	076C	—	—	—	—	—	—	—	—	DMA12MD	DMA8MD	DMA4MD	DMA0MD	—	—	—	—	0000
		—	—	—	—	—	—	—	—	DMA13MD	DMA9MD	DMA5MD	DMA1MD	—	—	—	—	0000
		—	—	—	—	—	—	—	—	DMA14MD	DMA10MD	DMA6MD	DMA2MD	—	—	—	—	0000
		—	—	—	—	—	—	—	—	—	DMA11MD	DMA7MD	DMA3MD	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-58: PORTC REGISTER MAP FOR dsPIC33EPXXX(GP/MC/MU)806 AND PIC24EPXXXGP806 DEVICES ONLY

File Name	Addr,	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E20	TRISC15	TRISC14	TRISC13	TRISC12	—	—	—	—	—	—	—	—	—	—	—	—	F000
PORTC	0E22	RC15	RC14	RC13	RC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
LATC	0E24	LATC15	LATC14	LATC13	LATC12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
ODCC	0E26	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
CNENC	0E28	CNIEC15	CNIEC14	CNIEC13	CNIEC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
CNPUC	0E2A	CNPUC15	CNPUC14	CNPUC13	CNPUC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
CNPDC	0E2C	CNPDC15	CNPDC14	CNPDC13	CNPDC12	—	—	—	—	—	—	—	—	—	—	—	—	0000
ANSELC	0E2E	—	ANSC14	ANSC13	—	—	—	—	—	—	—	—	—	—	—	—	—	6000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-59: PORTD REGISTER MAP FOR dsPIC33EPXXXMU810/814 AND PIC24EPXXXGU810/814 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISD	0E30	TRISD15	TRISD14	TRISD13	TRISD12	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	FFFF
PORTD	0E32	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
LATD	0E34	LATD15	LATD14	LATD13	LATD12	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
ODCD	0E36	ODCD15	ODCD14	ODCD13	ODCD12	ODCD11	ODCD10	ODCD9	ODCD8	—	—	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000
CNEND	0E38	CNIED15	CNIED14	CNIED13	CNIED12	CNIED11	CNIED10	CNIED9	CNIED8	CNIED7	CNIED6	CNIED5	CNIED4	CNIED3	CNIED2	CNIED1	CNIED0	0000
CNPUD	0E3A	CNPUD15	CNPUD14	CNPUD13	CNPUD12	CNPUD11	CNPUD10	CNPUD9	CNPUD8	CNPUD7	CNPUD6	CNPUD5	CNPUD4	CNPUD3	CNPUD2	CNPUD1	CNPUD0	0000
CNPDD	0E3C	CNPDD15	CNPDD14	CNPDD13	CNPDD12	CNPDD11	CNPDD10	CNPDD9	CNPDD8	CNPDD7	CNPDD6	CNPDD5	CNPDD4	CNPDD3	CNPDD2	CNPDD1	CNPDD0	0000
ANSELD	0E3E	—	—	—	—	—	—	—	—	ANSD7	ANSD6	—	—	—	—	—	—	00C0

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-60: PORTD REGISTER MAP FOR dsPIC33EPXXX(GP/MC/MU)806 AND PIC24EPXXXGP806 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISD	0E30	—	—	—	—	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	0FFF
PORTD	0E32	—	—	—	—	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
LATD	0E34	—	—	—	—	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
ODCD	0E36	—	—	—	—	ODCD11	ODCD10	ODCD9	ODCD8	—	—	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000
CNEND	0E38	—	—	—	—	CNIED11	CNIED10	CNIED9	CNIED8	CNIED7	CNIED6	CNIED5	CNIED4	CNIED3	CNIED2	CNIED1	CNIED0	0000
CNPUD	0E3A	—	—	—	—	CNPUD11	CNPUD10	CNPUD9	CNPUD8	CNPUD7	CNPUD6	CNPUD5	CNPUD4	CNPUD3	CNPUD2	CNPUD1	CNPUD0	0000
CNPDD	0E3C	—	—	—	—	CNPDD11	CNPDD10	CNPDD9	CNPDD8	CNPDD7	CNPDD6	CNPDD5	CNPDD4	CNPDD3	CNPDD2	CNPDD1	CNPDD0	0000
ANSELD	0E3E	—	—	—	—	—	—	—	—	ANSD7	ANSD6	—	—	—	—	—	—	00C0

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

7.0 INTERRUPT CONTROLLER

Note 1: This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 6. "Interrupts"** (DS70600) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 CPU.

The interrupt controller has the following features:

- Up to eight processor exceptions and software traps
- Eight user-selectable priority levels
- Interrupt Vector Table (IVT) with a unique vector for each interrupt or exception source
- Fixed priority within a specified user priority level
- Fixed interrupt entry and return latencies

7.1 Interrupt Vector Table

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 Interrupt Vector Table (IVT), shown in Figure 7-1, resides in the General Segment of program memory, starting at location, 0x000004, and is used when executing code from the General Segment. The IVT contains seven non-maskable trap vectors and up to 114 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with vector 0 takes priority over interrupts at any other vector address.

Note: Any unimplemented or unused vector locations in the IVT should be programmed with the address of a default interrupt handler routine that contains a `RESET` instruction.

7.2 Auxiliary Interrupt Vector

When code is being executed in the Auxiliary Segment, a special single interrupt vector, located at address, 0x7FFFFA, is used for all interrupt sources and traps. Once vectored to this single routine, the VECNUM<7:0> bits (INTTREG<7:0>, Register 7-7) can be examined to determine the source of the interrupt or trap so that it can be properly processed.

7.3 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices clear their registers in response to a Reset, which forces the PC to zero. The digital signal controller then begins program execution at location, 0x000000. A `GOTO` instruction at the Reset address can redirect program execution to the appropriate start-up routine.

Note: Reset locations are also located in the Auxiliary Segment at the addresses 0x7FFFFC and 0x7FFFFE. The Reset Target Vector Select bit, RSTPRI (FICD<2>) controls whether the primary (General Segment) or Auxiliary Segment Reset location is used.

11.4.4.1 Output Mapping

In contrast to inputs, the outputs of the Peripheral Pin Select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Like the RPINRx registers, each register contains sets of 6 bit fields, with each set associated with one RPn pin (see Register 11-44 through Register 11-51). The value of the bit field corresponds to one of the peripherals and that peripheral's output is mapped to the pin (see Table 11-3 and Figure 11-3).

A null output is associated with the Output Register Reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

FIGURE 11-3: MULTIPLEXING OF REMAPPABLE OUTPUT FOR RPn

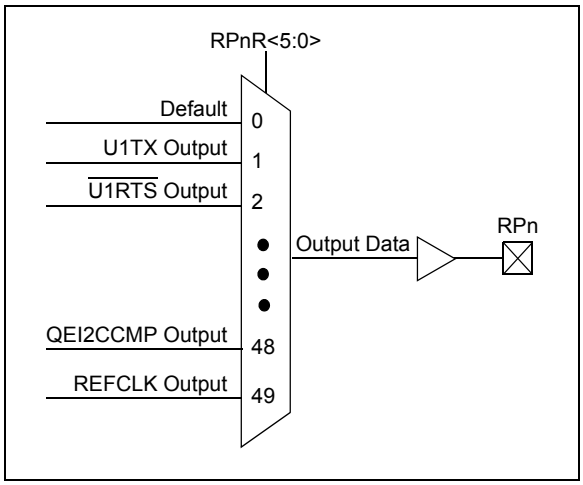


TABLE 11-3: OUTPUT SELECTION FOR REMAPPABLE PINS (RPn)

Function	RPnR<5:0>	Output Name
DEFAULT PORT	000000	RPn tied to Default Pin
U1TX	000001	RPn tied to UART1 Transmit
U1RTS	000010	RPn tied to UART1 Ready-to-Send
U2TX	000011	RPn tied to UART2 Transmit
U2RTS	000100	RPn tied to UART2 Ready-to-Send
SDO1	000101	RPn tied to SPI1 Data Output
SCK1	000110	RPn tied to SPI1 Clock Output
SS1	000111	RPn tied to SPI1 Slave Select
SS2	001010	RPn tied to SPI2 Slave Select
CSDO	001011	RPn tied to DCI Data Output
CSCK	001100	RPn tied to DCI Clock Output
COFS	001101	RPn tied to DCI FSYNC Output
C1TX	001110	RPn tied to CAN1 Transmit
C2TX	001111	RPn tied to CAN2 Transmit
OC1	010000	RPn tied to Output Compare 1 Output
OC2	010001	RPn tied to Output Compare 2 Output
OC3	010010	RPn tied to Output Compare 3 Output
OC4	010011	RPn tied to Output Compare 4 Output
OC5	010100	RPn tied to Output Compare 5 Output
OC6	010101	RPn tied to Output Compare 6 Output
OC7	010110	RPn tied to Output Compare 7 Output
OC8	010111	RPn tied to Output Compare 8 Output
C1OUT	011000	RPn tied to Comparator Output 1
C2OUT	011001	RPn tied to Comparator Output 2
C3OUT	011010	RPn tied to Comparator Output 3
U3TX	011011	RPn tied to UART3 Transmit
U3RTS	011100	RPn tied to UART3 Ready-to-Send

Note 1: This function is available in dsPIC33EPXXX(MC/MU)806/810/814 devices only.

REGISTER 11-57: RPOR13: PERIPHERAL PIN SELECT OUTPUT REGISTER 13

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP118R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP113R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP118R<5:0>:** Peripheral Output Function is Assigned to RP118 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP113R<5:0>:** Peripheral Output Function is Assigned to RP113 Output Pin bits (see Table 11-3 for peripheral function numbers)

REGISTER 11-58: RPOR14: PERIPHERAL PIN SELECT OUTPUT REGISTER 14

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP125R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP120R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP125R<5:0>:** Peripheral Output Function is Assigned to RP125 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP120R<5:0>:** Peripheral Output Function is Assigned to RP120 Output Pin bits (see Table 11-3 for peripheral function numbers)

REGISTER 16-19: IOCONx: PWMx I/O CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PENH	PENL	POLH	POLL	PMOD<1:0>(1)		OVRENH	OVRENL
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PENH:** PWMxH Output Pin Ownership bit
1 = PWM module controls PWMxH pin
0 = GPIO module controls PWMxH pin

bit 14 **PENL:** PWMxL Output Pin Ownership bit
1 = PWM module controls PWMxL pin
0 = GPIO module controls PWMxL pin

bit 13 **POLH:** PWMxH Output Pin Polarity bit
1 = PWMxH pin is active-low
0 = PWMxH pin is active-high

bit 12 **POLL:** PWMxL Output Pin Polarity bit
1 = PWMxL pin is active-low
0 = PWMxL pin is active-high

bit 11-10 **PMOD<1:0>:** PWM # I/O Pin Mode bits(1)
11 = PWM I/O pin pair is in the True Independent Output mode
10 = PWM I/O pin pair is in the Push-Pull Output mode
01 = PWM I/O pin pair is in the Redundant Output mode
00 = PWM I/O pin pair is in the Complementary Output mode

bit 9 **OVRENH:** Override Enable for PWMxH Pin bit
1 = OVRDAT<1> controls output on PWMxH pin
0 = PWM generator controls PWMxH pin

bit 8 **OVRENL:** Override Enable for PWMxL Pin bit
1 = OVRDAT<0> controls output on PWMxL pin
0 = PWM generator controls PWMxL pin

bit 7-6 **OVRDAT<1:0>:** Data for PWMxH, PWMxL Pins if Override is Enabled bits
If OVERENH = 1, PWMxH is driven to the state specified by OVRDAT<1>.
If OVERENL = 1, PWMxL is driven to the state specified by OVRDAT<0>.

bit 5-4 **FLTDAT<1:0>:** Data for PWMxH and PWMxL Pins if FLTMOD is Enabled bits
IFLTMOD (FCLCONx<15>) = 0: Normal Fault mode:
If Fault is active, PWMxH is driven to the state specified by FLTDAT<1>.
If Fault is active, PWMxL is driven to the state specified by FLTDAT<0>.

IFLTMOD (FCLCONx<15>) = 1: Independent Fault mode:
If current limit is active, PWMxH is driven to the state specified by FLTDAT<1>.
If Fault is active, PWMxL is driven to the state specified by FLTDAT<0>.

Note 1: These bits should not be changed after the PWM module is enabled (PTEN = 1).

REGISTER 16-24: AUXCONx: PWM AUXILIARY CONTROL REGISTER x

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	BLANKSEL<3:0>			
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **BLANKSEL<3:0>:** PWM State Blank Source Select bits

The selected state blank signal will block the current-limit and/or Fault input signals (if enabled via the BCH and BCL bits in the LEBCONx register).

1001 = Reserved
1000 = Reserved
0111 = PWM7H selected as state blank source
0110 = PWM6H selected as state blank source
0101 = PWM5H selected as state blank source
0100 = PWM4H selected as state blank source
0011 = PWM3H selected as state blank source
0010 = PWM2H selected as state blank source
0001 = PWM1H selected as state blank source
0000 = No state blanking

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 **CHOPSEL<3:0>:** PWM Chop Clock Source Select bits

The selected signal will enable and disable (CHOP) the selected PWM outputs.

1001 = Reserved
1000 = Reserved
0111 = PWM7H selected as CHOP clock source
0110 = PWM6H selected as CHOP clock source
0101 = PWM5H selected as CHOP clock source
0100 = PWM4H selected as CHOP clock source
0011 = PWM3H selected as CHOP clock source
0010 = PWM2H selected as CHOP clock source
0001 = PWM1H selected as CHOP clock source
0000 = Chop clock generator selected as CHOP clock source

bit 1 **CHOPHEN:** PWMxH Output Chopping Enable bit

1 = PWMxH chopping function is enabled
0 = PWMxH chopping function is disabled

bit 0 **CHOPLEN:** PWMxL Output Chopping Enable bit

1 = PWMxL chopping function is enabled
0 = PWMxL chopping function is disabled

REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER

R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC
ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10
bit 15							bit 8

R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF
bit 7							bit 0

Legend:	C = Clearable bit	U = Unimplemented bit, read as '0'	
R = Readable bit	W = Writable bit	HS = Hardware Settable bit	HSC = Hardware Settable/Clearable bit
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ACKSTAT:** Acknowledge Status bit
(when operating as I^2C™ master, applicable to master transmit operation)
1 = NACK received from slave
0 = ACK received from slave
Hardware is set or clear at the end of a slave Acknowledge.

bit 14 **TRSTAT:** Transmit Status bit (when operating as I^2C master, applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress
Hardware is set at the beginning of a master transmission. Hardware is clear at the end of a slave Acknowledge.

bit 13-11 **Unimplemented:** Read as '0'

bit 10 **BCL:** Master Bus Collision Detect bit
1 = A bus collision has been detected during a master operation
0 = No collision
Hardware is set at detection of a bus collision.

bit 9 **GCSTAT:** General Call Status bit
1 = General call address was received
0 = General call address was not received
Hardware is set when an address matches the general call address. Hardware is clear at a Stop detection.

bit 8 **ADD10:** 10-Bit Address Status bit
1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware is set at a match of the 2nd byte of a matched 10-bit address. Hardware is clear at a Stop detection.

bit 7 **IWCOL:** Write Collision Detect bit
1 = An attempt to write to the I2CxTRN register failed because the I^2C module is busy
0 = No collision
Hardware is set at an occurrence of a write to I2CxTRN while busy (cleared by software).

bit 6 **I2COV:** I2Cx Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register is still holding the previous byte
0 = No overflow
Hardware is set at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

bit 5 **D_A:** Data/Address bit (when operating as I^2C slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was a device address
Hardware is clear at a device address match. Hardware is set by reception of a slave byte.

bit 4 **P:** Stop bit
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last
Hardware is set or clear when a Start, Repeated Start or Stop is detected.

20.1 UARTx Helpful Tips

1. In multi-node direct-connect UARTx networks, UARTx receive inputs react to the complementary logic level defined by the URXINV bit (UxMODE<4>), which defines the Idle state, the default of which is logic high (i.e., URXINV = 0). Because remote devices do not initialize at the same time, it is likely that one of the devices, because the RX line is floating, will trigger a Start bit detection and will cause the first byte received, after the device has been initialized, to be invalid. To avoid this situation, the user should use a pull-up or pull-down resistor on the RX pin depending on the value of the URXINV bit.
   a) If URXINV = 0, use a pull-up resistor on the RX pin.
   b) If URXINV = 1, use a pull-down resistor on the RX pin.
2. The first character received on a wake-up from Sleep mode, caused by activity on the UxRX pin of the UARTx module, will be invalid. In Sleep mode, peripheral clocks are disabled. By the time the oscillator system has restarted and stabilized from Sleep mode, the baud rate bit sampling clock, relative to the incoming UxRX bit timing, is no longer synchronized resulting in the first character being invalid. This is to be expected.

20.2 UARTx Resources

Many useful resources related to the UARTx are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310

20.2.1 KEY RESOURCES

- **Section 17. "UART"** (DS70582) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

REGISTER 24-5: RSCON: DCI RECEIVE SLOT CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RSE15	RSE14	RSE13	RSE12	RSE11	RSE10	RSE9	RSE8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RSE7	RSE6	RSE5	RSE4	RSE3	RSE2	RSE1	RSE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **RSE<15:0>:** Receive Slot Enable bits

1 = CSDI data is received during the individual time slot n

0 = CSDI data is ignored during the individual time slot n

REGISTER 24-6: TSCON: DCI TRANSMIT SLOT CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TSE15	TSE14	TSE13	TSE12	TSE11	TSE10	TSE9	TSE8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TSE7	TSE6	TSE5	TSE4	TSE3	TSE2	TSE1	TSE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **TSE<15:0>:** Transmit Slot Enable Control bits

1 = Transmit buffer contents are sent during the individual time slot n

0 = CSDO pin is tri-stated or driven to logic ‘0’ during the individual time slot, depending on the state of the CSDOM bit

32.1 DC Characteristics

TABLE 32-1: OPERATING MIPS VS. VOLTAGE

Characteristic	VDD Range (in Volts)	Temp Range (in °C)	Maximum MIPS
			dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814
—	2.95V-3.6V(1)	-40°C to +85°C	70
—	2.95V-3.6V(1)	-40°C to +125°C	60

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.

TABLE 32-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typ.	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
Extended Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+140	°C
Operating Ambient Temperature Range	TA	-40	—	+125	°C
Power Dissipation: Internal chip power dissipation: PINT = VDD x (IDD – Σ IOH) I/O Pin Power Dissipation: I/O = Σ ({VDD – VOH} x IOH) + Σ (VOL x IOL)	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θJA			W

TABLE 32-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Typ.	Max.	Unit	Notes
Package Thermal Resistance, 64-pin QFN (9x9 mm)	θJA	28	—	°C/W	1
Package Thermal Resistance, 64-pin TQFP (10x10 mm)	θJA	47	—	°C/W	1
Package Thermal Resistance, 100-pin TQFP (12x12 mm)	θJA	43	—	°C/W	1
Package Thermal Resistance, 100-pin TQFP (14x14 mm)	θJA	43	—	°C/W	1
Package Thermal Resistance, 121-pin TFBGA (10x10 mm)	θJA	40	—	°C/W	1
Package Thermal Resistance, 144-pin LQFP (20x20 mm)	θJA	33	—	°C/W	1
Package Thermal Resistance, 144-pin TQFP (16x16 mm)	θJA	33	—	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θJA) numbers are achieved by package simulations.

TABLE 32-6: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param.(2)	**Typ.(3)**	**Max.**	**Units**	**Conditions**		
Idle Current (IIDLE)(1)						
DC40d	6	10	mA	-40°C	3.3V	10 MIPS
DC40a	7	12	mA	+25°C		
DC40b	8	13	mA	+85°C		
DC40c	9	15	mA	+125°C		
DC42d	11	18	mA	-40°C	3.3V	20 MIPS
DC42a	12	20	mA	+25°C		
DC42b	13	21	mA	+85°C		
DC42c	15	24	mA	+125°C		
DC44d	23	37	mA	-40°C	3.3V	40 MIPS
DC44a	24	39	mA	+25°C		
DC44b	25	40	mA	+85°C		
DC44c	27	44	mA	+125°C		
DC45d	34	55	mA	-40°C	3.3V	60 MIPS
DC45a	35	56	mA	+25°C		
DC45b	36	58	mA	+85°C		
DC45c	38	61	mA	+125°C		
DC46d	39	63	mA	-40°C	3.3V	70 MIPS
DC46a	41	66	mA	+25°C		
DC46b	42	68	mA	+85°C		

Note 1: Base IIDLE current is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC Clock Overshoot/Undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- External Secondary Oscillator (SOSC) is disabled (i.e., SOSCO and SOSCI pins are configured as digital I/O inputs)
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{\text{MCLR}}$ = VDD, WDT and FSCM are disabled
- No peripheral modules are operating; however, every peripheral is being clocked (defined PMDx bits are set to zero and unimplemented PMDx bits are set to one)
- The NVMSIDL bit (NVMCON<12>) = 1 (i.e., Flash regulator is set to stand-by while the device is in Idle mode)
- JTAG is disabled

2: These parameters are characterized but not tested in manufacturing.

3: Data in “Typ” column is at 3.3V, +25ºC unless otherwise stated.

TABLE 32-8: DC CHARACTERISTICS: DOZE CURRENT (I_{DOZE})(1)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Parameter	**Typ.(2)**	**Max.**	**Doze Ratio**	**Units**	**Conditions**		
DC73a	57	86	1:2	mA	-40°C	3.3V	70 MIPS
DC73g	40	60	1:128	mA			
DC70a	58	87	1:2	mA	+25°C	3.3V	70 MIPS
DC70g	41	62	1:128	mA			
DC71a	58	87	1:2	mA	+85°C	3.3V	70 MIPS
DC71g	42	63	1:128	mA			
DC72a	53	80	1:2	mA	+125°C	3.3V	60 MIPS
DC72g	38	57	1:128	mA			

Note 1: I_{DOZE} is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all I_{DOZE} measurements are as follows:

- Oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail with Overshoot/Undershoot < 250 mV
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to V_{SS}
- $\overline{MCLR}$ = V_{DD}, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (defined PMDx bits are set to zero and unimplemented PMDx bits are set to one)
- CPU executing `while(1)` statement
- JTAG is disabled

2: Data in the “Typ” column is at 3.3V, +25ºC unless otherwise stated.

TABLE 32-9: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic**	**Min.**	**Typ(1)**	**Max.**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
DI10		I/O Pins	VSS	—	0.2 VDD	V	
DI11		PMP Pins	VSS	—	0.15 VDD	V	PMPTTL = 1
DI15		$\overline{\text{MCLR}}$	VSS	—	0.2 VDD	V	
DI16		I/O Pins with OSC1 or SOSCI	VSS	—	0.2 VDD	V	
DI18		I/O Pins with SDAx, SCLx	VSS	—	0.3 VDD	V	SMBus disabled
DI19		I/O Pins with SDAx, SCLx	VSS	—	0.8	V	SMBus enabled
	VIH	**Input High Voltage**					
DI20		I/O Pins Not 5V Tolerant(4)	0.7 VDD	—	VDD	V	
		I/O Pins 5V Tolerant(4)	0.7 VDD	—	5.3	V	
		PMP Pins	0.25 VDD + 0.8	—	—	V	PMPTTL = 1
		I/O Pins with SDAx, SCLx	0.7 VDD	—	5.3	V	SMBus disabled
		I/O Pins with SDAx, SCLx	2.1	—	5.3	V	SMBus enabled
	ICNPU	**Change Notification Pull-up Current**					
DI30			50	250	400	μA	VDD = 3.3V, VPIN = VSS
	ICNPD	**Change Notification Pull-down Current(10)**					
DI31			—	50	—	μA	VDD = 3.3V, VPIN = VDD

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: See **"Pin Diagrams"** for the 5V tolerant I/O pins.

5: VIL source < (VSS – 0.3). Characterized but not tested.

6: Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.

7: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.

8: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

9: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted, provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

10: These parameters are characterized, but not tested.

TABLE 32-50: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param.	**Symbol**	**Characteristic(3)**		**Min.**	**Max.**	**Units**	**Conditions**
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	—	µs	
			400 kHz mode	1.3	—	µs	
			1 MHz mode(1)	0.5	—	µs	
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	µs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	µs	Device must operate at a minimum of 10 MHz
			1 MHz mode(1)	0.5	—	µs	
IS20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(1)	—	100	ns	
IS21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(1)	—	300	ns	
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode(1)	100	—	ns	
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	µs	
			400 kHz mode	0	0.9	µs	
			1 MHz mode(1)	0	0.3	µs	
IS30	TSU:STA	Start Condition Setup Time	100 kHz mode	4.7	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	0.6	—	µs	
			1 MHz mode(1)	0.25	—	µs	
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4.0	—	µs	After this period, the first clock pulse is generated
			400 kHz mode	0.6	—	µs	
			1 MHz mode(1)	0.25	—	µs	
IS33	TSU:STO	Stop Condition Setup Time	100 kHz mode	4.7	—	µs	
			400 kHz mode	0.6	—	µs	
			1 MHz mode(1)	0.6	—	µs	
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	4	—	µs	
			400 kHz mode	0.6	—	µs	
			1 MHz mode(1)	0.25		µs	
IS40	TAA:SCL	Output Valid From Clock	100 kHz mode	0	3500	ns	
			400 kHz mode	0	1000	ns	
			1 MHz mode(1)	0	350	ns	
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode(1)	0.5	—	µs	
IS50	CB	Bus Capacitive Loading		—	400	pF	
IS51	TPGD	Pulse Gobbler Delay		65	390	ns	See **Note 2**

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

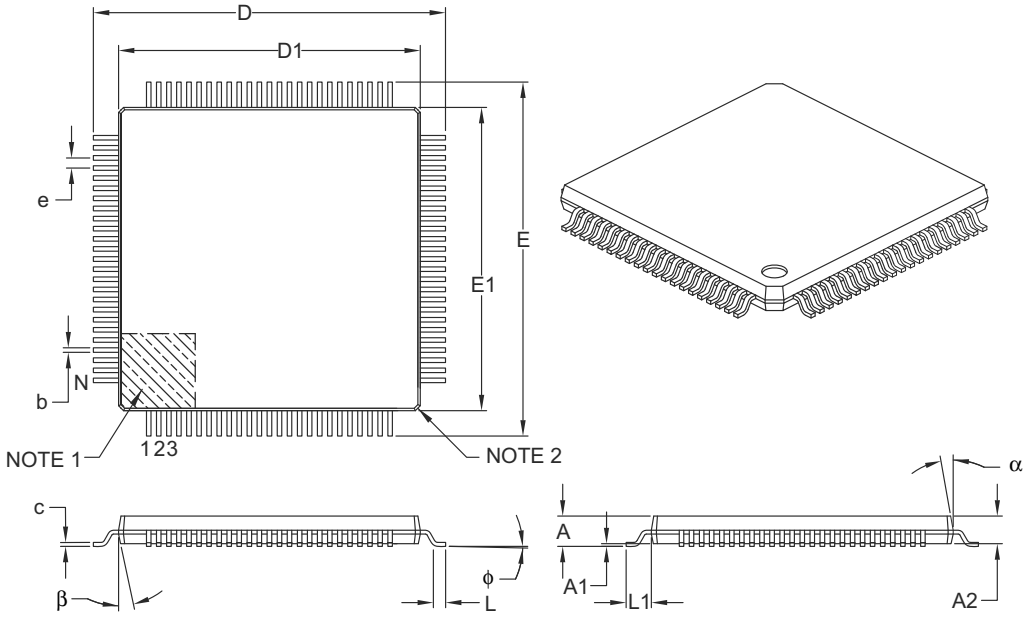
2: The typical value for this parameter is 130 ns.

3: These parameters are characterized, but not tested in manufacturing.

NOTES:

100-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		100	
Lead Pitch	e		0.40 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		14.00 BSC	
Overall Length	D		14.00 BSC	
Molded Package Width	E1		12.00 BSC	
Molded Package Length	D1		12.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.13	0.18	0.23
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-100B