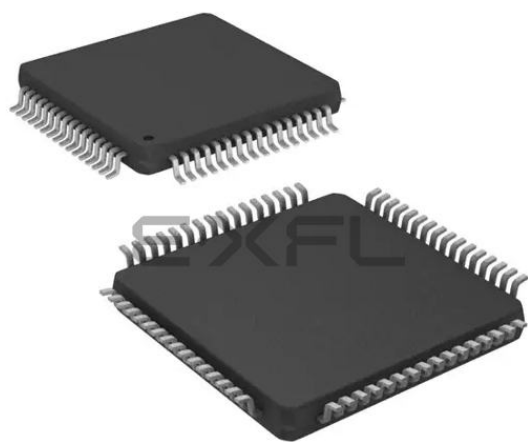




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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512mc806t-i-pt

Pin Diagrams (Continued)

121-Pin TFBGA⁽¹⁾

● = Pins are up to 5V tolerant

dsPIC33EP256MU810
dsPIC33EP512MU810

	1	2	3	4	5	6	7	8	9	10	11
A	○ RE4	○ RE3	● RG13	○ RE0	● RG0	● RF1	○ VDD	● NC	● RD12	● RD2	● RD1
B	● NC	● RG15	○ RE2	○ RE1	○ RA7	● RF0	○ VCAP	● RD5	● RD3	○ VSS	○ RC14
C	○ RE6	○ VDD	● RG12	● RG14	○ RA6	● NC	○ RD7	● RD4	● NC	○ RC13	● RD11
D	○ RC1	○ RE7	○ RE5	● NC	● NC	● NC	○ RD6	● RD13	● RD0	● NC	● RD10
E	○ RC4	○ RC3	○ RG6	○ RC2	● NC	● RG1	● NC	● RA15	● RD8	● RD9	● RA14
F	● MCLR	○ RG8	○ RG9	○ RG7	○ VSS	● NC	● NC	○ VDD	○ RC12	○ VSS	○ RC15
G	○ RE8	○ RE9	● RA0	● NC	○ VDD	○ VSS	○ VSS	● NC	● RA5	● RA3	● RA4
H	○ RB5	○ RB4	● NC	● NC	● NC	○ VDD	● NC	● VBUS	○ VUSB3V3	○ RG2	● RA2
J	○ RB3	○ RB2	○ RB7	○ AVDD	○ RB11	● RA1	○ RB12	● NC	● NC	● RF8	○ RG3
K	○ RB1	○ RB0	○ RA10	○ RB8	● NC	● RF12	○ RB14	○ VDD	● RD15	● RF3	● RF2
L	○ RB6	○ RA9	○ AVSS	○ RB9	○ RB10	● RF13	○ RB13	○ RB15	● RD14	● RF4	● RF5

Note 1: Refer to Table 2 for full pin names.

TABLE 4-4: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMU810 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	NVMIF	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	IC8IF	IC7IF	AD2IF	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	T6IF	DMA4IF	PMPIF	OC8IF	OC7IF	OC6IF	OC5IF	IC6IF	IC5IF	IC4IF	IC3IF	DMA3IF	C1IF	C1RXIF	SPI2IF	SPI2EIF	0000
IFS3	0806	—	RTCIF	DMA5IF	DCIIF	DCIEIF	QE11IF	PSEMIF	C2IF	C2RXIF	INT4IF	INT3IF	T9IF	T8IF	MI2C2IF	SI2C2IF	T7IF	0000
IFS4	0808	—	—	—	—	QE12IF	—	PSESMIF	—	C2TXIF	C1TXIF	DMA7IF	DMA6IF	CRCIF	U2EIF	U1EIF	—	0000
IFS5	080A	PWM2IF	PWM1IF	IC9IF	OC9IF	SPI3IF	SPI3EIF	U4TXIF	U4RXIF	U4EIF	USB1IF	—	—	U3TXIF	U3RXIF	U3EIF	—	0000
IFS6	080C	—	—	—	—	—	—	—	—	—	—	—	—	PWM6IF	PWM5IF	PWM4IF	PWM3IF	0000
IFS7	080E	IC11IF	OC11IF	IC10IF	OC10IF	SPI4IF	SPI4EIF	DMA11IF	DMA10IF	DMA9IF	DMA8IF	—	—	—	—	—	—	0000
IFS8	0810	—	ICDIF	IC16IF	OC16IF	IC15IF	OC15IF	IC14IF	OC14IF	IC13IF	OC13IF	—	DMA14IF	DMA13IF	DMA12IF	IC12IF	OC12IF	0000
IEC0	0820	NVMIE	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	IC8IE	IC7IE	AD2IE	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	T6IE	DMA4IE	PMPIE	OC8IE	OC7IE	OC6IE	OC5IE	IC6IE	IC5IE	IC4IE	IC3IE	DMA3IE	C1IE	C1RXIE	SPI2IE	SPI2EIE	0000
IEC3	0826	—	RTCIE	DMA5IE	DCIIE	DCIEIE	QE11IE	PSEMIE	C2IE	C2RXIE	INT4IE	INT3IE	T9IE	T8IE	MI2C2IE	SI2C2IE	T7IE	0000
IEC4	0828	—	—	—	—	QE12IE	—	PSESMIE	—	C2TXIE	C1TXIE	DMA7IE	DMA6IE	CRCIE	U2EIE	U1EIE	—	0000
IEC5	082A	PWM2IE	PWM1IE	IC9IE	OC9IE	SPI3IE	SPI3EIE	U4TXIE	U4RXIE	U4EIE	USB1IE	—	—	U3TXIE	U3RXIE	U3EIE	—	0000
IEC6	082C	—	—	—	—	—	—	—	—	—	—	—	—	PWM6IE	PWM5IE	PWM4IE	PWM3IE	0000
IEC7	082E	IC11IE	OC11IE	IC10IE	OC10IE	SPI4IE	SPI4EIE	DMA11IE	DMA10IE	DMA9IE	DMA8IE	—	—	—	—	—	—	0000
IEC8	0830	—	ICDIE	IC16IE	OC16IE	IC15IE	OC15IE	IC14IE	OC14IE	IC13IE	OC13IE	—	DMA14IE	DMA13IE	DMA12IE	IC12IE	OC12IE	0000
IPC0	0840	—	T1IP<2:0>			—	OC1IP<2:0>			—	IC1IP<2:0>			—	INT0IP<2:0>			4444
IPC1	0842	—	T2IP<2:0>			—	OC2IP<2:0>			—	IC2IP<2:0>			—	DMA0IP<2:0>			4444
IPC2	0844	—	U1RXIP<2:0>			—	SPI1IP<2:0>			—	SPI1EIP<2:0>			—	T3IP<2:0>			4444
IPC3	0846	—	NVMIP<2:0>			—	DMA1IP<2:0>			—	AD1IP<2:0>			—	U1TXIP<2:0>			4444
IPC4	0848	—	CNIP<2:0>			—	CMIP<2:0>			—	MI2C1IP<2:0>			—	SI2C1IP<2:0>			4444
IPC5	084A	—	IC8IP<2:0>			—	IC7IP<2:0>			—	AD2IP<2:0>			—	INT1IP<2:0>			4444
IPC6	084C	—	T4IP<2:0>			—	OC4IP<2:0>			—	OC3IP<2:0>			—	DMA2IP<2:0>			4444
IPC7	084E	—	U2TXIP<2:0>			—	U2RXIP<2:0>			—	INT2IP<2:0>			—	T5IP<2:0>			4444
IPC8	0850	—	C1IP<2:0>			—	C1RXIP<2:0>			—	SPI2IP<2:0>			—	SPI2EIP<2:0>			4444
IPC9	0852	—	IC5IP<2:0>			—	IC4IP<2:0>			—	IC3IP<2:0>			—	DMA3IP<2:0>			4444
IPC10	0854	—	OC7IP<2:0>			—	OC6IP<2:0>			—	OC5IP<2:0>			—	IC6IP<2:0>			4444
IPC11	0856	—	T6IP<2:0>			—	DMA4IP<2:0>			—	PMPIP<2:0>			—	OC8IP<2:0>			4444
IPC12	0858	—	T8IP<2:0>			—	MI2C2IP<2:0>			—	SI2C2IP<2:0>			—	T7IP<2:0>			4444
IPC13	085A	—	C2RXIP<2:0>			—	INT4IP<2:0>			—	INT3IP<2:0>			—	T9IP<2:0>			4444
IPC14	085C	—	DCIEIP<2:0>			—	QE11IP<2:0>			—	PSEMIP<2:0>			—	C2IP<2:0>			4444
IPC15	085E	—	—	—	—	—	RTCIP<2:0>			—	DMA5IP<2:0>			—	DCIIP<2:0>			0444

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMU806 DEVICES ONLY (CONTINUED)

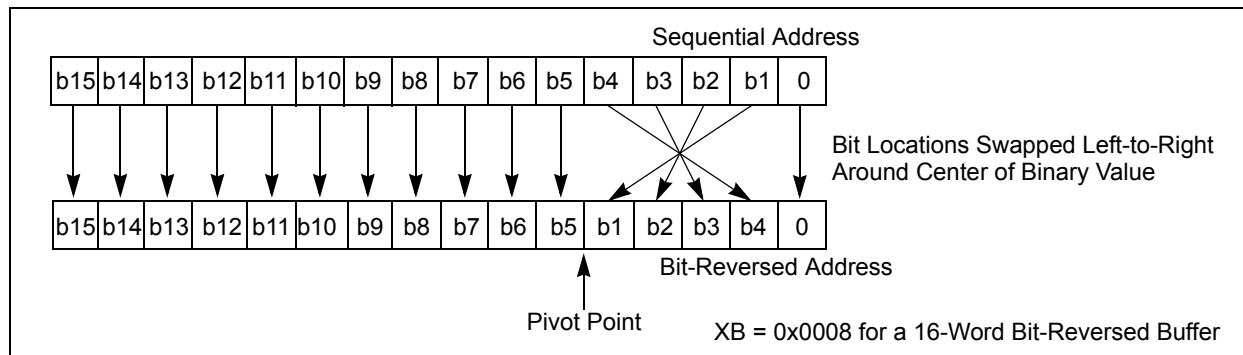
File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IPC16	0860	—	CRCIP<2:0>			—	U2EIP<2:0>			—	U1EIP<2:0>			—	—	—	—	4440
IPC17	0862	—	C2TXIP<2:0>			—	C1TXIP<2:0>			—	DMA7IP<2:0>			—	DMA6IP<2:0>			4444
IPC18	0864	—	QEI2IP<2:0>			—	—	—	—	—	PSESMIP<2:0>			—	—	—	—	4040
IPC20	0868	—	U3TXIP<2:0>			—	U3RXIP<2:0>			—	U3EIP<2:0>			—	—	—	—	4440
IPC21	086A	—	U4EIP<2:0>			—	USB1IP<2:0>			—	—	—	—	—	—	—	—	4400
IPC22	086C	—	SPI3IP<2:0>			—	SPI3EIP<2:0>			—	U4TXIP<2:0>			—	U4RXIP<2:0>			4444
IPC23	086E	—	PWM2IP<2:0>			—	PWM1IP<2:0>			—	IC9IP<2:0>			—	OC9IP<2:0>			4444
IPC24	0870	—	—	—	—	—	—	—	—	—	PWM4IP<2:0>			—	PWM3IP<2:0>			0044
IPC29	087A	—	DMA9IP<2:0>			—	DMA8IP<2:0>			—	—	—	—	—	—	—	—	4400
IPC30	087C	—	SPI4IP<2:0>			—	SPI4EIP<2:0>			—	DMA11IP<2:0>			—	DMA10IP<2:0>			4444
IPC31	087E	—	IC11IP<2:0>			—	OC11IP<2:0>			—	IC10IP<2:0>			—	OC10IP<2:0>			4444
IPC32	0880	—	DMA13IP<2:0>			—	DMA12IP<2:0>			—	IC12IP<2:0>			—	OC12IP<2:0>			4444
IPC33	0882	—	IC13IP<2:0>			—	OC13IP<2:0>			—	—	—	—	—	DMA14IP<2:0>			4404
IPC34	0884	—	IC15IP<2:0>			—	OC15IP<2:0>			—	IC14IP<2:0>			—	OC14IP<2:0>			4444
IPC35	0886	—	—	—	—	—	ICDIP<2:0>			—	IC16IP<2:0>			—	OC16IP<2:0>			0444
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFail	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	—	—	—	—	—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	—	—	—	—	—	—	—	—	—	UAE	DAE	DOOVR	—	—	—	—	0000
INTCON4	08C6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SGHT	0000
INTTREG	08C8	—	—	—	—	—	ILR<3:0>			VECNUM<7:0>								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-40: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXMU814 DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets		
RPINR35	06E6	—	IC14R<6:0>								—	IC13R<6:0>								0000
RPINR36	06E8	—	IC16R<6:0>								—	IC15R<6:0>								0000
RPINR37	06EA	—	SYNCI1R<6:0>								—	OCFCR<6:0>								0000
RPINR38	06EC	—	DTCMP1R<6:0>								—	SYNCI2R<6:0>								0000
RPINR39	06EE	—	DTCMP3R<6:0>								—	DTCMP2R<6:0>								0000
RPINR40	06F0	—	DTCMP5R<6:0>								—	DTCMP4R<6:0>								0000
RPINR41	06F2	—	DTCMP7R<6:0>								—	DTCMP6R<6:0>								0000
RPINR42	06F4	—	FLT6R<6:0>								—	FLT5R<6:0>								0000
RPINR43	06F6	—	—	—	—	—	—	—	—	—	FLT7R<6:0>								0000	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

FIGURE 4-11: BIT-REVERSED ADDRESS EXAMPLE**TABLE 4-76: BIT-REVERSED ADDRESS SEQUENCE (16-ENTRY)**

Normal Address					Bit-Reversed Address				
A3	A2	A1	A0	Decimal	A3	A2	A1	A0	Decimal
0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	0	0	0	8
0	0	1	0	2	0	1	0	0	4
0	0	1	1	3	1	1	0	0	12
0	1	0	0	4	0	0	1	0	2
0	1	0	1	5	1	0	1	0	10
0	1	1	0	6	0	1	1	0	6
0	1	1	1	7	1	1	1	0	14
1	0	0	0	8	0	0	0	1	1
1	0	0	1	9	1	0	0	1	9
1	0	1	0	10	0	1	0	1	5
1	0	1	1	11	1	1	0	1	13
1	1	0	0	12	0	0	1	1	3
1	1	0	1	13	1	0	1	1	11
1	1	1	0	14	0	1	1	1	7
1	1	1	1	15	1	1	1	1	15

5.0 FLASH PROGRAM MEMORY

Note 1: This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 5. “Flash Programming”** (DS70609) of the “dsPIC33E/PIC24E Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

- 2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices contain internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable during normal operation over the entire VDD range.

Flash memory can be programmed in two ways:

- In-Circuit Serial Programming™ (ICSP™) programming capability
- Run-Time Self-Programming (RTSP)

ICSP allows a dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 device to be serially programmed while in the end application circuit. This is done with two lines for programming clock and programming data (one of the alternate programming

pin pairs: PGECx/PGEDx), and three other lines for power (VDD), ground (VSS) and Master Clear ($\overline{\text{MCLR}}$). This allows customers to manufacture boards with unprogrammed devices and then program the device just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

RTSP is accomplished using TBLRD (table read) and TBLWT (table write) instructions. With RTSP, the user application can write program memory data either in blocks or ‘rows’ of 128 instructions (384 bytes) at a time or a single program memory word, and erase program memory in blocks or ‘pages’ of 1024 instructions (3072 bytes) at a time.

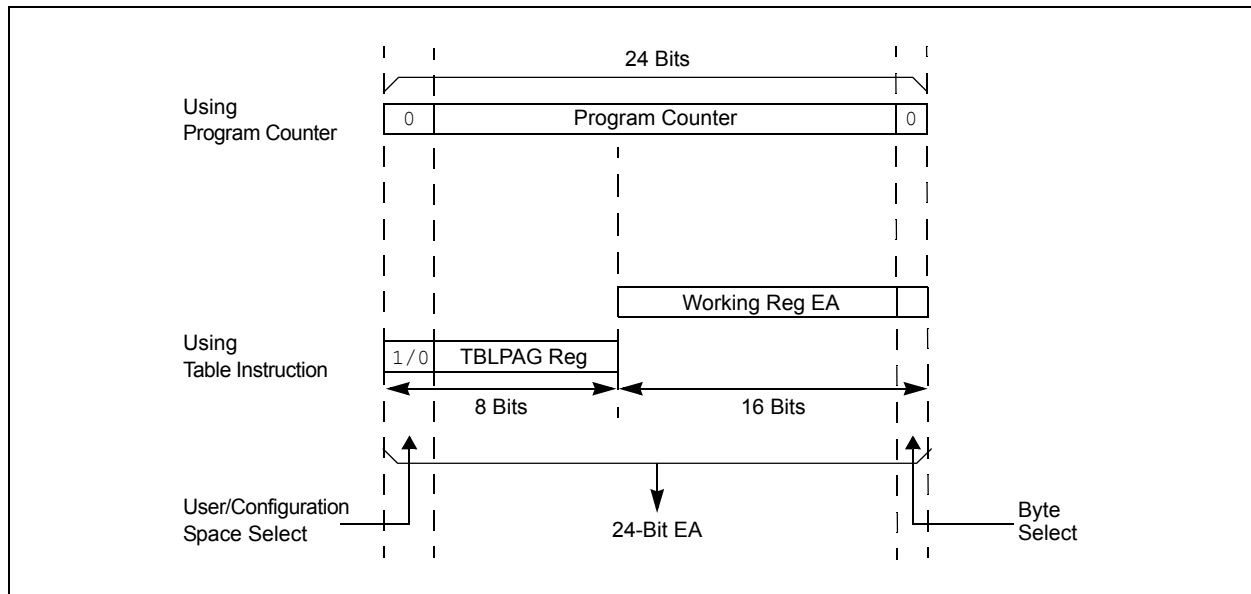
5.1 Table Instructions and Flash Programming

Regardless of the method used, all programming of Flash memory is done with the table read and table write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using bits<7:0> of the TBLPAG register and the Effective Address (EA) from a W register, specified in the table instruction, as shown in Figure 5-1.

The TBLRDL and the TBLWTL instructions are used to read or write to bits<15:0> of program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes.

The TBLRDH and TBLWTH instructions are used to read or write to bits<23:16> of program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS



REGISTER 5-1: NVMCON: NON-VOLATILE MEMORY (NVM) CONTROL REGISTER

R/SO-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0	U-0	U-0	U-0	U-0
WR	WREN	WRERR	NVMSIDL ⁽²⁾	—	—	—	—
bit 15				bit 8			

U-0	U-0	U-0	U-0	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾
—	—	—	—	NVMOP<3:0> ^(3,4)			
bit 7				bit 0			

Legend:	SO = Settable Only bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **WR:** Write Control bit⁽¹⁾
1 = Initiates a Flash memory program or erase operation; the operation is self-timed and the bit is cleared by hardware once operation is complete
0 = Program or erase operation is complete and inactive
- bit 14 **WREN:** Write Enable bit⁽¹⁾
1 = Enables Flash program/erase operations
0 = Inhibits Flash program/erase operations
- bit 13 **WRERR:** Write Sequence Error Flag bit⁽¹⁾
1 = An improper program or erase sequence attempt or termination has occurred (bit is set automatically on any set attempt of the WR bit)
0 = The program or erase operation completed normally
- bit 12 **NVMSIDL:** NVM Stop-in-Idle Control bit⁽²⁾
1 = Flash voltage regulator goes into Stand-by mode during Idle mode
0 = Flash voltage regulator is active during Idle mode
- bit 11-4 **Unimplemented:** Read as '0'
- bit 3-0 **NVMOP<3:0>:** NVM Operation Select bits^(1,3,4)
1111 = Reserved
1110 = Reserved
1101 = Bulk erase primary program Flash memory
1100 = Reserved
1011 = Reserved
1010 = Bulk erase auxiliary program Flash memory
0011 = Memory page erase operation
0010 = Memory row program operation
0001 = Memory word program operation⁽⁵⁾
0000 = Program a single Configuration register byte

- Note 1:** These bits can only be reset on a POR.
- 2:** If this bit is set, upon exiting Idle mode, there is a delay (TVREG) before Flash memory becomes operational.
- 3:** All other combinations of NVMOP<3:0> are unimplemented.
- 4:** Execution of the PWRSAV instruction is ignored while any of the NVM operations are in progress.
- 5:** Two adjacent words are programmed during execution of this operation.

REGISTER 9-3: PLLFBD: PLL FEEDBACK DIVISOR REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	PLLDIV<8>
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
PLLDIV<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as '0'

bit 8-0 **PLLDIV<8:0>:** PLL Feedback Divisor bits (also denoted as 'M', PLL multiplier)

11111111 = 513

•

•

•

000110000 = 50 (default)

•

•

•

000000010 = 4

000000001 = 3

000000000 = 2

Note 1: This register is reset only on a Power-on Reset (POR).

REGISTER 11-33: RPINR33: PERIPHERAL PIN SELECT INPUT REGISTER 33

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IC10R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IC9R<6:0>						
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **IC10R<6:0>:** Assign Input Capture 10 (IC10) to the Corresponding RPn/RPIn Pin bits
(see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.
. .
.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **IC9R<6:0>:** Assign Input Capture 9 (IC9) to the Corresponding RPn/RPIn Pin bits
(see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.
. .
.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

REGISTER 11-57: RPOR13: PERIPHERAL PIN SELECT OUTPUT REGISTER 13

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP118R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP113R<5:0>					
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'bit 13-8 **RP118R<5:0>**: Peripheral Output Function is Assigned to RP118 Output Pin bits
(see Table 11-3 for peripheral function numbers)bit 7-6 **Unimplemented:** Read as '0'bit 5-0 **RP113R<5:0>**: Peripheral Output Function is Assigned to RP113 Output Pin bits
(see Table 11-3 for peripheral function numbers)**REGISTER 11-58: RPOR14: PERIPHERAL PIN SELECT OUTPUT REGISTER 14**

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP125R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP120R<5:0>					
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'bit 13-8 **RP125R<5:0>**: Peripheral Output Function is Assigned to RP125 Output Pin bits
(see Table 11-3 for peripheral function numbers)bit 7-6 **Unimplemented:** Read as '0'bit 5-0 **RP120R<5:0>**: Peripheral Output Function is Assigned to RP120 Output Pin bits
(see Table 11-3 for peripheral function numbers)

12.1 Timer Resources

Many useful resources related to Timers are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310
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12.1.1 KEY RESOURCES

- **Section 11. “Timers”** (DS70362) in the *“dsPIC33E/PIC24E Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *“dsPIC33E/PIC24E Family Reference Manual”* Sections
- Development Tools

REGISTER 17-7: VELxCNT: VELOCITY COUNTER x REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VELCNT<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VELCNT<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **VELCNT<15:0>**: Velocity Counter bits

REGISTER 17-8: INDXCNT: INDEX COUNTER x HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INDXCNT<31:24>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INDXCNT<23:16>							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **INDXCNT<31:16>**: High Word Used to Form 32-Bit Index Counter Register (INDXxCNT) bits

REGISTER 17-9: INDXCNTL: INDEX COUNTER x LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INDXCNT<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INDXCNT<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **INDXCNT<15:0>**: Low Word Used to Form 32-Bit Index Counter Register (INDXxCNT) bits

REGISTER 17-18: INTxTMRL: INTERVAL TIMER x LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTTMR<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTTMR<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **INTTMR<15:0>**: Low Word Used to Form 32-Bit Interval Timer Register (INTxTMR) bits**REGISTER 17-19: INTxHLDH: INTERVAL TIMER x HOLD HIGH WORD REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<31:24>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<23:16>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **INTHLD<31:16>**: Hold Register for Reading and Writing INTxTMRH bits**REGISTER 17-20: INTxHLDL: INTERVAL TIMER x HOLD LOW WORD REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **INTHLD<15:0>**: Hold Register for Reading and Writing INTxTMRL bits

20.1 UARTx Helpful Tips

1. In multi-node direct-connect UARTx networks, UARTx receive inputs react to the complementary logic level defined by the URXINV bit (UxMODE<4>), which defines the Idle state, the default of which is logic high (i.e., URXINV = 0). Because remote devices do not initialize at the same time, it is likely that one of the devices, because the RX line is floating, will trigger a Start bit detection and will cause the first byte received, after the device has been initialized, to be invalid. To avoid this situation, the user should use a pull-up or pull-down resistor on the RX pin depending on the value of the URXINV bit.
 - a) If URXINV = 0, use a pull-up resistor on the RX pin.
 - b) If URXINV = 1, use a pull-down resistor on the RX pin.
2. The first character received on a wake-up from Sleep mode, caused by activity on the UxRX pin of the UARTx module, will be invalid. In Sleep mode, peripheral clocks are disabled. By the time the oscillator system has restarted and stabilized from Sleep mode, the baud rate bit sampling clock, relative to the incoming UxRX bit timing, is no longer synchronized resulting in the first character being invalid. This is to be expected.

20.2 UARTx Resources

Many useful resources related to the UARTx are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310>

20.2.1 KEY RESOURCES

- **Section 17. “UART”** (DS70582) in the *“dsPIC33E/PIC24E Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *“dsPIC33E/PIC24E Family Reference Manual”* Sections
- Development Tools

FIGURE 32-18: SPI1, SPI3 AND SPI4 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS

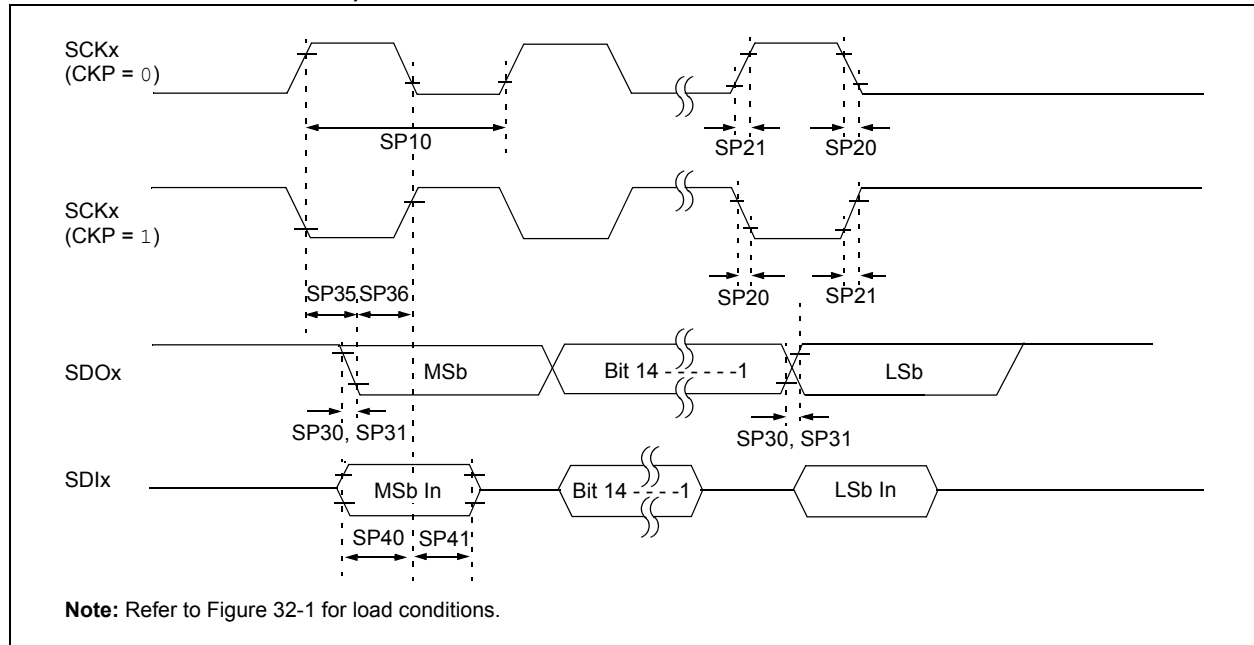


TABLE 32-36: SPI1, SPI3 AND SPI4 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP10	TscP	Maximum SCKx Frequency	—	—	9	MHz	-40°C to +125°C and see Note 3
SP20	TscF	SCKx Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP21	TscR	SCKx Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid After SCKx Edge	—	6	20	ns	
SP36	TdoV2sch, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2sch, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCKx is 111 ns. The clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

FIGURE 32-21: SPI1, SPI3 AND SPI4 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS

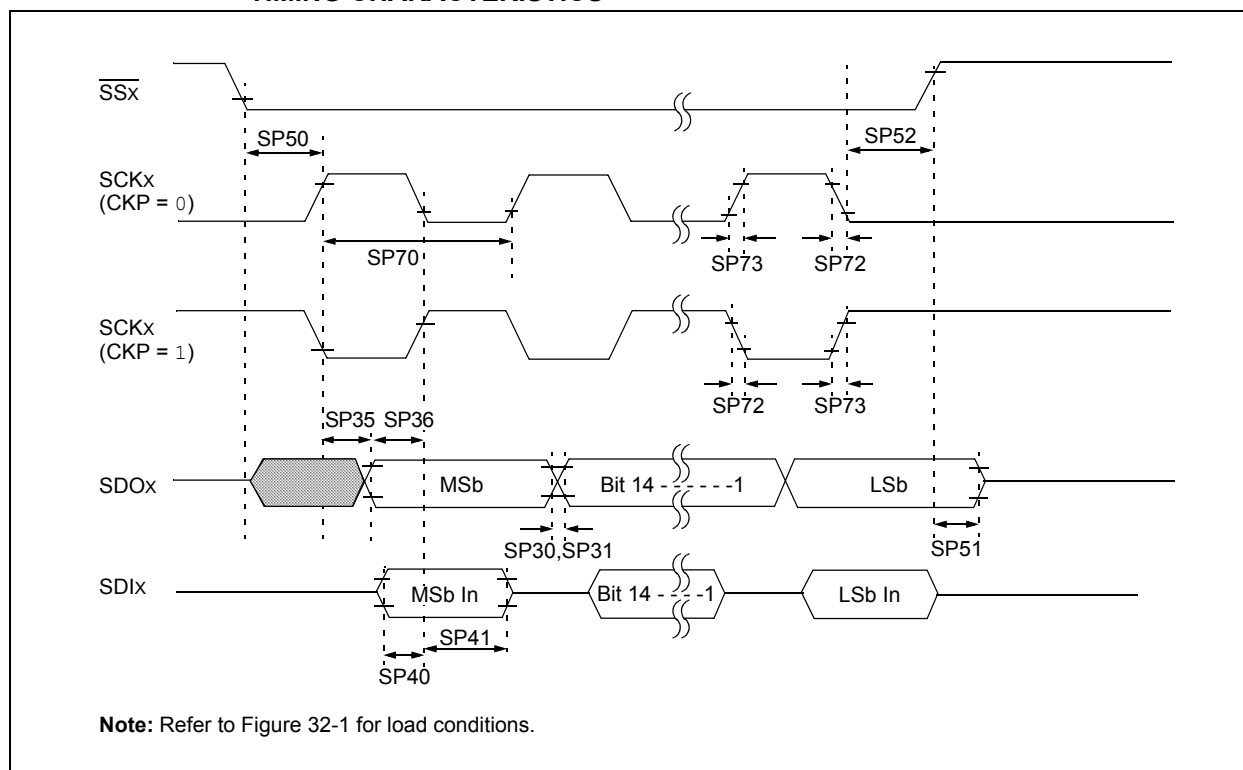


TABLE 32-46: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	TscP	Maximum SCKx Input Frequency	—	—	11	MHz	See Note 3
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↑ or SCKx ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output, High-Impedance	10	—	50	ns	See Note 4
SP52	Tsch2ssH, TscL2ssH	$\overline{SSx}$ ↑ after SCKx Edge	1.5 TCY + 40	—	—	ns	See Note 4
SP60	TssL2doV	SDOx Data Output Valid after $\overline{SSx}$ Edge	—	—	50	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCKx is 91 ns. Therefore, the SCKx clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

FIGURE 32-29: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS

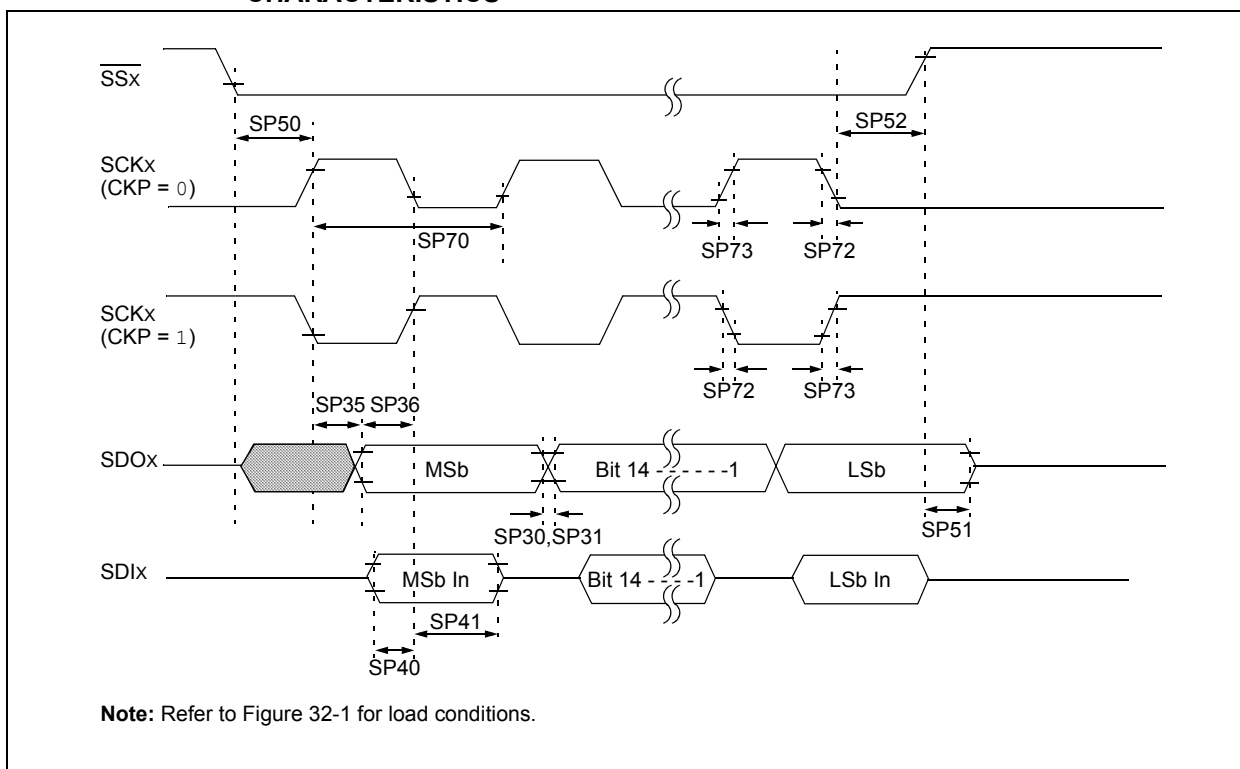
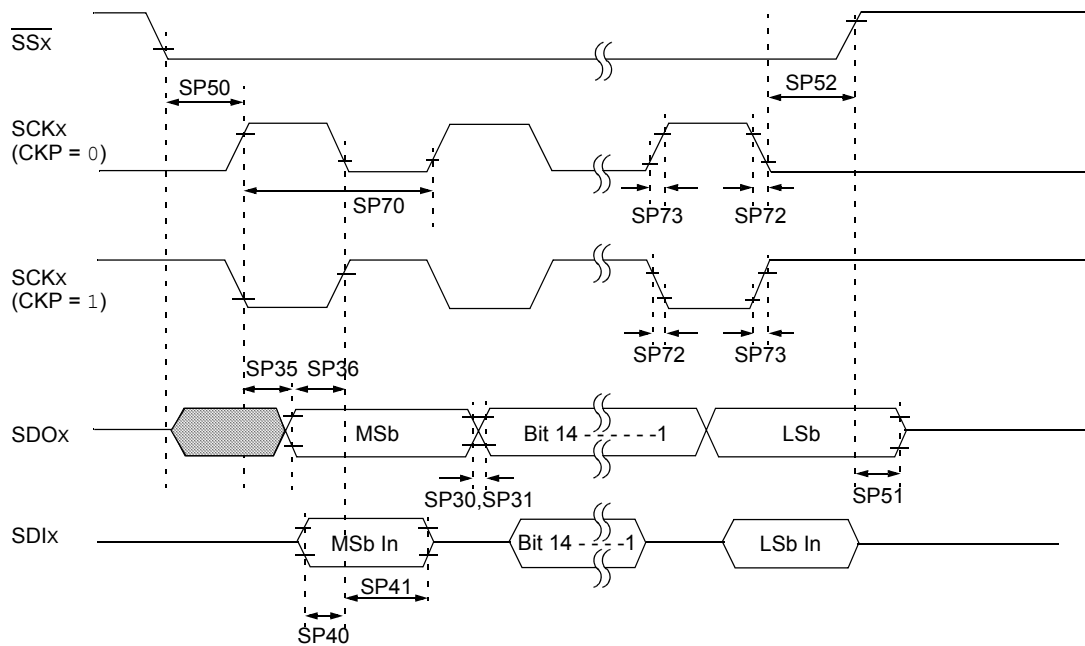


FIGURE 32-30: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 32-1 for load conditions.

FIGURE 32-43: PARALLEL MASTER PORT READ TIMING DIAGRAM

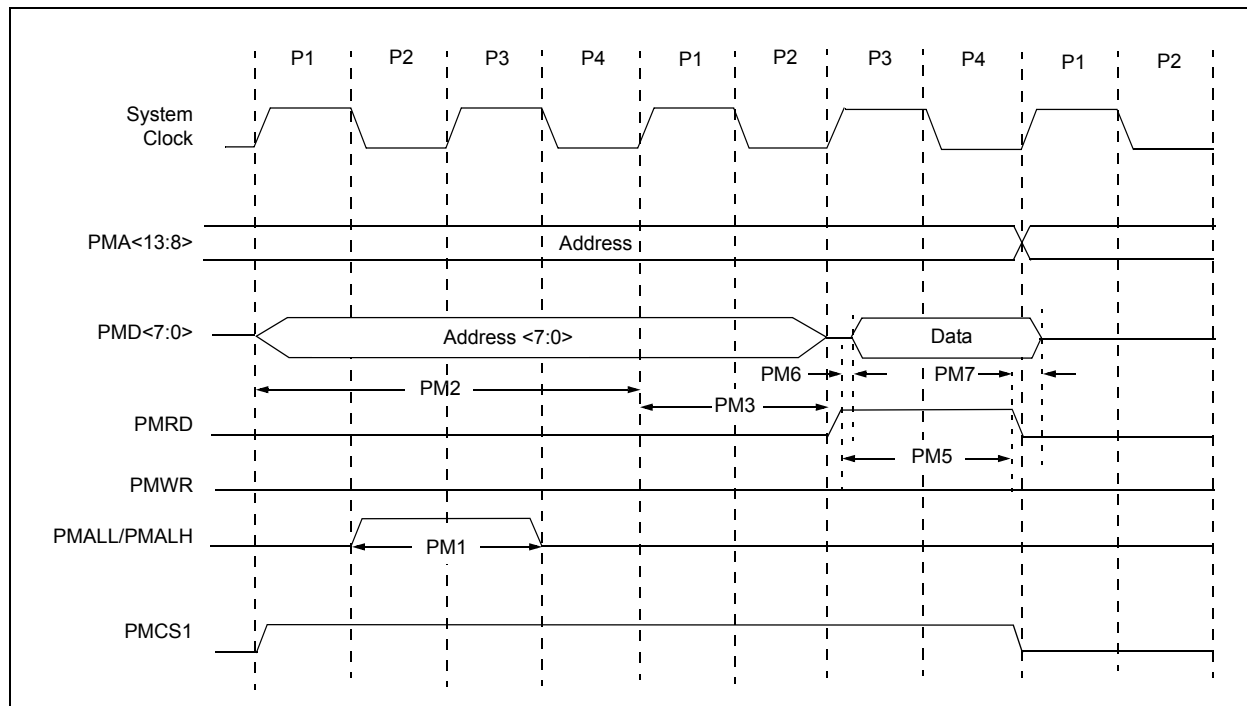


TABLE 32-66: PARALLEL MASTER PORT READ TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param.	Characteristic ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
PM1	PMALL/PMALH Pulse Width	—	0.5 T _{CY}	—	ns	
PM2	Address Out Valid to PMALL/PMALH Invalid (address setup time)	—	1 T _{CY}	—	ns	
PM3	PMALL/PMALH Invalid to Address Out Invalid (address hold time)	—	0.5 T _{CY}	—	ns	
PM5	PMRD Pulse Width	—	0.5 T _{CY}	—	ns	
PM6	PMRD or PMENB Active to Data In Valid (data setup time)	150	—	—	ns	
PM7	PMRD or PMENB Inactive to Data In Invalid (data hold time)	—	—	5	ns	

Note 1: These parameters are characterized, but not tested in manufacturing.