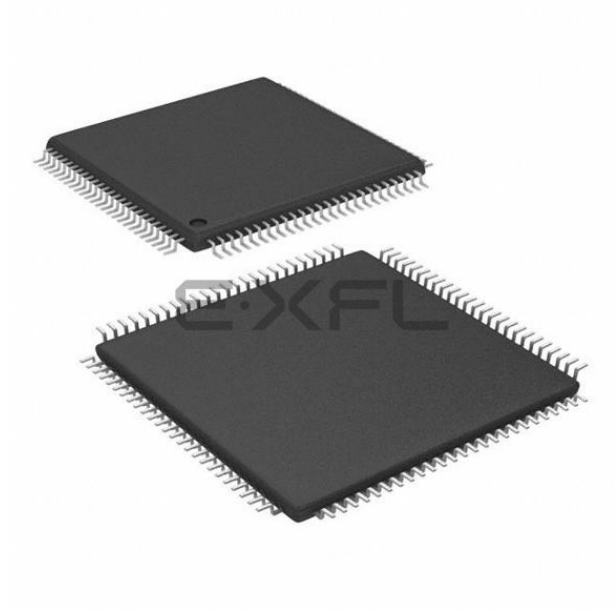
Microchip Technology - DSPIC33EP512MU810-E/PF Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, QEI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	83
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512mu810-e-pf

TABLE 3: PIN NAMES: PIC24EP256GU810 AND PIC24EP512GU810 DEVICES(1,2)

Pin Number	Full Pin Name
A1	AN28/PMD4/RP84/RE4
A2	AN27/PMD3/RPI83/RE3
A3	RP125/RG13
A4	AN24/PMD0/RP80/RE0
A5	RP112/RG0
A6	VCMPST2/RP97/RF1
A7	VDD
A8	No Connect
A9	RPI76/RD12
A10	DPH/RP66/RD2
A11	VCPCON/RP65/RD1
B1	No Connect
B2	RP127/RG15
B3	AN26/PMD2/RP82/RE2
B4	AN25/PMD1/RPI81/RE1
B5	AN23/RPI23/RA7
B6	VCMPST1/RP96/RF0
B7	VCAP
B8	PMRD/RP69/RD5
B9	PMBE/RP67/RD3
B10	VSS
B11	PGEC2/SOSCO/C3IN1-/T1CK/RPI62/RC14
C1	AN30/PMD6/RPI86/RE6
C2	VDD
C3	RPI124/RG12
C4	RP126/RG14
C5	AN22/RPI22/RA6
C6	No Connect
C7	C3IN1+/VCMPST3/RP71/RD7
C8	PMWR/RP68/RD4
C9	No Connect
C10	PGED2/SOSCI/C3IN3-/RPI61/RC13
C11	PMCS1/RPI75/RD11
D1	AN16/RPI49/RC1
D2	AN31/PMD7/RP87/RE7
D3	AN29/PMD5/RP85/RE5
D4	No Connect
D5	No Connect
D6	No Connect
D7	C3IN2-/RP70/RD6
D8	RPI77/RD13
D9	INT0/DMH/RP64/RD0
D10	No Connect
D11	ASCL1(3)/PMCS2/RPI74/RD10

Pin Number	Full Pin Name
E8	RPI31/RA15
E9	RTCC/DMLN/RPI72/RD8
E10	ASDA1(3)/DPLN/RPI73/RD9
E11	RPI30/RA14
F1	$\overline{\text{MCLR}}$
F2	C2IN3-/SDO2/PMA3/RP120/RG8
F3	C2IN1-/PMA2/RPI121/RG9
F4	C1IN1-/SDI2/PMA4/RPI119/RG7
F5	VSS
F6	No Connect
F7	No Connect
F8	VDD
F9	OSC1/RPI60/RC12
F10	VSS
F11	OSC2/CLKO/RC15
G1	AN20/RPI88/RE8
G2	AN21/RPI89/RE9
G3	TMS/RPI16/RA0
G4	No Connect
G5	VDD
G6	VSS
G7	VSS
G8	No Connect
G9	TDO/RPI21/RA5
G10	ASDA2(3)/RPI19/RA3
G11	TDI/RPI20/RA4
H1	AN5/C1IN1+/VBUSON/VBUSST/RPI37/RB5
H2	AN4/C1IN2-/USBOEN/RPI36/RB4
H3	No Connect
H4	No Connect
H5	No Connect
H6	VDD
H7	No Connect
H8	VBUS
H9	VUSB3V3
H10	D+/RG2(4)
H11	ASCL2(3)/RPI18/RA2
J1	AN3/C2IN1+/VPIO/RPI35/RB3
J2	AN2/C2IN2-/VMIO/RPI34/RB2
J3	PGED1/AN7/RCV/RPI39/RB7
J4	AVDD
J5	AN11/PMA12/RPI43/RB11
J6	TCK/RPI17/RA1
J7	AN12/PMA11/RPI44/RB12

Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The availability of I^2C™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

4: The pin name is SCL1/RG2 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.

5: The pin name is SDA1/RG3 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.

Referenced Sources

This device data sheet is based on the following individual chapters of the *"dsPIC33E/PIC24E Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note: To access the documents listed below, browse to the documentation section of the dsPIC33EP512MU814 product page on the Microchip web site (www.microchip.com).

In the event you are not able to access the product page using the link above, enter this URL in your browser:
http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310#1

- **Section 1. "Introduction"** (DS70573)
- **Section 2. "CPU"** (DS70359)
- **Section 3. "Data Memory"** (DS70595)
- **Section 4. "Program Memory"** (DS70613)
- **Section 5. "Flash Programming"** (DS70609)
- **Section 6. "Interrupts"** (DS70600)
- **Section 7. "Oscillator"** (DS70580)
- **Section 8. "Reset"** (DS70602)
- **Section 9. "Watchdog Timer and Power-Saving Modes"** (DS70615)
- **Section 10. "I/O Ports"** (DS70598)
- **Section 11. "Timers"** (DS70362)
- **Section 12. "Input Capture"** (DS70352)
- **Section 13. "Output Compare"** (DS70358)
- **Section 14. "High-Speed PWM"** (DS70645)
- **Section 15. "Quadrature Encoder Interface (QEI)"** (DS70601)
- **Section 16. "Analog-to-Digital Converter (ADC)"** (DS70621)
- **Section 17. "UART"** (DS70582)
- **Section 18. "Serial Peripheral Interface (SPI)"** (DS70569)
- **Section 19. "Inter-Integrated Circuit™ (I^2C™)"** (DS70330)
- **Section 20. "Data Converter Interface (DCI)"** (DS70356)
- **Section 21. "Enhanced Controller Area Network (ECAN™)"** (DS70353)
- **Section 22. "Direct Memory Access (DMA)"** (DS70348)
- **Section 23. "CodeGuard™ Security"** (DS70634)
- **Section 24. "Programming and Diagnostics"** (DS70608)
- **Section 25. "USB On-The-Go (OTG)"** (DS70571)
- **Section 26. "Op Amp/Comparator"** (DS70357)
- **Section 27. "Programmable Cyclic Redundancy Check (CRC)"** (DS70346)
- **Section 28. "Parallel Master Port (PMP)"** (DS70576)
- **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS70584)
- **Section 30. "Device Configuration"** (DS70618)

TABLE 4-49: PMD REGISTER MAP FOR dsPIC33EPXXXMU806 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	QEI1MD	PWMMD	DCIMD	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	C2MD	C1MD	AD1MD	0000
PMD2	0762	IC8MD	IC7MD	IC6MD	IC5MD	IC4MD	IC3MD	IC2MD	IC1MD	OC8MD	OC7MD	OC6MD	OC5MD	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	T9MD	T8MD	T7MD	T6MD	—	CMPMD	RTCCMD	PMPMD	CRCMD	—	QEI2MD	—	U3MD	—	I2C2MD	AD2MD	0000
PMD4	0766	—	—	—	—	—	—	—	—	—	—	U4MD	—	REFOMD	—	—	USB1MD	0000
PMD5	0768	IC16MD	IC15MD	IC14MD	IC13MD	IC12MD	IC11MD	IC10MD	IC9MD	OC16MD	OC15MD	OC14MD	OC13MD	OC12MD	OC11MD	OC10MD	OC9MD	0000
PMD6	076A	—	—	—	—	PWM4MD	PWM3MD	PWM2MD	PWM1MD	—	—	—	—	—	—	SPI4MD	SPI3MD	0000
PMD7	076C	—	—	—	—	—	—	—	—	DMA12MD	DMA8MD	DMA4MD	DMA0MD	—	—	—	—	0000
		—	—	—	—	—	—	—	—	DMA13MD	DMA9MD	DMA5MD	DMA1MD	—	—	—	—	0000
		—	—	—	—	—	—	—	—	DMA14MD	DMA10MD	DMA6MD	DMA2MD	—	—	—	—	0000
		—	—	—	—	—	—	—	—	—	DMA11MD	DMA7MD	DMA3MD	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-50: PMD REGISTER MAP FOR dsPIC33EPXXXMC806 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	QEI1MD	PWMMD	DCIMD	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	C2MD	C1MD	AD1MD	0000
PMD2	0762	IC8MD	IC7MD	IC6MD	IC5MD	IC4MD	IC3MD	IC2MD	IC1MD	OC8MD	OC7MD	OC6MD	OC5MD	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	T9MD	T8MD	T7MD	T6MD	—	CMPMD	RTCCMD	PMPMD	CRCMD	—	QEI2MD	—	U3MD	—	I2C2MD	AD2MD	0000
PMD4	0766	—	—	—	—	—	—	—	—	—	—	U4MD	—	REFOMD	—	—	—	0000
PMD5	0768	IC16MD	IC15MD	IC14MD	IC13MD	IC12MD	IC11MD	IC10MD	IC9MD	OC16MD	OC15MD	OC14MD	OC13MD	OC12MD	OC11MD	OC10MD	OC9MD	0000
PMD6	076A	—	—	—	—	PWM4MD	PWM3MD	PWM2MD	PWM1MD	—	—	—	—	—	—	SPI4MD	SPI3MD	0000
PMD7	076C	—	—	—	—	—	—	—	—	DMA12MD	DMA8MD	DMA4MD	DMA0MD	—	—	—	—	0000
		—	—	—	—	—	—	—	—	DMA13MD	DMA9MD	DMA5MD	DMA1MD	—	—	—	—	0000
		—	—	—	—	—	—	—	—	DMA14MD	DMA10MD	DMA6MD	DMA2MD	—	—	—	—	0000
		—	—	—	—	—	—	—	—	—	DMA11MD	DMA7MD	DMA3MD	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-54: DMAC REGISTER MAP (CONTINUED)

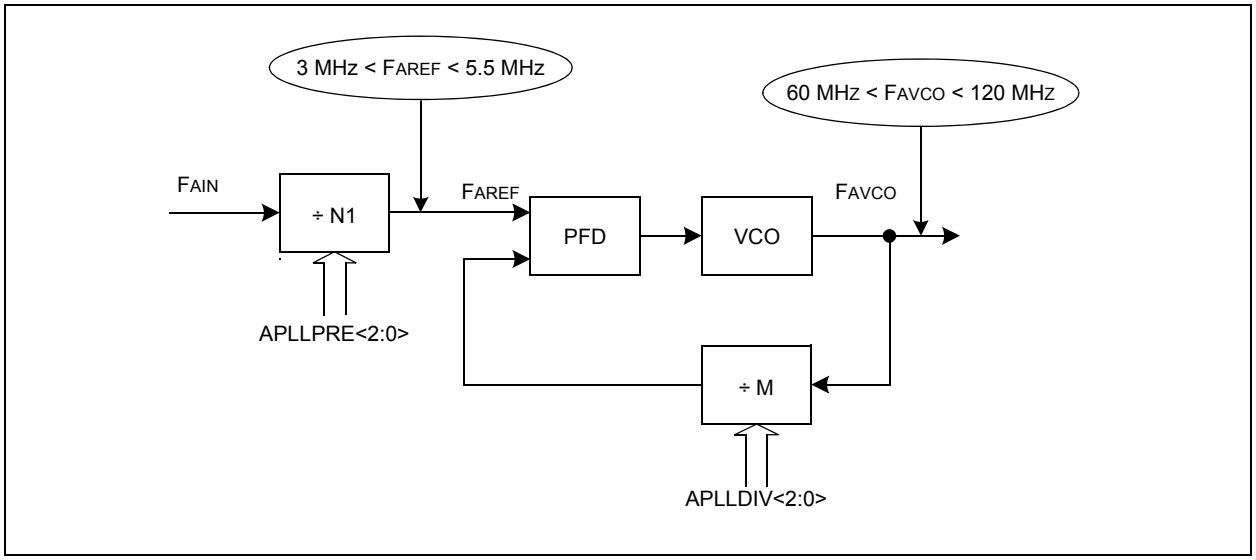
File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
DMA8STBH	0B8A	—	—	—	—	—	—	—	—	STB<23:16>								0000
DMA8PAD	0B8C	PAD<15:0>																0000
DMA8CNT	0B8E	—	—	CNT<13:0>														0000
DMA9CON	0B90	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000
DMA9REQ	0B92	FORCE	—	—	—	—	—	—	—	IRQSEL<7:0>								00FF
DMA9STAL	0B94	STA<15:0>																0000
DMA9STAH	0B96	—	—	—	—	—	—	—	—	STA<23:16>								0000
DMA9STBL	0B98	STB<15:0>																0000
DMA9STBH	0B9A	—	—	—	—	—	—	—	—	STB<23:16>								0000
DMA9PAD	0B9C	PAD<15:0>																0000
DMA9CNT	0B9E	—	—	CNT<13:0>														0000
DMA10CON	0BA0	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000
DMA10REQ	0BA2	FORCE	—	—	—	—	—	—	—	IRQSEL<7:0>								00FF
DMA10STAL	0BA4	STA<15:0>																0000
DMA10STAH	0BA6	—	—	—	—	—	—	—	—	STA<23:16>								0000
DMA10STBL	0BA8	STB<15:0>																0000
DMA10STBH	0BAA	—	—	—	—	—	—	—	—	STB<23:16>								0000
DMA10PAD	0BAC	PAD<15:0>																0000
DMA10CNT	0BAE	—	—	CNT<13:0>														0000
DMA11CON	0BB0	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000
DM11AREQ	0BB2	FORCE	—	—	—	—	—	—	—	IRQSEL<7:0>								00FF
DMA11STAL	0BB4	STA<15:0>																0000
DMA11STAH	0BB6	—	—	—	—	—	—	—	—	STA<23:16>								0000
DMA11STBL	0BB8	STB<15:0>																0000
DMA11STBH	0BBA	—	—	—	—	—	—	—	—	STB<23:16>								0000
DMA11PAD	0BBC	PAD<15:0>																0000
DMA11CNT	0BBE	—	—	CNT<13:0>														0000
DMA12CON	0BC0	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000
DMA12REQ	0BC2	FORCE	—	—	—	—	—	—	—	IRQSEL<7:0>								00FF
DMA12STAL	0BC4	STA<15:0>																0000
DMA12STAH	0BC6	—	—	—	—	—	—	—	—	STA<23:16>								0000
DMA12STBL	0BC8	STB<15:0>																0000
DMA12STBH	0BCA	—	—	—	—	—	—	—	—	STB<23:16>								0000
DMA12PAD	0BCC	PAD<15:0>																0000
DMA12CNT	0BCE	—	—	CNT<13:0>														0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Figure 9-3 illustrates a block diagram of the auxiliary PLL module.

Note:	The auxiliary PLL module is only available on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices.

FIGURE 9-3: APLL BLOCK DIAGRAM



Equation 9-4 shows the relationship between the auxiliary PLL input clock frequency (FAIN) and the AVCO frequency (FAVCO).

EQUATION 9-4: FAVCO CALCULATION

$$F_{AVCO} = F_{AIN} \times \left(\frac{M}{N1}\right)$$

10.5 Power-Saving Resources

Many useful resources related to Power-Saving features are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310

10.5.1 KEY RESOURCES

- **Section 9. "Watchdog Timer and Power-Saving Modes"** (DS70615) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

10.6 Special Function Registers

Seven registers, PMD1: Peripheral Module Disable Control Register 1 through PMD7: Peripheral Module Disable Control Register 7, are provided for peripheral module control.

REGISTER 11-40: RPINR40: PERIPHERAL PIN SELECT INPUT REGISTER 40

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	DTCMP5R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	DTCMP4R<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **DTCMP5R<6:0>:** Assign PWM Dead-Time Compensation Input 5 to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **DTCMP4R<6:0>:** Assign PWM Dead-Time Compensation Input 4 to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

18.1 SPI Helpful Tips

1. In Frame mode, if there is a possibility that the master may not be initialized before the slave:
   a) If FRMPOL (SPIxCON2<13>) = 1, use a pull-down resistor on SSx.
   b) If FRMPOL = 0, use a pull-up resistor on SSx.

Note:	This insures that the first frame transmission after initialization is not shifted or corrupted.

2. In Non-Framed 3-Wire mode, (i.e., not using SSx from a master):
   a) If CKP (SPIxCON1<6>) = 1, always place a pull-up resistor on SSx.
   b) If CKP = 0, always place a pull-down resistor on SSx.

Note:	This will insure that during power-up and initialization, the master/slave will not lose synchronization due to an errant SCKx transition that would cause the slave to accumulate data shift errors, for both transmit and receive, appearing as corrupted data.

3. FRMEN (SPIxCON2<15>) = 1 and SSEN (SPIxCON1<7>) = 1 are exclusive and invalid. In Frame mode, SCKx is continuous and the Frame Sync pulse is active on the SSx pin, which indicates the start of a data frame.

Note:	Not all third-party devices support Frame mode timing. Refer to the SPIx electrical characteristics for details.

4. In Master mode only, set the SMP bit (SPIxCON1<9>) to a '1' for the fastest SPI data rate possible. The SMP bit can only be set at the same time or after the MSTEN bit (SPIxCON1<5>) is set.

To avoid invalid slave read data to the master, the user's master software must ensure enough time for slave software to fill its write buffer before the user application initiates a master write/read cycle. It is always advisable to preload the SPIxBUF Transmit register in advance of the next master transaction cycle. SPIxBUF is transferred to the SPIx Shift register and is empty once the data transmission begins.

18.2 SPI Resources

Many useful resources related to SPI are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554301

18.2.1 KEY RESOURCES

- **Section 18. "Serial Peripheral Interface (SPI)"** (DS70569) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

REGISTER 18-3: SPIxCON2: SPIx CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
FRMEN	SPIFSD	FRMPOL	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	FRMDLY	SPIBEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **FRMEN:** Framed SPIx Support bit
1 = Framed SPIx support is enabled ($\overline{SSx}$ pin is used as a Frame Sync pulse input/output)
0 = Framed SPIx support is disabled

bit 14 **SPIFSD:** Frame Sync Pulse Direction Control bit
1 = Frame Sync pulse input (slave)
0 = Frame Sync pulse output (master)

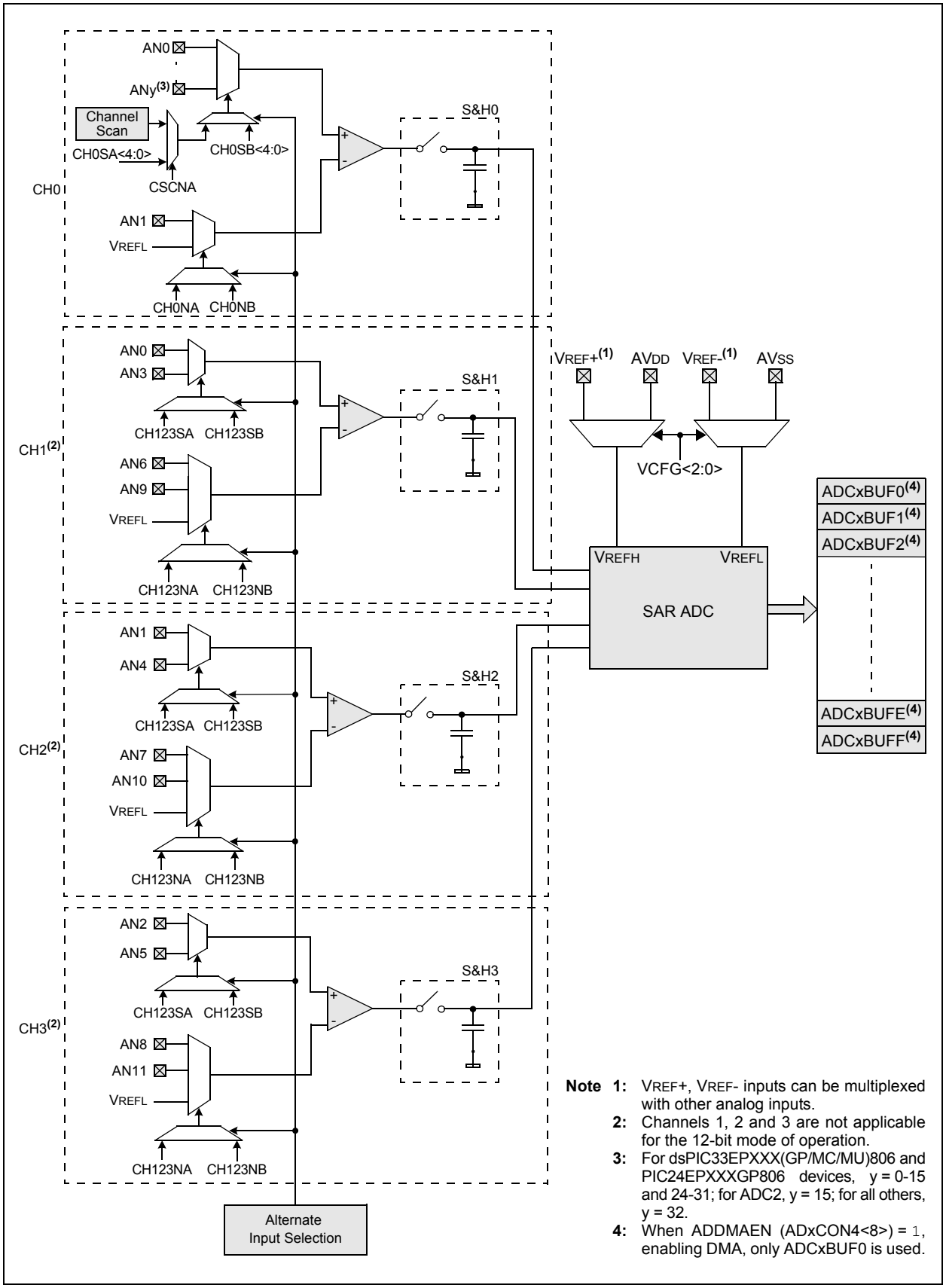
bit 13 **FRMPOL:** Frame Sync Pulse Polarity bit
1 = Frame Sync pulse is active-high
0 = Frame Sync pulse is active-low

bit 12-2 **Unimplemented:** Read as '0'

bit 1 **FRMDLY:** Frame Sync Pulse Edge Select bit
1 = Frame Sync pulse coincides with the first bit clock
0 = Frame Sync pulse precedes the first bit clock

bit 0 **SPIBEN:** Enhanced Buffer Enable bit
1 = Enhanced Buffer is enabled
0 = Enhanced Buffer is disabled (Standard mode)

FIGURE 23-1: ADCx MODULE BLOCK DIAGRAM



Note 1: VREF+, VREF- inputs can be multiplexed with other analog inputs.

2: Channels 1, 2 and 3 are not applicable for the 12-bit mode of operation.

3: For dsPIC33EPXXX(GP/MC/MU)806 and PIC24EPXXXGP806 devices, y = 0-15 and 24-31; for ADC2, y = 15; for all others, y = 32.

4: When ADDMAEN (ADxCON4<8>) = 1, enabling DMA, only ADCxBUF0 is used.

REGISTER 23-1: ADxCON1: ADCx CONTROL REGISTER 1 (CONTINUED)

bit 7-5 **SSRC<2:0>:** Sample Clock Source Select bits

If SSRCG = 1:
111 = Reserved
110 = PWM Generator 7 primary trigger compare ends sampling and starts conversion(2)
101 = PWM Generator 6 primary trigger compare ends sampling and starts conversion(2)
100 = PWM Generator 5 primary trigger compare ends sampling and starts conversion(2)
011 = PWM Generator 4 primary trigger compare ends sampling and starts conversion(2)
010 = PWM Generator 3 primary trigger compare ends sampling and starts conversion(2)
001 = PWM Generator 2 primary trigger compare ends sampling and starts conversion(2)
000 = PWM Generator 1 primary trigger compare ends sampling and starts conversion(2)

If SSRCG = 0:
111 = Internal counter ends sampling and starts conversion (auto-convert)
110 = Reserved
101 = PWM secondary Special Event Trigger ends sampling and starts conversion(2)
100 = Timer5 compare ends sampling and starts conversion
011 = PWM primary Special Event Trigger ends sampling and starts conversion(2)
010 = Timer3 compare ends sampling and starts conversion
001 = Active transition on the INT0 pin ends sampling and starts conversion
000 = Clearing the Sample bit (SAMP) ends sampling and starts conversion (Manual mode)

bit 4 **SSRCG:** Sample Clock Source Group bit

(See bits<7-5> for details.)

bit 3 **SIMSAM:** Simultaneous Sample Select bit (only applicable when CHPS<1:0> = 01 or 1x)

When AD12B = 1, SIMSAM is: U-0, Unimplemented, Read as '0'
1 = Samples CH0, CH1, CH2, CH3 simultaneously (when CHPS<1:0> = 1x); or samples CH0 and CH1 simultaneously (when CHPS<1:0> = 01)
0 = Samples multiple channels individually in sequence

bit 2 **ASAM:** ADC Sample Auto-Start bit(3)

1 = Sampling begins immediately after the last conversion; SAMP bit is auto-set
0 = Sampling begins when the SAMP bit is set

bit 1 **SAMP:** ADC Sample Enable bit

1 = ADC S&H amplifiers are sampling
0 = ADC S&H amplifiers are holding
If ASAM = 0, software can write '1' to begin sampling. Automatically set by hardware if ASAM = 1.
If SSRC = 000, software can write '0' to end sampling and start conversion. If SSRC ≠ 000, automatically cleared by hardware to end sampling and start conversion.

bit 0 **DONE:** ADC Conversion Status bit(3)

1 = ADC conversion cycle is completed.
0 = ADC conversion has not started or is in progress
Automatically set by hardware when ADC conversion is complete. Software can write '0' to clear the DONE status (software not allowed to write '1'). Clearing this bit does NOT affect any operation in progress. Automatically cleared by hardware at the start of a new conversion.

Note 1: This bit is only available in the ADC1 module. In the ADC2 module, this bit is unimplemented and is read as '0'.

2: This setting is available in dsPIC33EPXXX(MC/MU)806/810/814 devices only.

3: Do not clear the DONE bit in software if ADC Sample Auto-Start is enabled (ASAM = 1).

24.0 DATA CONVERTER INTERFACE (DCI) MODULE

Note 1: This data sheet is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Section 20. Data Converter Interface (DCI)"** (DS70356) of the *"dsPIC33E/PIC24E Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

24.1 Module Introduction

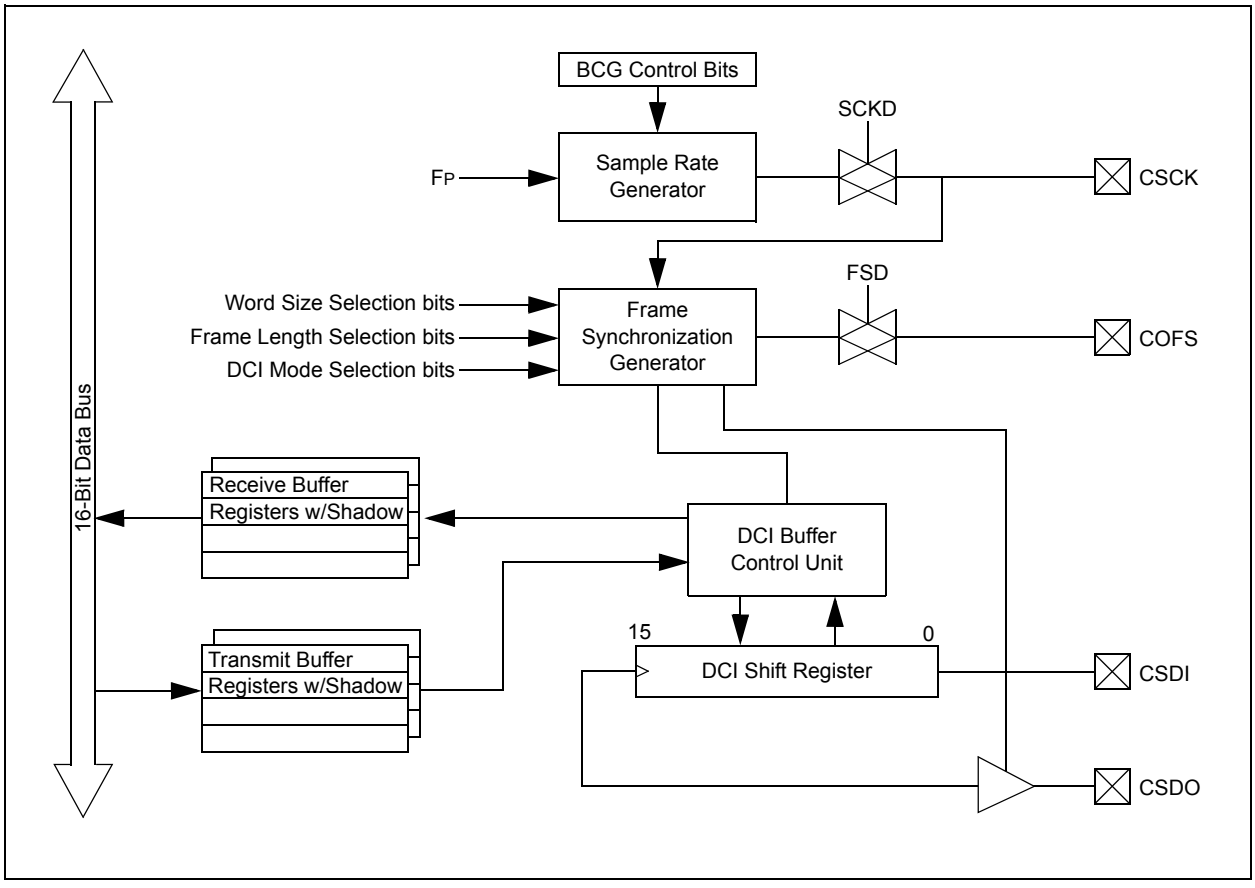
The Data Converter Interface (DCI) module allows simple interfacing of devices, such as audio coder/decoders (Codecs), ADC and D/A Converters. The following interfaces are supported:

- Framed Synchronous Serial Transfer (Single or Multi-Channel)
- Inter-IC Sound (I^2S) Interface
- AC-Link Compliant mode

General features include:

- Programmable word size up to 16 bits
- Supports up to 16 time slots, for a maximum frame size of 256 bits
- Data buffering for up to 4 samples without CPU overhead

FIGURE 24-1: DCI MODULE BLOCK DIAGRAM



24.2 DCI Resources

Many useful resources related to DCI are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310

24.2.1 KEY RESOURCES

- **Section 20. "Data Converter Interface (DCI)"** (DS70356) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

TABLE 32-10: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
DO10	VOL	**Output Low Voltage** I/O Pins: 4x Sink Driver Pins – All I/O Pins except OSC2 and SOSCO	—	—	0.4	V	IOL ≤ 10 mA, VDD = 3.3V
		Output Low Voltage I/O Pins: 8x Sink Driver Pins – OSC2 and SOSCO	—	—	0.4	V	IOL ≤ 15 mA, VDD = 3.3V
DO20	VOH	**Output High Voltage** I/O Pins: 4x Sink Driver Pins – All I/O Pins except OSC2 and SOSCO	2.4	—	—	V	IOH ≥ -10 mA, VDD = 3.3V
		Output High Voltage I/O Pins: 8x Sink Driver Pins – OSC2 and SOSCO	2.4	—	—	V	IOH ≥ -15 mA, VDD = 3.3V
DO20A	VOH1	**Output High Voltage** I/O Pins: 4x Sink Driver Pins – All I/O Pins except OSC2 and SOSCO	1.5(1)	—	—	V	IOH ≥ -14 mA, VDD = 3.3V
			2.0(1)	—	—		IOH ≥ -12 mA, VDD = 3.3V
			3.0(1)	—	—		IOH ≥ -7 mA, VDD = 3.3V
		Output High Voltage I/O Pins: 8x Sink Driver Pins – OSC2 and SOSCO	1.5(1)	—	—	V	IOH ≥ -22 mA, VDD = 3.3V
			2.0(1)	—	—		IOH ≥ -18 mA, VDD = 3.3V
			3.0(1)	—	—		IOH ≥ -10 mA, VDD = 3.3V

Note 1: Parameters are characterized, but not tested.

TABLE 32-11: ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(2) (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic**	**Min.(1)**	**Typ.**	**Max.**	**Units**	**Conditions**
BO10	VBOR	BOR Event on VDD Transition High-to-Low	2.7	—	2.9	V	VDD

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

2: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized.

FIGURE 32-7: TIMERQ (QEI MODULE) EXTERNAL CLOCK TIMING CHARACTERISTICS

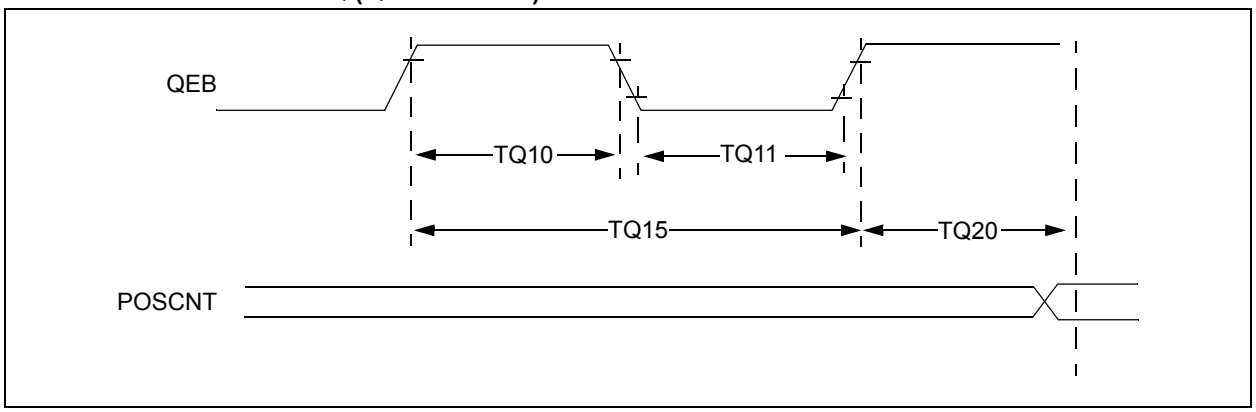
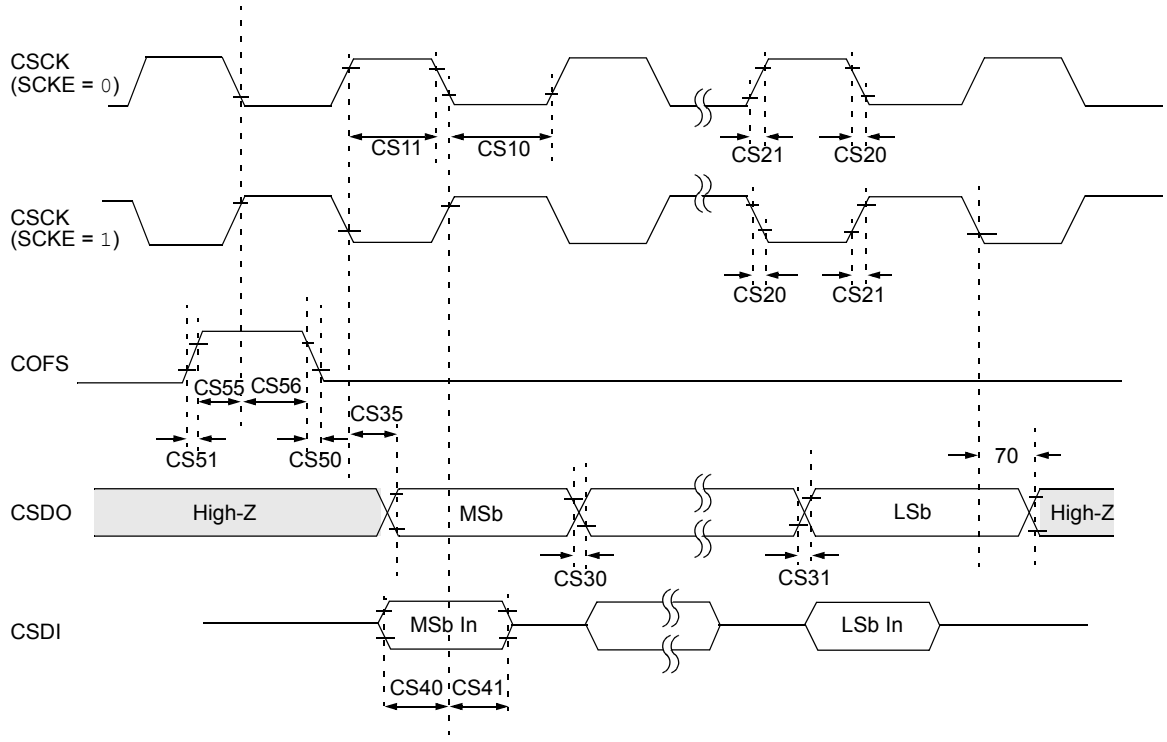


TABLE 32-26: QEI MODULE EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**		**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
TQ10	TtQH	TQCK High Time	Synchronous, with Prescaler	[Greater of (12.5 or 0.5 TCY)/N] + 25	—	—	ns	Must also meet Parameter TQ15
TQ11	TtQL	TQCK Low Time	Synchronous, with Prescaler	[Greater of (12.5 or 0.5 TCY)/N] + 25	—	—	ns	Must also meet Parameter TQ15
TQ15	TtQP	TQCP Input Period	Synchronous, with Prescaler	[Greater of (25 or TCY)/N] + 50	—	—	ns	
TQ20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		—	1	TCY	—	

Note 1: These parameters are characterized but not tested in manufacturing.

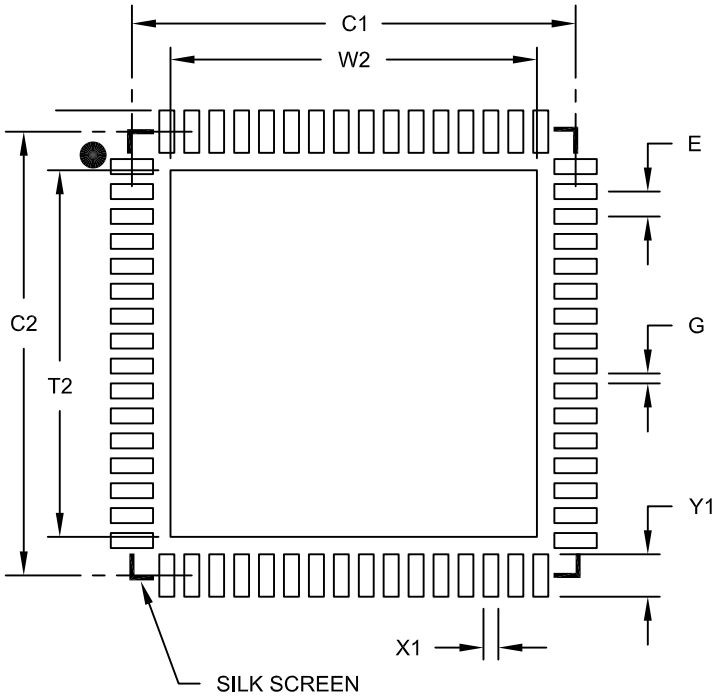
FIGURE 32-40: DCI MODULE (MULTI-CHANNEL, I²S MODES) TIMING CHARACTERISTICS



Note: Refer to Figure 32-1 for load conditions.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			7.35
Optional Center Pad Length	T2			7.35
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			0.85
Distance Between Pads	G	0.20		

Notes:

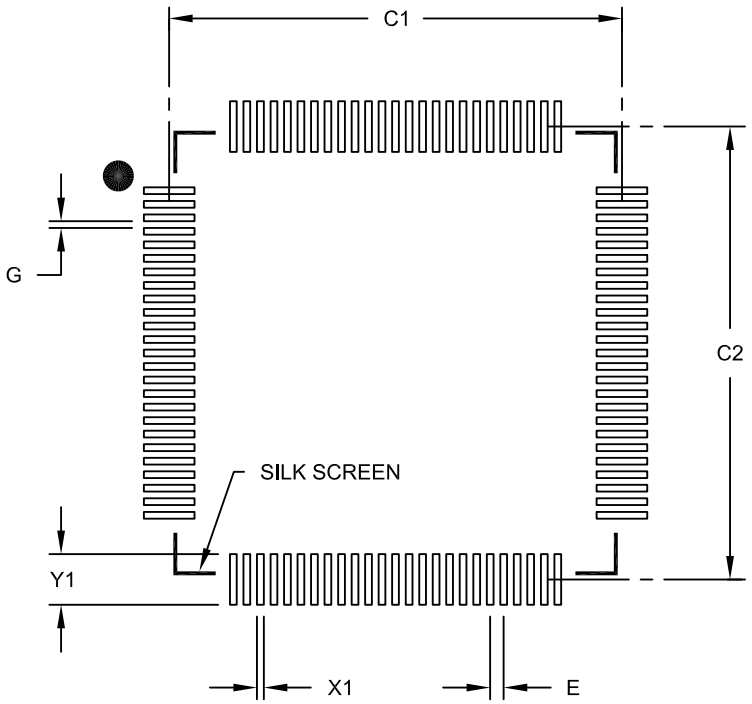
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2149A

100-Lead Plastic Thin Quad Flatpack (PT)- 12x12x1mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Contact Pad Spacing	C1		13.40	
Contact Pad Spacing	C2		13.40	
Contact Pad Width (X100)	X1			0.20
Contact Pad Length (X100)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2100B

APPENDIX A: REVISION HISTORY

Revision A (December 2009)

This is the initial released version of this document.

Revision B (July 2010)

This revision includes minor typographical and formatting changes throughout the data sheet text.

The major changes are referenced by their respective section in Table A-1.

TABLE A-1: MAJOR SECTION UPDATES

Section Name	Update Description
"High-Performance, 16-bit Digital Signal Controllers and Microcontrollers"	Removed reference to dual triggers for Motor Control Peripherals. Relocated the VBUSST pin in all pin diagrams (see **"Pin Diagrams"**, Table 2 and Table 3). Added SCK2, SDI2, SDO2 pins in pin location 4,5 and 6 respectively in 64-pin QFN. Added SCK2, SDI2, SDO2 pins in pin location 4,5 and 6 respectively in 64-pin TQFP. Added SCK2, SDI2, SDO2 pins in pin location 10,11 and 12 respectively in 100-pin TQFP. Added SCK2, SDI2, SDO2 pins in Table 2 and Table 3. Moved the RP30 pin to pin location 95, and the RP31 pin to pin location 96 in the 144-pin TQFP and 144-pin LQFP pin diagrams.
Section 1.0 "Device Overview"	Removed the SCL1 and SDA1 pins from the Pinout I/O Descriptions (see Table 1-1).
Section 2.0 "Guidelines for Getting Started with 16-bit Digital Signal Controllers and Microcontrollers"	Removed Section 2.8 "Configuration of Analog and Digital Pins During ICSP Operations"
Section 3.0 "CPU"	Added Note 4 to the CPU Status Register (SR) in Register 3-1. Added the VAR bit (CORCON<15>) to Register 3-2.

INDEX