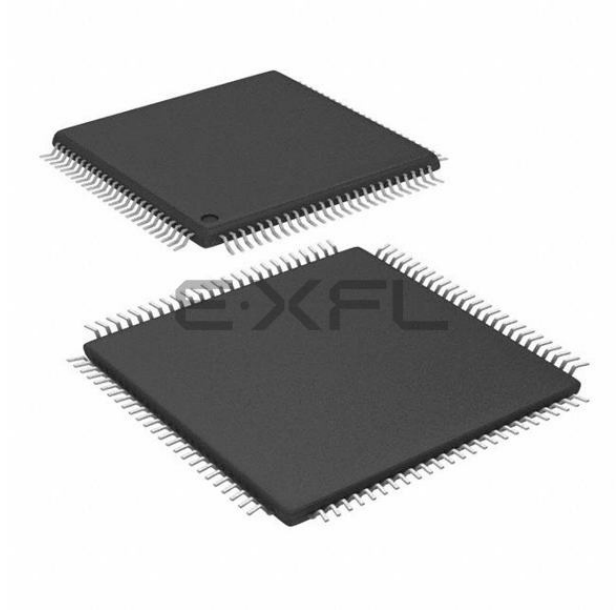
Microchip Technology - DSPIC33EP512MU810-I/PT Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, QEI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	83
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512mu810-i-pt

Pin Diagrams (Continued)

121-Pin TFBGA(1)

● = Pins are up to 5V tolerant

PIC24EP256GU810
PIC24EP512GU810

	1	2	3	4	5	6	7	8	9	10	11
A	RE4	RE3	RG13	RE0	RG0	RF1	VDD	NC	RD12	RD2	RD1
B	NC	RG15	RE2	RE1	RA7	RF0	VCAP	RD5	RD3	VSS	RC14
C	RE6	VDD	RG12	RG14	RA6	NC	RD7	RD4	NC	RC13	RD11
D	RC1	RE7	RE5	NC	NC	NC	RD6	RD13	RD0	NC	RD10
E	RC4	RC3	RG6	RC2	NC	RG1	NC	RA15	RD8	RD9	RA14
F	$\overline{\text{MCLR}}$	RG8	RG9	RG7	VSS	NC	NC	VDD	RC12	VSS	RC15
G	RE8	RE9	RA0	NC	VDD	VSS	VSS	NC	RA5	RA3	RA4
H	RB5	RB4	NC	NC	NC	VDD	NC	VBUS	VUSB3V3	RG2	RA2
J	RB3	RB2	RB7	AVDD	RB11	RA1	RB12	NC	NC	RF8	RG3
K	RB1	RB0	RA10	RB8	NC	RF12	RB14	VDD	RD15	RF3	RF2
L	RB6	RA9	AVSS	RB9	RB10	RF13	RB13	RB15	RD14	RF4	RF5

Note 1: Refer to Table 3 for full pin names.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	PPS	Description
SCL1(5)	I/O	ST	No	Synchronous serial clock input/output for I2C1.
SDA1(5)	I/O	ST	No	Synchronous serial data input/output for I2C1.
ASCL1(5)	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1.
ASDA1(5)	I/O	ST	No	Alternate synchronous serial data input/output for I2C1.
SCL2(5)	I/O	ST	No	Synchronous serial clock input/output for I2C2.
SDA2(5)	I/O	ST	No	Synchronous serial data input/output for I2C2.
ASCL2(5)	I/O	ST	No	Alternate synchronous serial clock input/output for I2C2.
ASDA2(5)	I/O	ST	No	Alternate synchronous serial data input/output for I2C2.
TMS	I	ST	No	JTAG Test mode select pin.
TCK	I	ST	No	JTAG test clock input pin.
TDI	I	ST	No	JTAG test data input pin.
TDO	O	—	No	JTAG test data output pin.
INDX1(1)	I	ST	Yes	Quadrature Encoder Index1 pulse input.
HOME1(1)	I	ST	Yes	Quadrature Encoder Home1 pulse input.
QEA1(1)	I	ST	Yes	Quadrature Encoder Phase A input in QEI1 mode. Auxiliary timer external clock input in Timer mode.
QEB1(1)	I	ST	Yes	Quadrature Encoder Phase A input in QEI1 mode. Auxiliary timer external gate input in Timer mode.
CNTCMP1(1)	O	—	Yes	Quadrature Encoder Compare Output 1.
INDX2(1)	I	ST	Yes	Quadrature Encoder Index2 pulse input.
HOME2(1)	I	ST	Yes	Quadrature Encoder Home2 pulse input.
QEA2(1)	I	ST	Yes	Quadrature Encoder Phase A input in QEI2 mode. Auxiliary timer external clock input in Timer mode.
QEB2(1)	I	ST	Yes	Quadrature Encoder Phase B input in QEI2 mode. Auxiliary timer external gate input in Timer mode.
CNTCMP2(1)	O	—	Yes	Quadrature Encoder Compare Output 2.
COFS	I/O	ST	Yes	Data Converter Interface frame synchronization pin.
CSCK	I/O	ST	Yes	Data Converter Interface serial clock input/output pin.
CSDI	I	ST	Yes	Data Converter Interface serial data input pin.
CSDO	O	—	Yes	Data Converter Interface serial data output pin.
C1RX	I	ST	Yes	ECAN1 bus receive pin.
C1TX	O	—	Yes	ECAN1 bus transmit pin.
C2RX	I	ST	Yes	ECAN2 bus receive pin.
C2TX	O	—	Yes	ECAN2 bus transmit pin.
RTCC	O	—	No	Real-Time Clock alarm output.
CVREF	O	Analog	No	Comparator voltage reference output.
C1IN1+, C1IN2-, C1IN1-, C1IN3-	I	Analog	No	Comparator 1 inputs
C1OUT	O	—	Yes	Comparator 1 output.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

Note 1: This pin is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

2: AVDD must be connected at all times.

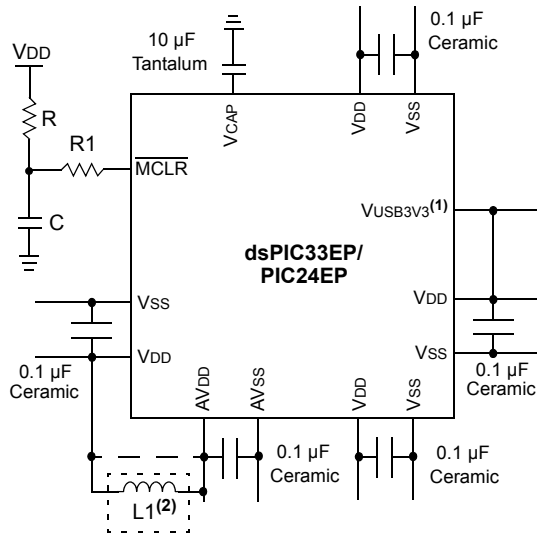
3: These pins are input only on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices.

4: These pins are only available on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices.

5: The availability of I^2C™ interfaces varies by device. Refer to the **"Pin Diagrams"** section for availability. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

6: Analog functionality is activated by enabling the USB module and is not controlled by the ANSEL register.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



Note 1: If the USB module is not used, VUSB3V3 must be connected to VDD, as shown.

2: As an option, instead of a hard-wired connection, an inductor (L1) can be substituted between VDD and AVDD to improve ADC noise rejection. The inductor impedance should be less than 1Ω and the inductor capacity greater than 10 mA.

Where:

$$f = \frac{F_{CNV}}{2}$$ (i.e., ADC conversion rate/2)

$$f = \frac{1}{(2\pi\sqrt{LC})}$$

$$L = \left(\frac{1}{(2\pi f\sqrt{C})}\right)^2$$

2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

2.3 CPU Logic Filter Capacitor Connection (VCAP)

A low-ESR (< 1 Ohms) capacitor is required on the VCAP pin, which is used to stabilize the voltage regulator output voltage. The VCAP pin must not be connected to VDD and must have a capacitor greater than 4.7 µF (10 µF is recommended), 16V connected to ground. The type can be ceramic or tantalum. See **Section 32.0 "Electrical Characteristics"** for additional information.

The placement of this capacitor should be close to the VCAP. It is recommended that the trace length not exceeds one-quarter inch (6 mm). See **Section 29.2 "On-Chip Voltage Regulator"** for details.

2.4 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions:

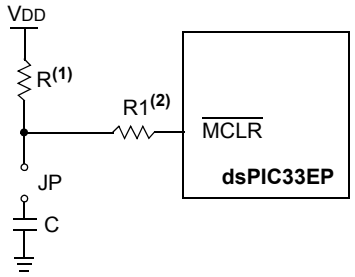
- Device Reset
- Device Programming and Debugging

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-2, it is recommended that the capacitor C, be isolated from the MCLR pin during programming and debugging operations.

Place the components as shown in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



Note 1: R ≤ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the MCLR pin VIH and VIL specifications are met.

2: R1 ≤ 470Ω will limit any current flowing into MCLR from the external capacitor C, in the event of MCLR pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the MCLR pin VIH and VIL specifications are met.

TABLE 4-38: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXMU806 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	—	RP65R<5:0>						—	—	RP64R<5:0>						0000
RPOR1	0682	—	—	RP67R<5:0>						—	—	RP66R<5:0>						0000
RPOR2	0684	—	—	RP69R<5:0>						—	—	RP68R<5:0>						0000
RPOR3	0686	—	—	RP71R<5:0>						—	—	RP70R<5:0>						0000
RPOR4	0688	—	—	RP80R<5:0>						—	—	—	—	—	—	—	—	0000
RPOR5	068A	—	—	RP84R<5:0>						—	—	RP82R<5:0>						0000
RPOR6	068C	—	—	RP87R<5:0>						—	—	RP85R<5:0>						0000
RPOR7	068E	—	—	RP97R<5:0>						—	—	RP96R<5:0>						0000
RPOR8	0690	—	—	RP99R<5:0>						—	—	—	—	—	—	—	—	0000
RPOR9	0692	—	—	RP101R<5:0>						—	—	RP100R<5:0>						0000
RPOR13	069A	—	—	RP118R<5:0>						—	—	—	—	—	—	—	—	0000
RPOR14	069C	—	—	—	—	—	—	—	—	—	—	RP120R<5:0>						0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-39: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXX(GP/MC/MU)806 AND PIC24EPXXXGP806 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	—	RP65R<5:0>						—	—	RP64R<5:0>						0000
RPOR1	0682	—	—	RP67R<5:0>						—	—	RP66R<5:0>						0000
RPOR2	0684	—	—	RP69R<5:0>						—	—	RP68R<5:0>						0000
RPOR3	0686	—	—	RP71R<5:0>						—	—	RP70R<5:0>						0000
RPOR4	0688	—	—	RP80R<5:0>						—	—	—	—	—	—	—	—	0000
RPOR5	068A	—	—	RP84R<5:0>						—	—	RP82R<5:0>						0000
RPOR6	068C	—	—	RP87R<5:0>						—	—	RP85R<5:0>						0000
RPOR7	068E	—	—	RP97R<5:0>						—	—	RP96R<5:0>						0000
RPOR8	0690	—	—	RP99R<5:0>						—	—	RP98R<5:0>						0000
RPOR9	0692	—	—	RP101R<5:0>						—	—	RP100R<5:0>						0000
RPOR10	0694	—	—	—	—	—	—	—	—	—	—	RP102R<5:0>						0000
RPOR13	069A	—	—	RP118R<5:0>						—	—	—	—	—	—	—	—	0000
RPOR14	069C	—	—	—	—	—	—	—	—	—	—	RP120R<5:0>						0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

In addition, DMA transfers can be triggered by timers as well as external interrupts. Each DMA channel is unidirectional. Two DMA channels must be allocated to read and write to a peripheral. If more than one channel receive a request to transfer data, a simple fixed priority scheme, based on channel number, dictates which channel completes the transfer and which channel, or channels, are left pending. Each DMA channel moves a block of data, after which it generates an interrupt to the CPU to indicate that the block is available for processing.

The DMA controller provides these functional capabilities:

- Up to 15 DMA Channels
- Register Indirect With Post-Increment Addressing mode
- Register Indirect Without Post-Increment Addressing mode
- Peripheral Indirect Addressing mode (peripheral generates destination address)
- CPU Interrupt after Half or Full Block Transfer Complete
- Byte or Word Transfers
- Fixed Priority Channel Arbitration
- Manual (software) or Automatic (peripheral DMA requests) Transfer Initiation
- One-Shot or Auto-Repeat Block Transfer modes
- Ping-Pong mode (automatic switch between two DPSRAM start addresses after each block transfer complete)
- DMA Request for Each Channel can be Selected from Any Supported Interrupt Source
- Debug Support Features

The peripherals that can utilize DMA are listed in Table 8-1.

TABLE 8-1: DMA CHANNEL TO PERIPHERAL ASSOCIATIONS

Peripheral to DMA Association	DMAxREQ Register IRQSEL<7:0> Bits	DMAxPAD Register (Values to Read from Peripheral)	DMAxPAD Register (Values to Write to Peripheral)
INT0 – External Interrupt 0	00000000	—	—
IC1 – Input Capture 1	00000001	0x0144 (IC1BUF)	—
IC2 – Input Capture 2	00000101	0x014C (IC2BUF)	—
IC3 – Input Capture 3	00100101	0x0154 (IC3BUF)	—
IC4 – Input Capture 4	00100110	0x015C (IC4BUF)	—
OC1 – Output Compare 1	00000010	—	0x0906 (OC1R) 0x0904 (OC1RS)
OC2 – Output Compare 2	00000110	—	0x0910 (OC2R) 0x090E (OC2RS)
OC3 – Output Compare 3	00011001	—	0x091A (OC3R) 0x0918 (OC3RS)
OC4 – Output Compare 4	00011010	—	0x0924 (OC4R) 0x0922 (OC4RS)
TMR2 – Timer2	00000111	—	—
TMR3 – Timer3	00001000	—	—
TMR4 – Timer4	00011011	—	—
TMR5 – Timer5	00011100	—	—
SPI1 Transfer Done	00001010	0x0248 (SPI1BUF)	0x0248 (SPI1BUF)
SPI2 Transfer Done	00100001	0x0268 (SPI2BUF)	0x0268 (SPI2BUF)
SPI3 Transfer Done	01011011	0x02A8 (SPI3BUF)	0x02A8 (SPI3BUF)
SPI4 Transfer Done	01111011	0x02C8 (SPI4BUF)	0x02C8 (SPI4BUF)
UART1RX – UART1 Receiver	00001011	0x0226 (U1RXREG)	—
UART1TX – UART1 Transmitter	00001100	—	0x0224 (U1TXREG)
UART2RX – UART2 Receiver	00011110	0x0236 (U2RXREG)	—
UART2TX – UART2 Transmitter	00011111	—	0x0234 (U2TXREG)
UART3RX – UART3 Receiver	01010010	0x0256 (U3RXREG)	—
UART3TX – UART3 Transmitter	01010011	—	0x0254 (U3TXREG)

REGISTER 10-2: PMD2: PERIPHERAL MODULE DISABLE CONTROL REGISTER 2 (CONTINUED)

bit 3 **OC4MD:** Output Compare 4 Module Disable bit
1 = Output Compare 4 module is disabled
0 = Output Compare 4 module is enabled

bit 2 **OC3MD:** Output Compare 3 Module Disable bit
1 = Output Compare 3 module is disabled
0 = Output Compare 3 module is enabled

bit 1 **OC2MD:** Output Compare 2 Module Disable bit
1 = Output Compare 2 module is disabled
0 = Output Compare 2 module is enabled

bit 0 **OC1MD:** Output Compare 1 Module Disable bit
1 = Output Compare 1 module is disabled
0 = Output Compare 1 module is enabled

11.7 Peripheral Pin Select Control Registers

REGISTER 11-1: RPINR0: PERIPHERAL PIN SELECT INPUT REGISTER 0

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	INT1R<6:0>						
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **INT1R<6:0>:** Assign External Interrupt 1 (INT1) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 11-47: RPOR3: PERIPHERAL PIN SELECT OUTPUT REGISTER 3

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP71R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP70R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP71R<5:0>:** Peripheral Output Function is Assigned to RP71 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP70R<5:0>:** Peripheral Output Function is Assigned to RP70 Output Pin bits (see Table 11-3 for peripheral function numbers)

REGISTER 11-48: RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP80R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP79R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP80R<5:0>:** Peripheral Output Function is Assigned to RP80 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP79R<5:0>:** Peripheral Output Function is Assigned to RP79 Output Pin bits (see Table 11-3 for peripheral function numbers)

REGISTER 19-1: I2CxCON: I2Cx CONTROL REGISTER (CONTINUED)

bit 6 **STREN:** SCLx Clock Stretch Enable bit (when operating as I^2C slave)
Used in conjunction with the SCLREL bit.
1 = Enables software or receives clock stretching
0 = Disables software or receives clock stretching

bit 5 **ACKDT:** Acknowledge Data bit (when operating as I^2C master, applicable during master receive)
Value that is transmitted when the software initiates an Acknowledge sequence.
1 = Sends NACK during Acknowledge
0 = Sends ACK during Acknowledge

bit 4 **ACKEN:** Acknowledge Sequence Enable bit (when operating as I^2C master, applicable during master receive)
1 = Initiates Acknowledge sequence on SDAx and SCLx pins and transmits the ACKDT data bit. Hardware is clear at the end of a master Acknowledge sequence.
0 = Acknowledge sequence is not in progress

bit 3 **RCEN:** Receive Enable bit (when operating as I^2C master)
1 = Enables Receive mode for I^2C. Hardware is clear at the end of the eighth bit of a master receive data byte.
0 = Receive sequence is not in progress

bit 2 **PEN:** Stop Condition Enable bit (when operating as I^2C master)
1 = Initiates Stop condition on SDAx and SCLx pins. Hardware is clear at the end of a master Stop sequence.
0 = Stop condition is not in progress

bit 1 **RSEN:** Repeated Start Condition Enable bit (when operating as I^2C master)
1 = Initiates Repeated Start condition on SDAx and SCLx pins. Hardware is clear at the end of a master Repeated Start sequence.
0 = Repeated Start condition is not in progress

bit 0 **SEN:** Start Condition Enable bit (when operating as I^2C master)
1 = Initiates Start condition on SDAx and SCLx pins. Hardware is clear at the end of a master Start sequence.
0 = Start condition is not in progress

Note 1: When performing master operations, ensure that the IPMIEN bit is '0'.

REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
- 1 = Address Detect mode is enabled; if 9-bit mode is not selected, this does not take effect
- 0 = Address Detect mode is disabled

bit 4 **RIDLE:** Receiver Idle bit (read-only)
- 1 = Receiver is Idle
- 0 = Receiver is active

bit 3 **PERR:** Parity Error Status bit (read-only)
- 1 = Parity error has been detected for the current character (character at the top of the receive FIFO)
- 0 = Parity error has not been detected

bit 2 **FERR:** Framing Error Status bit (read-only)
- 1 = Framing error has been detected for the current character (character at the top of the receive FIFO)
- 0 = Framing error has not been detected

bit 1 **OERR:** Receive Buffer Overrun Error Status bit (read/clear only)
- 1 = Receive buffer has overflowed
- 0 = Receive buffer has not overflowed; clearing a previously set OERR bit (1 → 0 transition) resets the receiver buffer and the UxRSR to the empty state

bit 0 **URXDA:** Receive Buffer Data Available bit (read-only)
- 1 = Receive buffer has data, at least one more character can be read
- 0 = Receive buffer is empty

Note 1: Refer to **Section 17. "UART"** (DS70582) in the *"dsPIC33E/PIC24E Family Reference Manual"* for information on enabling the UARTx module for transmit operation.

REGISTER 21-8: CxEC: ECANx TRANSMIT/RECEIVE ERROR COUNT REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TERRCNT<7:0>							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
RERRCNT<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **TERRCNT<7:0>:** Transmit Error Count bits

bit 7-0 **RERRCNT<7:0>:** Receive Error Count bits

REGISTER 21-9: CxCFG1: ECANx BAUD RATE CONFIGURATION REGISTER 1

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SJW<1:0>		BRP<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-6 **SJW<1:0>:** Synchronization Jump Width bits

11 = Length is 4 x TQ
10 = Length is 3 x TQ
01 = Length is 2 x TQ
00 = Length is 1 x TQ

bit 5-0 **BRP<5:0>:** Baud Rate Prescaler bits

11 1111 = TQ = 2 x 64 x 1/FCAN
•
•
•
00 0010 = TQ = 2 x 3 x 1/FCAN
00 0001 = TQ = 2 x 2 x 1/FCAN
00 0000 = TQ = 2 x 1 x 1/FCAN

REGISTER 21-15: CxBUFPNT4: ECANx FILTER 12-15 BUFFER POINTER REGISTER 4

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F15BP<3:0>				F14BP<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F13BP<3:0>				F12BP<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **F15BP<3:0>:** RX Buffer Mask for Filter 15 bits

1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F14BP<3:0>:** RX Buffer Mask for Filter 14 bits (same values as bit 15-12)

bit 7-4 **F13BP<3:0>:** RX Buffer Mask for Filter 13 bits (same values as bit 15-12)

bit 3-0 **F12BP<3:0>:** RX Buffer Mask for Filter 12 bits (same values as bit 15-12)

REGISTER 22-6: UxCON: USB CONTROL REGISTER (HOST MODE)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-x, HSC	R-x, HSC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
JSTATE	SE0	TOKBUSY	USBRST	HOSTEN	RESUME	PPBRST	SOFEN
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **JSTATE:** Live Differential Receiver J State Flag bit
1 = J state (differential '0' in low-speed, differential '1' in full-speed) is detected on the USB
0 = No J state is detected

bit 6 **SE0:** Live Single-Ended Zero Flag bit
1 = Single-ended zero is active on the USB bus
0 = No single-ended zero is detected

bit 5 **TOKBUSY:** Token Busy Status bit
1 = Token is being executed by the USB module in On-The-Go state
0 = No token is being executed

bit 4 **USBRST:** USB Reset bit
1 = USB Reset has been generated; for Software Reset, application must set this bit for 50 ms and then clear it
0 = USB Reset is terminated

bit 3 **HOSTEN:** USB Host Mode Enable bit
1 = USB host capability is enabled; pull-downs on D+ and D- are activated in hardware
0 = USB host capability is disabled

bit 2 **RESUME:** USB Resume Signaling Enable bit
1 = Resume signaling is activated; software must set the bit for 10 ms and then clear to enable remote wake-up
0 = Resume signaling is disabled

bit 1 **PPBRST:** Ping-Pong Buffers Reset bit
1 = Resets all Ping-Pong Buffer Pointers to the EVEN buffer descriptor banks
0 = Ping-Pong Buffer Pointers are not reset

bit 0 **SOFEN:** USB Start-of-Frame (SOF) Enable bit
1 = Start-of-Frame token is sent every one 1 ms
0 = Start-of-Frame token is disabled

REGISTER 22-7: UxADDR: USB ADDRESS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LSPDEN(1)	DEVADDR<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **LSPDEN:** USB Low-Speed Enable Indicator bit(1)
1 = USB module operates at low-speed
0 = USB module operates at full-speed

bit 6-0 **DEVADDR<6:0>:** USB Device Address bits

Note 1: Host mode only. In Device mode, this bit is unimplemented.

REGISTER 22-8: UxTOK: USB TOKEN REGISTER (HOST MODE ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PID<3:0>(1)				EP<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-4 **PID<3:0>:** Token Type Identifier bits(1)
1101 = SETUP (TX) token type transaction
1001 = IN (RX) token type transaction
0001 = OUT (TX) token type transaction

bit 3-0 **EP<3:0>:** Token Command Endpoint Address bits
This value must specify a valid endpoint on the attached device.

Note 1: All other combinations are reserved and are not to be used.

REGISTER 22-13: UxOTGIE: USB OTG INTERRUPT ENABLE REGISTER (HOST MODE ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	—	VBUSVDIE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **IDIE:** ID Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 6 **T1MSECIE:** 1 Millisecond Timer Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 5 **LSTATEIE:** Line State Stable Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 4 **ACTVIE:** Bus Activity Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 3 **SESVDIE:** Session Valid Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 2 **SESENDIE:** B-Device Session End Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIE:** A-Device VBUS Valid Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

TABLE 29-2: CONFIGURATION BITS DESCRIPTION (CONTINUED)

Bit Field	Register	RTSP Effect	Description
WINDIS	FWDT	Immediate	Watchdog Timer Window Enable bit 1 = Watchdog Timer is in Non-Window mode 0 = Watchdog Timer is in Window mode
PLLKEN	FWDT	Immediate	PLL Lock Wait Enable bit 1 = Clock switches to the PLL source will wait until the PLL lock signal is valid 0 = Clock switch will not wait for PLL lock
WDTPRE	FWDT	Immediate	Watchdog Timer Prescaler bit 1 = 1:128 0 = 1:32
APLK<1:0>	FAS(2)	Immediate	Auxiliary Segment Key bits These bits must be set to '00' if AWRP = 1 and APL = 1. These bits must be set to '11' for any other value of the AWRP and APL bits. Any mismatch between either the AWRP or APL bits and the APLK bits (as described above), will result in code protection becoming enabled for the Auxiliary Segment. A Flash bulk erase will be required to unlock the device.
APL	FAS(2)	Immediate	Auxiliary Segment Code-Protect bit 1 = Auxiliary program memory is not code-protected 0 = Auxiliary program memory is code-protected
AWRP	FAS(2)	Immediate	Auxiliary Segment Write-Protect bit 1 = Auxiliary program memory is not write-protected 0 = Auxiliary program memory is write-protected
WDTPOST<3:0>	FWDT	Immediate	Watchdog Timer Postscaler bits 1111 = 1:32,768 1110 = 1:16,384 • • • 0001 = 1:2 0000 = 1:1
FPWRT<2:0>	FPOR	Immediate	Power-on Reset Timer Value Select bits 111 = PWRT = 128 ms 110 = PWRT = 64 ms 101 = PWRT = 32 ms 100 = PWRT = 16 ms 011 = PWRT = 8 ms 010 = PWRT = 4 ms 001 = PWRT = 2 ms 000 = PWRT = Disabled
BOREN(1)	FPOR	Immediate	Brown-out Reset (BOR) Detection Enable bit 1 = BOR is enabled 0 = BOR is disabled
ALTI2C2	FPOR	Immediate	Alternate I^2C™ pins for I2C2 bit 1 = I2C2 is mapped to the SDA2/SCL2 pins 0 = I2C2 is mapped to the ASDA2/ASCL2 pins
ALTI2C1	FPOR	Immediate	Alternate I^2C pins for I2C1 bit 1 = I2C1 is mapped to the SDA1/SCL1 pins 0 = I2C1 is mapped to the ASDA1/ASCL1 pins

Note 1: BOR should always be enabled for proper operation (BOREN = 1).

2: This register can only be modified when code protection and write protection are disabled for both the General and Auxiliary Segments (APL = 1, AWRP = 1, APLK = 0, GSS = 1, GWRP = 1 and GSSK = 0).

TABLE 32-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param.	**Typ.(2)**	**Max.**	**Units**	**Conditions**		
Power-Down Current (IPD)(1)						
DC60d	50	100	µA	-40°C	3.3V	Base Power-Down Current(1,4)
DC60a	60	200	µA	+25°C		
DC60b	250	500	µA	+85°C		
DC60c	1600	3000	µA	+125°C		
DC61d	8	10	µA	-40°C	3.3V	Watchdog Timer Current: ΔIWDT(3)
DC61a	10	15	µA	+25°C		
DC61b	12	20	µA	+85°C		
DC61c	13	25	µA	+125°C		

Note 1: IPD (Sleep) current is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC Clock Overshoot/Undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- External Secondary Oscillator (SOSC) is disabled (i.e., SOSCO and SOSCI pins are configured as digital I/O inputs)
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{\text{MCLR}}$ = VDD, WDT and FSCM are disabled, all peripheral modules are disabled (PMDx bits are all ones)
- The VREGS bit (RCON<8>) = 0 (i.e., core regulator is set to stand-by while the device is in Sleep mode)
- RTCC is disabled
- The VREGSF bit (RCON<11>) = 0 (i.e., Flash regulator is set to stand-by while the device is in Sleep mode)
- JTAG is disabled

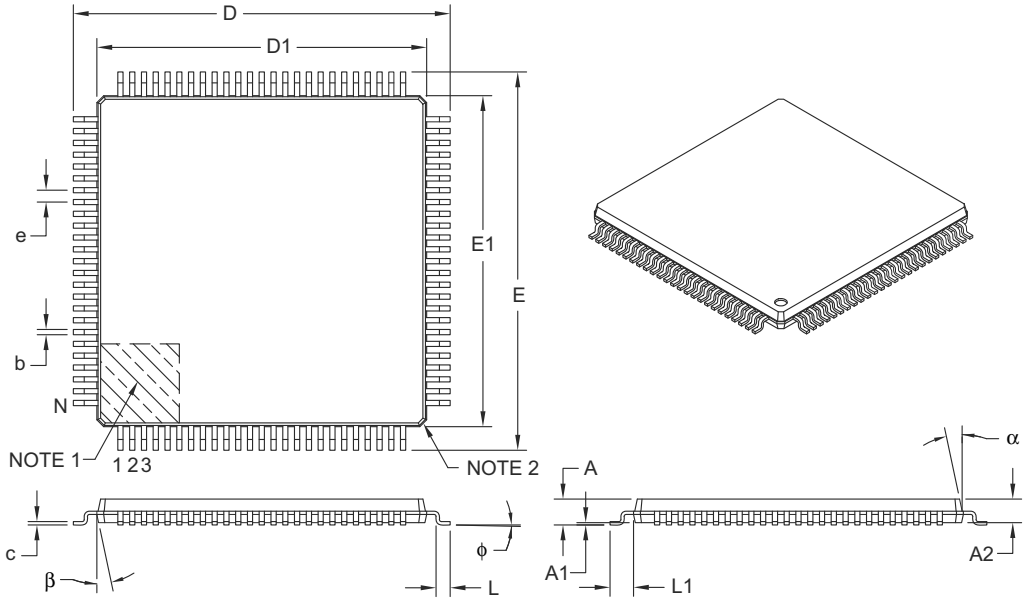
2: Data in the "Typ" column is at 3.3V, +25ºC unless otherwise stated.

3: The Watchdog Timer current is the additional current consumed when the WDT module is enabled. This current should be added to the base IPD current.

4: These currents are measured on the device containing the most memory in this family.

100-Lead Plastic Thin Quad Flatpack (PF) – 14x14x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		100	
Lead Pitch	e		0.50 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		16.00 BSC	
Overall Length	D		16.00 BSC	
Molded Package Width	E1		14.00 BSC	
Molded Package Length	D1		14.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-110B

TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 4.0 "Memory Organization"	Added the Write Latch and Auxiliary Interrupt Vector to the Program Memory Map (see Figure 4-1). Updated the All Resets value for the DSRPAG and DSWPAG registers in the CPU Core Register Maps (see Table 4-1 and Table 4-2). Updated the All Resets value for the INTCON2 register in the Interrupt Controller Register Maps (see Table 4-3 through Table 4-6). Updated the All Resets values for all registers in the Output Compare 1 - Output Compare 16 Register Map, with the exception of the OCxTMR and OCxCON1 registers (see Table 4-9). Removed the DTM bit (TRGCON1<7> from all PWM Generator # Register Maps (see Table 4-11 through Table 4-17). Updated the All Resets value for the QEI1IOC register in the QEI1 Register Map (see Table 4-18). Updated the All Resets value for the QEI2IOC register in the QEI1 Register Map (see Table 4-19). Added Note 4 to the USB OTG Register Map (see Table 4-25) Updated all addresses in the Real-Time Clock and Calendar Register Map (see Table 4-34). Removed RPINR22 from Table 4-37 through Table 4-40. Updated the All Resets values for all registers in the Peripheral Pin Select Input Register Maps and modified the RPIN37-RPINR43 registers (see Table 4-37 through Table 4-40). Added the VREGSF bit (RCON<11>) to the System Control Register Map (see Table 4-43). Added the REFOMD bit (PMD4<3>) to the PMD Register Maps (see Table 4-44 through Table 4-47). Changed the bit range for CNT from <15:0> to <13:0> for all DMAxCNT registers in the DMAC Register Map (see Table 4-49). Updated the All Resets value and removed the ANSC15 and ANSC12 bits in the ANSLEC registers in the PORTC Register Maps (see Table 4-52 and Table 4-53). Updated DSxPAG and Page Description of O, Read and U, Read in Table 4-66. Added Note to the Table 4-67. Updated Arbiter Architecture in Figure 4-8. Updated the Unimplemented value and removed the LATG3 and LATG2 bits in the LATG registers and the CNPUG3 and CNPUG2 bits from the CNPUG registers in the PORTG Register Maps (see Table 4-60 and Table 4-61) Updated the All Resets value and removed the TRISG3 and TRISG2 bits in the TRISG registers and the ODCG3 and ODCG2 bits from the ODCG registers in the PORTG Register Maps (see Table 4-60 and Table 4-61).
Section 5.0 "Flash Program Memory"	Updated the NVMOP<3:0> = 1110 definition to Reserved and added Note 6 to the Nonvolatile Memory (NVM) Control Register (see Register 5-1).
Section 6.0 "Resets"	Added the VREGSF bit (RCON<11>) to the Reset Control Register (see Register 6-1).