Microchip Technology - DSPIC33EP512MU814-E/PH Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, QEI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	122
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TQFP
Supplier Device Package	144-TQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512mu814-e-ph

3.6 CPU Resources

Many useful resources related to the CPU are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310

3.6.1 KEY RESOURCES

- See **Section 16. "CPU"** (DS70359) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

TABLE 4-4: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMU810 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	NVMIF	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	IC8IF	IC7IF	AD2IF	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	T6IF	DMA4IF	PMPIF	OC8IF	OC7IF	OC6IF	OC5IF	IC6IF	IC5IF	IC4IF	IC3IF	DMA3IF	C1IF	C1RXIF	SPI2IF	SPI2EIF	0000
IFS3	0806	—	RTCIF	DMA5IF	DCIIF	DCIEIF	QEI1IF	PSEMIF	C2IF	C2RXIF	INT4IF	INT3IF	T9IF	T8IF	MI2C2IF	SI2C2IF	T7IF	0000
IFS4	0808	—	—	—	—	QEI2IF	—	PSESMIF	—	C2TXIF	C1TXIF	DMA7IF	DMA6IF	CRCIF	U2EIF	U1EIF	—	0000
IFS5	080A	PWM2IF	PWM1IF	IC9IF	OC9IF	SPI3IF	SPI3EIF	U4TXIF	U4RXIF	U4EIF	USB1IF	—	—	U3TXIF	U3RXIF	U3EIF	—	0000
IFS6	080C	—	—	—	—	—	—	—	—	—	—	—	—	PWM6IF	PWM5IF	PWM4IF	PWM3IF	0000
IFS7	080E	IC11IF	OC11IF	IC10IF	OC10IF	SPI4IF	SPI4EIF	DMA11IF	DMA10IF	DMA9IF	DMA8IF	—	—	—	—	—	—	0000
IFS8	0810	—	ICDIF	IC16IF	OC16IF	IC15IF	OC15IF	IC14IF	OC14IF	IC13IF	OC13IF	—	DMA14IF	DMA13IF	DMA12IF	IC12IF	OC12IF	0000
IEC0	0820	NVMIE	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	IC8IE	IC7IE	AD2IE	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	T6IE	DMA4IE	PMPIE	OC8IE	OC7IE	OC6IE	OC5IE	IC6IE	IC5IE	IC4IE	IC3IE	DMA3IE	C1IE	C1RXIE	SPI2IE	SPI2EIE	0000
IEC3	0826	—	RTCIE	DMA5IE	DCIIE	DCIEIE	QEI1IE	PSEMIE	C2IE	C2RXIE	INT4IE	INT3IE	T9IE	T8IE	MI2C2IE	SI2C2IE	T7IE	0000
IEC4	0828	—	—	—	—	QEI2IE	—	PSESMIE	—	C2TXIE	C1TXIE	DMA7IE	DMA6IE	CRCIE	U2EIE	U1EIE	—	0000
IEC5	082A	PWM2IE	PWM1IE	IC9IE	OC9IE	SPI3IE	SPI3EIE	U4TXIE	U4RXIE	U4EIE	USB1IE	—	—	U3TXIE	U3RXIE	U3EIE	—	0000
IEC6	082C	—	—	—	—	—	—	—	—	—	—	—	—	PWM6IE	PWM5IE	PWM4IE	PWM3IE	0000
IEC7	082E	IC11IE	OC11IE	IC10IE	OC10IE	SPI4IE	SPI4EIE	DMA11IE	DMA10IE	DMA9IE	DMA8IE	—	—	—	—	—	—	0000
IEC8	0830	—	ICDIE	IC16IE	OC16IE	IC15IE	OC15IE	IC14IE	OC14IE	IC13IE	OC13IE	—	DMA14IE	DMA13IE	DMA12IE	IC12IE	OC12IE	0000
IPC0	0840	—	T1IP<2:0>			—	OC1IP<2:0>			—	IC1IP<2:0>			—	INT0IP<2:0>			4444
IPC1	0842	—	T2IP<2:0>			—	OC2IP<2:0>			—	IC2IP<2:0>			—	DMA0IP<2:0>			4444
IPC2	0844	—	U1RXIP<2:0>			—	SPI1IP<2:0>			—	SPI1EIP<2:0>			—	T3IP<2:0>			4444
IPC3	0846	—	NVMIP<2:0>			—	DMA1IP<2:0>			—	AD1IP<2:0>			—	U1TXIP<2:0>			4444
IPC4	0848	—	CNIP<2:0>			—	CMIP<2:0>			—	MI2C1IP<2:0>			—	SI2C1IP<2:0>			4444
IPC5	084A	—	IC8IP<2:0>			—	IC7IP<2:0>			—	AD2IP<2:0>			—	INT1IP<2:0>			4444
IPC6	084C	—	T4IP<2:0>			—	OC4IP<2:0>			—	OC3IP<2:0>			—	DMA2IP<2:0>			4444
IPC7	084E	—	U2TXIP<2:0>			—	U2RXIP<2:0>			—	INT2IP<2:0>			—	T5IP<2:0>			4444
IPC8	0850	—	C1IP<2:0>			—	C1RXIP<2:0>			—	SPI2IP<2:0>			—	SPI2EIP<2:0>			4444
IPC9	0852	—	IC5IP<2:0>			—	IC4IP<2:0>			—	IC3IP<2:0>			—	DMA3IP<2:0>			4444
IPC10	0854	—	OC7IP<2:0>			—	OC6IP<2:0>			—	OC5IP<2:0>			—	IC6IP<2:0>			4444
IPC11	0856	—	T6IP<2:0>			—	DMA4IP<2:0>			—	PMPIP<2:0>			—	OC8IP<2:0>			4444
IPC12	0858	—	T8IP<2:0>			—	MI2C2IP<2:0>			—	SI2C2IP<2:0>			—	T7IP<2:0>			4444
IPC13	085A		C2RXIP<2:0>			—	INT4IP<2:0>			—	INT3IP<2:0>			—	T9IP<2:0>			4444
IPC14	085C	—	DCIEIP<2:0>			—	QEI1IP<2:0>			—	PSEMIP<2:0>			—	C2IP<2:0>			4444
IPC15	085E	—	—	—	—	—	RTCIP<2:0>			—	DMA5IP<2:0>			—	DCIIP<2:0>			0444

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-12: PWM REGISTER MAP FOR dsPIC33EPXXX(MC/MU)806/810/814 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PTCON	0C00	PTEN	—	PTSIDL	SESTAT	SEIEN	EIPU	SYNCPOL	SYNCOEN	SYNCEN	SYNCSRC<2:0>			SEVTPS<3:0>				0000
PTCON2	0C02	—	—	—	—	—	—	—	—	—	—	—	—	—	PCLKDIV<2:0>			0000
PTPER	0C04	PTPER<15:0>																FFF8
SEVTCMP	0C06	SEVTCMP<15:0>																0000
MDC	0C0A	MDC<15:0>																0000
STCON	0C0E	—	—	—	SESTAT	SEIEN	EIPU	SYNCPOL	SYNCOEN	SYNCEN	SYNCSRC<2:0>			SEVTPS<3:0>				0000
STCON2	0C10	—	—	—	—	—	—	—	—	—	—	—	—	—	PCLKDIV<2:0>			0000
STPER	0C12	STPER<15:0>																FFF8
SSEVTCMP	0C14	SSEVTCMP<15:0>																0000
CHOP	0C1A	CHPCLKEN	—	—	—	—	—	CHOPCLK<9:0>										0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-13: PWM GENERATOR 1 REGISTER MAP FOR dsPIC33EPXXX(MC/MU)806/810/814 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON1	0C20	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC<1:0>		DTCP	—	MTBS	CAM	XPRES	IUE	0000
IOCON1	0C22	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000
FCLCON1	0C24	IFLTMOD	CLSRC<4:0>					CLPOL	CLMOD	FLTSRC<4:0>					FLTPOL	FLTMOD<1:0>		0000
PDC1	0C26	PDC1<15:0>																0000
PHASE1	0C28	PHASE1<15:0>																0000
DTR1	0C2A	—	—	DTR1<13:0>														0000
ALTDTR1	0C2C	—	—	ALTDTR1<13:0>														0000
SDC1	0C2E	SDC1<15:0>																0000
SPHASE1	0C30	SPHASE1<15:0>																0000
TRIG1	0C32	TRGCMP<15:0>																0000
TRGCON1	0C34	TRGDIV<3:0>				—	—	—	—	—	—	TRGSTRT<5:0>						0000
PWMCAP1	0C38	PWMCAP1<15:0>																0000
LEBCON1	0C3A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000
LEBDLY1	0C3C	—	—	—	—	LEB<11:0>												0000
AUXCON1	0C3E	—	—	—	—	BLANKSEL<3:0>				—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLEN	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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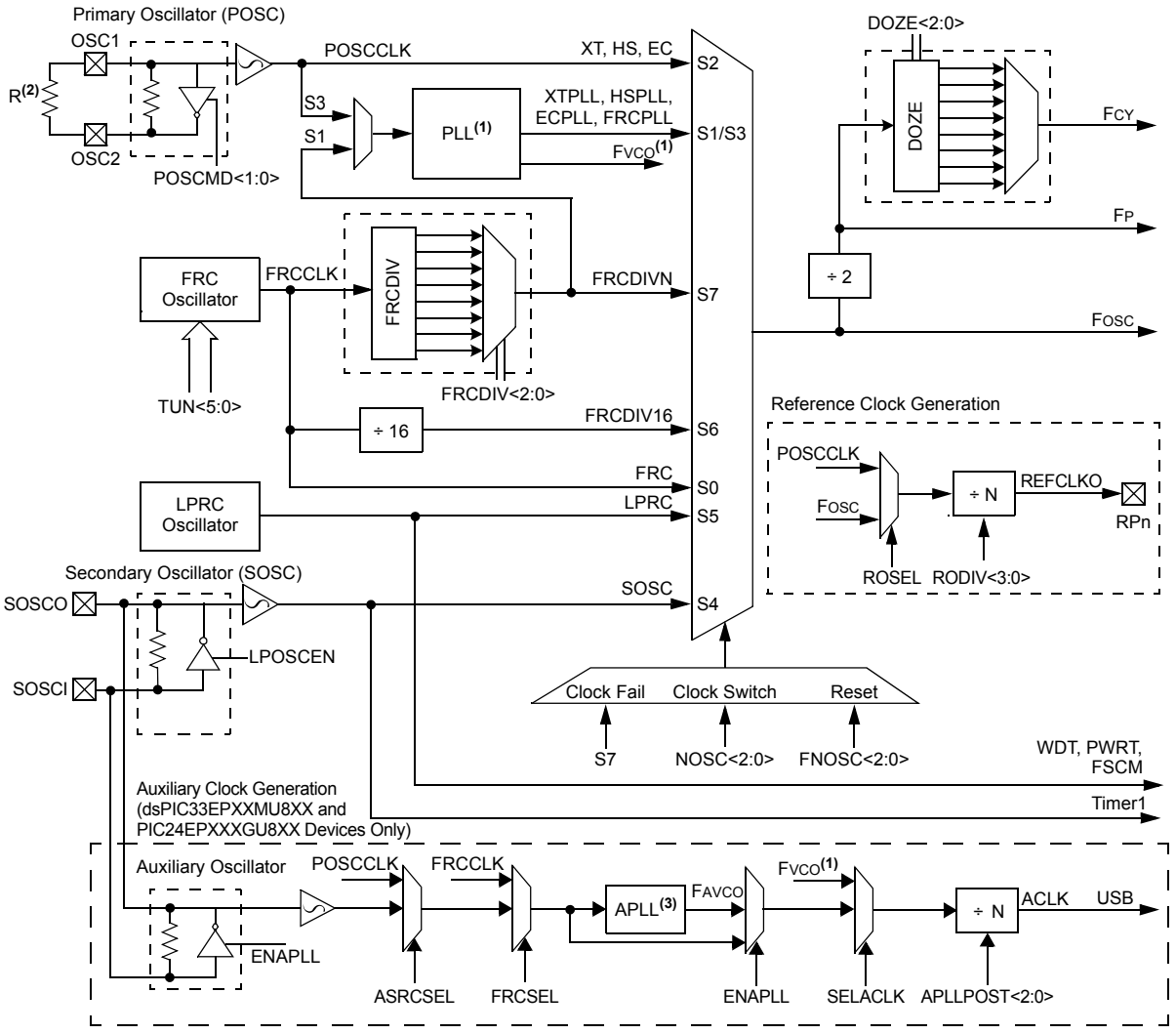
FIGURE 9-1: OSCILLATOR SYSTEM DIAGRAM



Note 1: See Figure 9-2 for PLL and FVCO details.
2: If the oscillator is used with XT or HS modes, an external parallel resistor with the value of 1 MΩ must be connected.
3: See Figure 9-3 for APLL details.

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REGISTER 9-6: ACLKDIV3: AUXILIARY CLOCK DIVISOR REGISTER 3(1,2)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	APLLDIV<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-3 **Unimplemented:** Read as '0'

bit 2-0 **APLLDIV<2:0>:** PLL Feedback Divisor bits (PLL Multiplier Ratio)

111 = 24
110 = 21
101 = 20
100 = 19
011 = 18
010 = 17
001 = 16
000 = 15 (default)

Note 1: This register resets only on a Power-on Reset (POR).

2: This register is only available on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices.

REGISTER 10-5: PMD5: PERIPHERAL MODULE DISABLE CONTROL REGISTER 5 (CONTINUED)

bit 3 **OC12MD:** OC12 Module Disable bit
1 = OC12 module is disabled
0 = OC12 module is enabled

bit 2 **OC11MD:** OC11 Module Disable bit
1 = OC11 module is disabled
0 = OC11 module is enabled

bit 1 **OC10MD:** OC10 Module Disable bit
1 = OC10 module is disabled
0 = OC10 module is enabled

bit 0 **OC9MD:** OC9 Module Disable bit
1 = OC9 module is disabled
0 = OC9 module is enabled

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FIGURE 11-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE

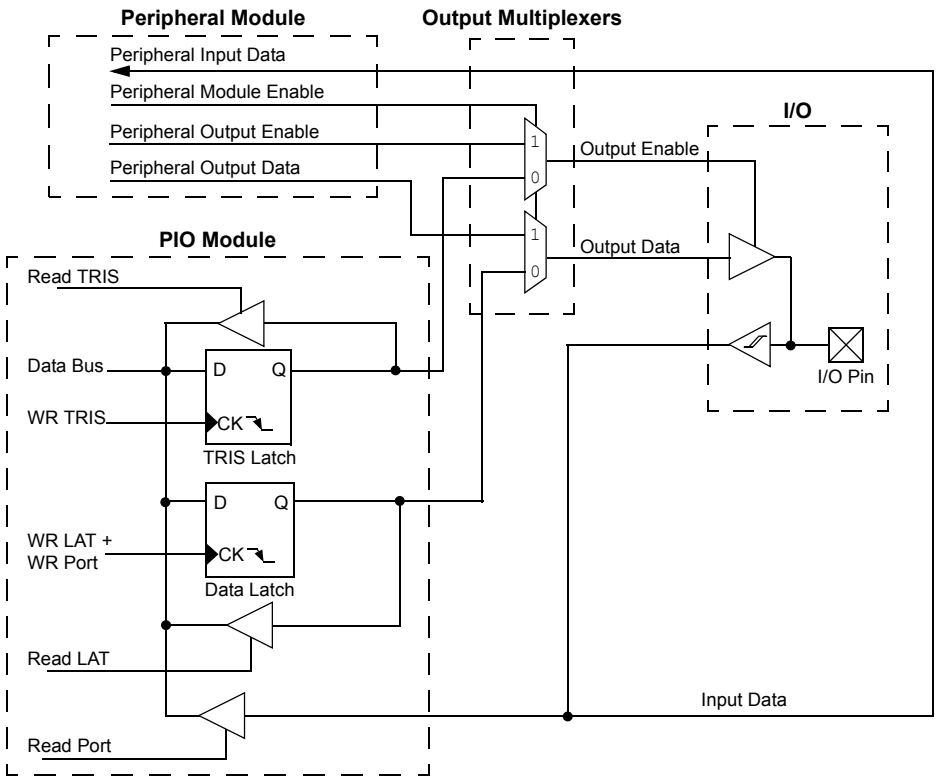

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TABLE 11-1: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION) (CONTINUED)

Input Name(1)	Function Name	Register	Configuration Bits
DCI Data Input	CSDI	RPINR24	CSDIR<6:0>
DCI Clock Input	CSCKIN	RPINR24	CSCKR<6:0>
DCI FSYNC Input	COFSIN	RPINR25	COFSR<6:0>
CAN1 Receive	C1RX	RPINR26	C1RXR<6:0>
CAN2 Receive	C2RX	RPINR26	C2RXR<6:0>
UART3 Receive	U3RX	RPINR27	U3RXR<6:0>
UART3 Clear-to-Send	$\overline{\text{U3CTS}}$	RPINR27	U3CTSR<6:0>
UART4 Receive	U4RX	RPINR28	U4RXR<6:0>
UART4 Clear-to-Send	$\overline{\text{U4CTS}}$	RPINR28	U4CTSR<6:0>
SPI3 Data Input	SDI3	RPINR29	SDI3R<6:0>
SPI3 Clock Input	SCK3	RPINR29	SCK3R<6:0>
SPI3 Slave Select	$\overline{\text{SS3}}$	RPINR30	SS3R<6:0>
SPI4 Data Input	SDI4	RPINR31	SDI4R<6:0>
SPI4 Clock Input	SCK4	RPINR31	SCK4R<6:0>
SPI4 Slave Select	$\overline{\text{SS4}}$	RPINR32	SS4R<6:0>
Input Capture 9	IC9	RPINR33	IC9R<6:0>
Input Capture 10	IC10	RPINR33	IC10R<6:0>
Input Capture 11	IC11	RPINR34	IC11R<6:0>
Input Capture 12	IC12	RPINR34	IC12R<6:0>
Input Capture 13	IC13	RPINR35	IC13R<6:0>
Input Capture 14	IC14	RPINR35	IC14R<6:0>
Input Capture 15	IC15	RPINR36	IC15R<6:0>
Input Capture 16	IC16	RPINR36	IC16R<6:0>
Output Compare Fault C	OCFC	RPINR37	OCFCR<6:0>
PWM Fault 5(2)	FLT5	RPINR42	FLT5R<6:0>
PWM Fault 6(2)	FLT6	RPINR42	FLT6R<6:0>
PWM Fault 7(2)	FLT7	RPINR43	FLT7R<6:0>
PWM Dead-Time Compensation 1(2)	DTCMP1	RPINR38	DTCMP1R<6:0>
PWM Dead-Time Compensation 2(2)	DTCMP2	RPINR39	DTCMP2R<6:0>
PWM Dead-Time Compensation 3(2)	DTCMP3	RPINR39	DTCMP3R<6:0>
PWM Dead-Time Compensation 4(2)	DTCMP4	RPINR40	DTCMP4R<6:0>
PWM Dead-Time Compensation 5(2)	DTCMP5	RPINR40	DTCMP5R<6:0>
PWM Dead-Time Compensation 6(2)	DTCMP6	RPINR41	DTCMP6R<6:0>
PWM Dead-Time Compensation 7(2)	DTCMP7	RPINR41	DTCMP7R<6:0>
PWM Synch Input 1(2)	SYNCI1	RPINR37	SYNCI1R<6:0>
PWM Synch Input 2(2)	SYNCI2	RPINR38	SYNCI2R<6:0>

Note 1: Unless otherwise noted, all inputs use the Schmitt Trigger input buffers.

2: This input source is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

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REGISTER 11-51: RPOR7: PERIPHERAL PIN SELECT OUTPUT REGISTER 7

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP97R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP96R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP97R<5:0>:** Peripheral Output Function is Assigned to RP97 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP96R<5:0>:** Peripheral Output Function is Assigned to RP96 Output Pin bits (see Table 11-3 for peripheral function numbers)

REGISTER 11-52: RPOR8: PERIPHERAL PIN SELECT OUTPUT REGISTER 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP99R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP98R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP99R<5:0>:** Peripheral Output Function is Assigned to RP99 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP98R<5:0>:** Peripheral Output Function is Assigned to RP98 Output Pin bits (see Table 11-3 for peripheral function numbers)

REGISTER 15-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2 (CONTINUED)

bit 4-0 **SYNCSEL<4:0>:** Trigger/Synchronization Source Selection bits

11111 = No Sync or Trigger source for OCx
11110 = INT2 pin synchronizes or triggers OCx
11101 = INT1 pin synchronizes or triggers OCx
11100 = Reserved
11011 = ADC1 module synchronizes or triggers OCx
11010 = CMP3 module synchronizes or triggers OCx
11001 = CMP2 module synchronizes or triggers OCx
11000 = CMP1 module synchronizes or triggers OCx
10111 = IC8 module synchronizes or triggers OCx
10110 = IC7 module synchronizes or triggers OCx
10101 = IC6 module synchronizes or triggers OCx
10100 = IC5 module synchronizes or triggers OCx
10011 = IC4 module synchronizes or triggers OCx
10010 = IC3 module synchronizes or triggers OCx
10001 = IC2 module synchronizes or triggers OCx
10000 = IC1 module synchronizes or triggers OCx
01111 = Timer5 synchronizes or triggers OCx
01110 = Timer4 synchronizes or triggers OCx
01101 = Timer3 synchronizes or triggers OCx
01100 = Timer2 synchronizes or triggers OCx (default)
01011 = Timer1 synchronizes or triggers OCx
01010 = No Sync or Trigger source for OCx
01001 = OC9 module synchronizes or triggers OCx(1,2)
01000 = OC8 module synchronizes or triggers OCx(1,2)
00111 = OC7 module synchronizes or triggers OCx(1,2)
00110 = OC6 module synchronizes or triggers OCx(1,2)
00101 = OC5 module synchronizes or triggers OCx(1,2)
00100 = OC4 module synchronizes or triggers OCx(1,2)
00011 = OC3 module synchronizes or triggers OCx(1,2)
00010 = OC2 module synchronizes or triggers OCx(1,2)
00001 = OC1 module synchronizes or triggers OCx(1,2)
00000 = No Sync or Trigger source for OCx

Note 1: Do not use the OCx module as its own Sync or Trigger source.

2: When the OCy module is turned OFF, it sends a trigger out signal. If the OCx module uses the OCy module as a Trigger source, the OCy module must be unselected as a Trigger source prior to disabling it.

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REGISTER 16-14: PHASEx: PWMx PRIMARY PHASE SHIFT REGISTER(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PHASEx<15:0>:** PWM Phase Shift Value or Independent Time Base Period for the PWM Generator bits

Note 1: If ITB (PWMCONx<9>) = 0, the following applies based on the mode of operation:
- Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCON<11:10>) = 00, 01 or 10), PHASEx<15:0> = Phase shift value for PWMxH and PWMxL outputs.
- True Independent Output mode (PMOD<1:0> (IOCONx<11:10>) = 11), PHASEx<15:0> = Phase shift value for PWMxH only.

2: If ITB (PWMCONx<9>) = 1, the following applies based on the mode of operation:
- Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10), PHASEx<15:0> = Independent time base period value for PWMxH and PWMxL.
- True Independent Output mode (PMOD<1:0> (IOCONx<11:10>) = 11), PHASEx<15:0> = Independent time base period value for PWMxH only.

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REGISTER 17-1: QEIxCON: QEIx CONTROL REGISTER (CONTINUED)

bit 6-4 **INTDIV<2:0>:** Timer Input Clock Prescale Select bits (interval timer, main timer (position counter), velocity counter and index counter internal clock divider select)(3)
111 = 1:128 prescale value
110 = 1:64 prescale value
101 = 1:32 prescale value
100 = 1:16 prescale value
011 = 1:8 prescale value
010 = 1:4 prescale value
001 = 1:2 prescale value
000 = 1:1 prescale value

bit 3 **CNTPOL:** Position and Index Counter/Timer Direction Select bit
1 = Counter direction is negative unless modified by external up/down signal
0 = Counter direction is positive unless modified by external up/down signal

bit 2 **GATEN:** External Count Gate Enable bit
1 = External gate signal controls position counter operation
0 = External gate signal does not affect position counter/timer operation

bit 1-0 **CCM<1:0>:** Counter Control Mode Selection bits
11 = Internal Timer mode with optional external count is selected
10 = External clock count with optional external count is selected
01 = External clock count with external up/down direction is selected
00 = Quadrature Encoder Interface (x4 mode) Count mode is selected

Note 1: When CCM = 10 or CCM = 11, all of the QEI counters operate as timers and the PIMOD<2:0> bits are ignored.

2: When CCM = 00, and QEA and QEB values match Index Match Value (IMV), the POSCNTH and POSCNTL registers are reset.

3: The selected clock rate should be at least twice the expected maximum quadrature count rate.

REGISTER 23-3: AD2CON2: ADC2 CONTROL REGISTER 2 (CONTINUED)

bit 1 **BUFM:** Buffer Fill Mode Select bit

1 = Starts buffer filling the first half of the buffer on the first interrupt and the second half of the buffer on the next interrupt

0 = Always starts filling the buffer from the Start address

bit 0 **ALTS:** Alternate Input Sample Mode Select bit

1 = Uses channel input selects for Sample A on first sample and Sample B on next sample

0 = Always uses channel input selects for Sample A

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REGISTER 26-8: ALRMVAL (WHEN ALRMPTR<1:0> = 10): ALARM MONTH AND DAY VALUE REGISTER(1)

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	MTHTEN0	MTHONE<3:0>			
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	DAYTEN<1:0>		DAYONE<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **MTHTEN0:** Binary Coded Decimal Value of Month's Tens Digit bit
Contains a value of 0 or 1.

bit 11-8 **MTHONE<3:0>:** Binary Coded Decimal Value of Month's Ones Digit bits
Contains a value from 0 to 9.

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DAYTEN<1:0>:** Binary Coded Decimal Value of Day's Tens Digit bits
Contains a value from 0 to 3.

bit 3-0 **DAYONE<3:0>:** Binary Coded Decimal Value of Day's Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

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31.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers and dsPIC® digital signal controllers are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB C Compiler for Various Device Families
  - HI-TECH C® for Various Device Families
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers
  - MPLAB ICD 3
  - PICkit™ 3 Debug Express
- Device Programmers
  - PICkit™ 2 Programmer
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits

31.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16/32-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
  - Simulator
  - Programmer (sold separately)
  - In-Circuit Emulator (sold separately)
  - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either C or assembly)
- One-touch compile or assemble, and download to emulator and simulator tools (automatically updates all project information)
- Debug using:
  - Source files (C or assembly)
  - Mixed C and assembly
  - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

TABLE 32-47: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	TscP	Maximum SCKx Input Frequency	—	—	15	MHz	See **Note 3**
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See **Note 4**
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See **Note 4**
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See **Note 4**
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↑ or SCKx ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output, High-Impedance	10	—	50	ns	See **Note 4**
SP52	TscH2ssH, TscL2ssH	$\overline{SSx}$ ↑ after SCKx Edge	1.5 TCY + 40	—	—	ns	See **Note 4**

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCKx is 66.7 ns. Therefore, the SCKx clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

TABLE 32-59: DCI MODULE (MULTI-CHANNEL, I²S MODES) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
CS10	TCSCKL	CSCK Input Low Time (CSCK pin is an input)	TCY/2 + 20	—	—	ns	
		CSCK Output Low Time(3) (CSCK pin is an output)	30	—	—	ns	
CS11	TCSCKH	CSCK Input High Time (CSCK pin is an input)	TCY/2 + 20	—	—	ns	
		CSCK Output High Time(3) (CSCK pin is an output)	30	—	—	ns	
CS20	TCSCKF	CSCK Output Fall Time (CSCK pin is an output)	—	—	—	ns	See Parameter DO32
CS21	TCSCKR	CSCK Output Rise Time (CSCK pin is an output)	—	—	—	ns	See Parameter DO31
CS30	TCSDOF	CSDO Data Output Fall Time	—	—	—	ns	See Parameter DO32
CS31	TCSDOR	CSDO Data Output Rise Time	—	—	—	ns	See Parameter DO31
CS35	TDV	Clock Edge to CSDO Data Valid	—	—	10	ns	
CS36	TDIV	Clock Edge to CSDO Tri-Stated	10	—	20	ns	
CS40	TCSDI	Setup Time of CSDI Data Input to CSCK Edge (CSCK pin is input or output)	20	—	—	ns	
CS41	THCSDI	Hold Time of CSDI Data Input to CSCK Edge (CSCK pin is input or output)	20	—	—	ns	
CS50	TCOFSF	COFS Fall Time (COFS pin is output)	—	—	—	ns	See Parameter DO32
CS51	TCOFSR	COFS Rise Time (COFS pin is output)	—	—	—	ns	See Parameter DO31
CS55	TSCOFS	Setup Time of COFS Data Input to CSCK Edge (COFS pin is input)	20	—	—	ns	
CS56	THCOFS	Hold Time of COFS Data Input to CSCK Edge (COFS pin is input)	20	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for CSCK is 100 ns. Therefore, the clock generated in Master mode must not violate this specification.

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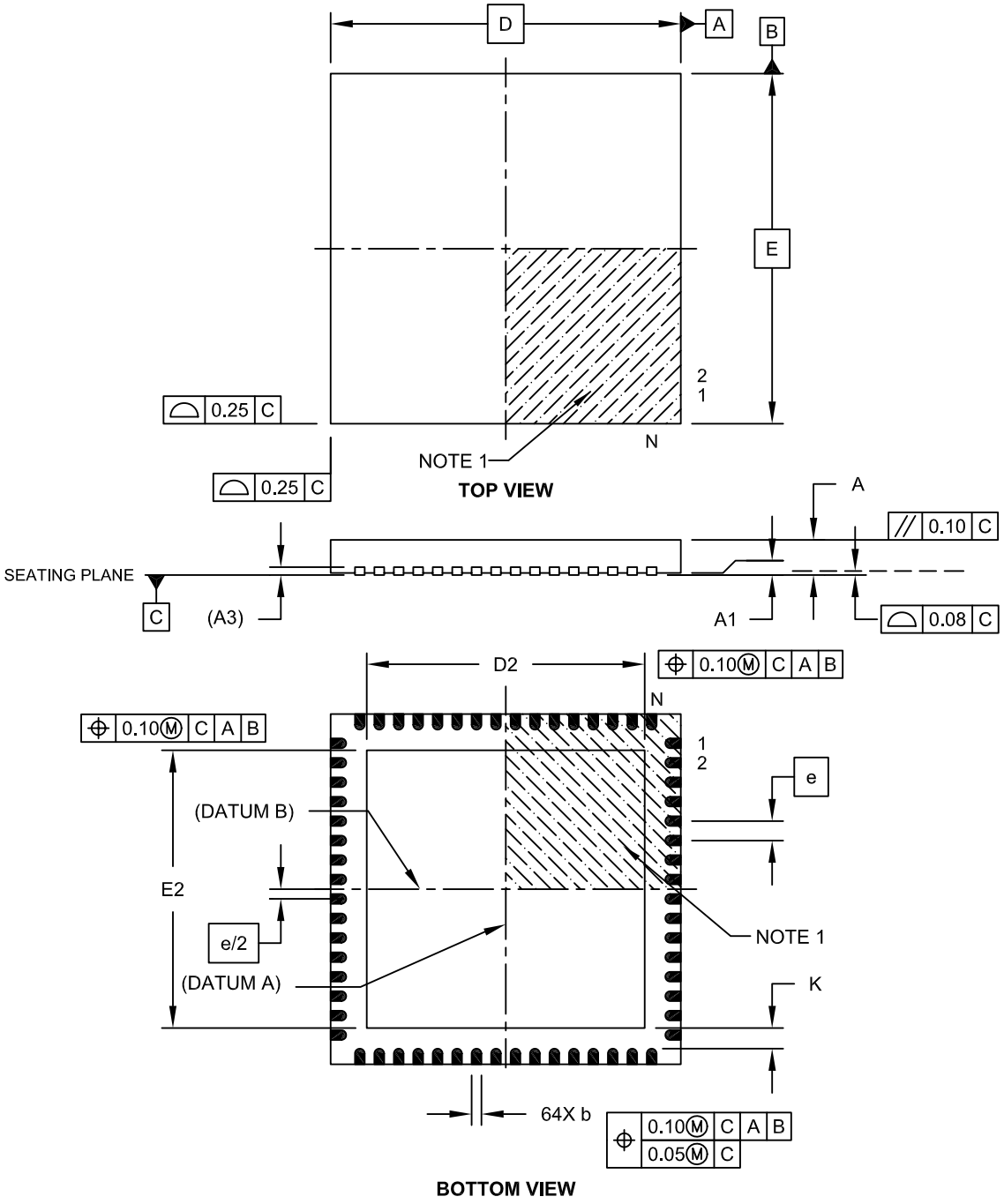
34.2 Package Details

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] With 7.15 x 7.15 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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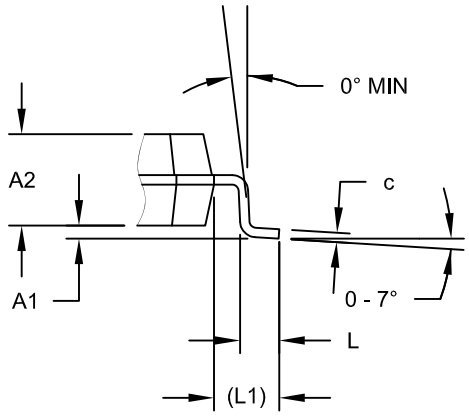
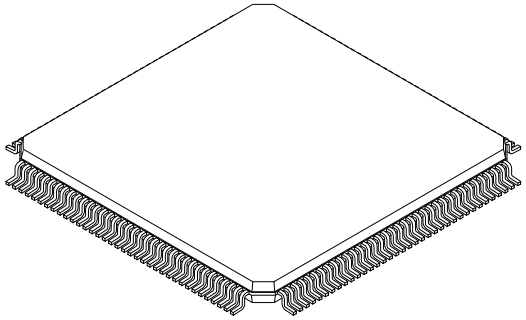
144-Lead Plastic Low Profile Quad Flatpack (PL) – 20x20x1.40 mm Body, with 2.00 mm Footprint [LQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL A



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		144	
Lead Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.60
Molded Package Height	A2	1.35	1.40	1.45
Standoff	A1	0.05	-	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 (REF)	
Overall Width	E		22.00 BSC	
Overall Length	D		22.00 BSC	
Molded Body Width	E1		20.00 BSC	
Molded Body Length	D1		20.00 BSC	
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.17	0.22	0.27

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-044B Sheet 2 of 2

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NOTES:

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