Microchip Technology - DSPIC33EP512MU814-E/PL Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, QEI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	122
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512mu814-e-pl

4.2.5 X AND Y DATA SPACES

The dsPIC33EPXXX(GP/MC/MU)806/810/814 core has two data spaces, X and Y. These data spaces can be considered either separate (for some DSP instructions), or as one unified linear address range (for MCU instructions). The data spaces are accessed using two Address Generation Units (AGUs) and separate data paths. This feature allows certain instructions to concurrently fetch two words from RAM, thereby enabling efficient execution of DSP algorithms such as Finite Impulse Response (FIR) filtering and Fast Fourier Transform (FFT).

The PIC24EPXXX(GP/GU)806/810/814 devices do not have a Y data space and a Y AGU. For these devices, the entire data space is treated as X data space.

The X data space is used by all instructions and supports all addressing modes. X data space has separate read and write data buses. The X read data bus is the read data path for all instructions that view data space as combined X and Y address space. It is also the X data prefetch path for the dual operand DSP instructions (`MAC` class).

The Y data space is used in concert with the X data space by the `MAC` class of instructions (`CLR`, `ED`, `EDAC`, `MAC`, `MOVSAC`, `MPY`, `MPY.N` and `MSC`) to provide two concurrent data read paths.

Both the X and Y data spaces support Modulo Addressing mode for all instructions, subject to addressing mode restrictions. Bit-Reversed Addressing mode is only supported for writes to X data space. Modulo Addressing and Bit-Reversed Addressing are not present in PIC24EPXXX(GP/GU)806/810/814 devices.

All data memory writes, including in DSP instructions, view data space as combined X and Y address space. The boundary between the X and Y data spaces is device-dependent and is not user-programmable.

4.2.6 DMA RAM

Each dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 device contains 4 Kbytes of dual ported DMA RAM located at the end of Y data RAM and is part of Y data space. Memory locations in the DMA RAM space are accessible simultaneously by the CPU and the DMA Controller module. DMA RAM is utilized by the DMA controller to store data to be transferred to various peripherals using DMA, as well as data transferred from various peripherals using DMA. The DMA RAM can be accessed by the DMA controller without having to steal cycles from the CPU.

When the CPU and the DMA controller attempt to concurrently write to the same DMA RAM location, the hardware ensures that the CPU is given precedence in accessing the DMA RAM location. Therefore, the DMA RAM provides a reliable means of transferring DMA data without ever having to stall the CPU.

Note 1: DMA RAM can be used for general purpose data storage if the DMA function is not required in an application.

2: On PIC24EPXXX(GP/GU)806/810/814 devices, DMA RAM is located at the end of X data RAM and is part of X data space.

4.3 Program Memory Resources

Many useful resources related to the Program Memory are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310

4.3.1 KEY RESOURCES

- **Section 4. "Program Memory"** (DS70612) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

4.4 Special Function Register Maps

Table 4-1 through Table 4-72 provide mapping tables for all Special Function Registers (SFRs).

TABLE 4-10: INPUT CAPTURE 1 THROUGH INPUT CAPTURE 16 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IC1CON1	0140	—	—	ICSIDL	ICTSEL<2:0>			—	—	—	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
IC1CON2	0142	—	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL<4:0>					000D
IC1BUF	0144	Input Capture 1 Buffer Register																xxxx
IC1TMR	0146	Input Capture 1 Timer																0000
IC2CON1	0148	—	—	ICSIDL	ICTSEL<2:0>			—	—	—	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
IC2CON2	014A	—	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL<4:0>					000D
IC2BUF	014C	Input Capture 2 Buffer Register																xxxx
IC2TMR	014E	Input Capture 2 Timer																0000
IC3CON1	0150	—	—	ICSIDL	ICTSEL<2:0>			—	—	—	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
IC3CON2	0152	—	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL<4:0>					000D
IC3BUF	0154	Input Capture 3 Buffer Register																xxxx
IC3TMR	0156	Input Capture 3 Timer																0000
IC4CON1	0158	—	—	ICSIDL	ICTSEL<2:0>			—	—	—	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
IC4CON2	015A	—	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL<4:0>					000D
IC4BUF	015C	Input Capture 4 Buffer Register																xxxx
IC4TMR	015E	Input Capture 4 Timer																0000
IC5CON1	0160	—	—	ICSIDL	ICTSEL<2:0>			—	—	—	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
IC5CON2	0162	—	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL<4:0>					000D
IC5BUF	0164	Input Capture 5 Buffer Register																xxxx
IC5TMR	0166	Input Capture 5 Timer																0000
IC6CON1	0168	—	—	ICSIDL	ICTSEL<2:0>			—	—	—	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
IC6CON2	016A	—	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL<4:0>					000D
IC6BUF	016C	Input Capture 6 Buffer Register																xxxx
IC6TMR	016E	Input Capture 6 Timer																0000
IC7CON1	0170	—	—	ICSIDL	ICTSEL<2:0>			—	—	—	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
IC7CON2	0172	—	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL<4:0>					000D
IC7BUF	0174	Input Capture 7 Buffer Register																xxxx
IC7TMR	0176	Input Capture 7 Timer																0000
IC8CON1	0178	—	—	ICSIDL	ICTSEL<2:0>			—	—	—	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
IC8CON2	017A	—	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL<4:0>					000D
IC8BUF	017C	Input Capture 8 Buffer Register																xxxx
IC8TMR	017E	Input Capture 8 Timer																0000

TABLE 4-33: ECAN2 REGISTER MAP WHEN WIN (C2CTRL<0>) = 1 (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C2RXF11EID	056E	EID<15:8>								EID<7:0>								xxxx
C2RXF12SID	0570	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C2RXF12EID	0572	EID<15:8>								EID<7:0>								xxxx
C2RXF13SID	0574	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C2RXF13EID	0576	EID<15:8>								EID<7:0>								xxxx
C2RXF14SID	0578	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C2RXF14EID	057A	EID<15:8>								EID<7:0>								xxxx
C2RXF15SID	057C	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C2RXF15EID	057E	EID<15:8>								EID<7:0>								xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-53: COMPARATOR REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMSTAT	0A80	CMSIDL	—	—	—	—	C3EVT	C2EVT	C1EVT	—	—	—	—	—	C3OUT	C2OUT	C1OUT	0000
CVRCON	0A82	—	—	—	—	—	VREFSEL	BGSEL<1:0>		CVREN	CVROE	CVRR	CVRSS	CVR<3:0>				0000
CM1CON	0A84	CON	COE	CPOL	—	—	—	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
CM1MSKSRC	0A86	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
CM1MSKCON	0A88	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM1FLTR	0A8A	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000
CM2CON	0A8C	CON	COE	CPOL	—	—	—	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
CM2MSKSRC	0A8E	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
CM2MSKCON	0A90	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM2FLTR	0A92	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000
CM3CON	0A94	CON	COE	CPOL	—	—	—	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
CM3MSKSRC	0A96	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
CM3MSKCON	0A98	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM3FLTR	0A9A	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.4.3 EDS ARBITRATION AND BUS MASTER PRIORITY

EDS accesses from bus masters in the system are arbitrated.

The arbiter for data memory (including EDS) arbitrates between the CPU, the DMA, the USB module and the ICD module. In the event of coincidental access to a bus by the bus masters, the arbiter determines which bus master access has the highest priority. The other bus masters are suspended and processed after the access of the bus by the bus master with the highest priority.

By default, the CPU is Bus Master 0 (M0) with the highest priority and the ICD is Bus Master 4 (M4) with the lowest priority. The remaining bus masters (USB and DMA Controllers) are allocated to M2 and M3, respectively (M1 is reserved and cannot be used). The user application may raise or lower the priority of the masters to be above that of the CPU by setting the appropriate bits in the EDS Bus Master Priority Control (MSTRPR) register. All bus masters with raised priorities will maintain the same priority relationship relative to each other (i.e., M1 being highest and M3 being lowest, with M2 in between). Also, all the bus masters with priorities below that of the CPU maintain the same priority relationship relative to each other. The priority schemes for bus masters with different MSTRPR values are tabulated in Table 4-74.

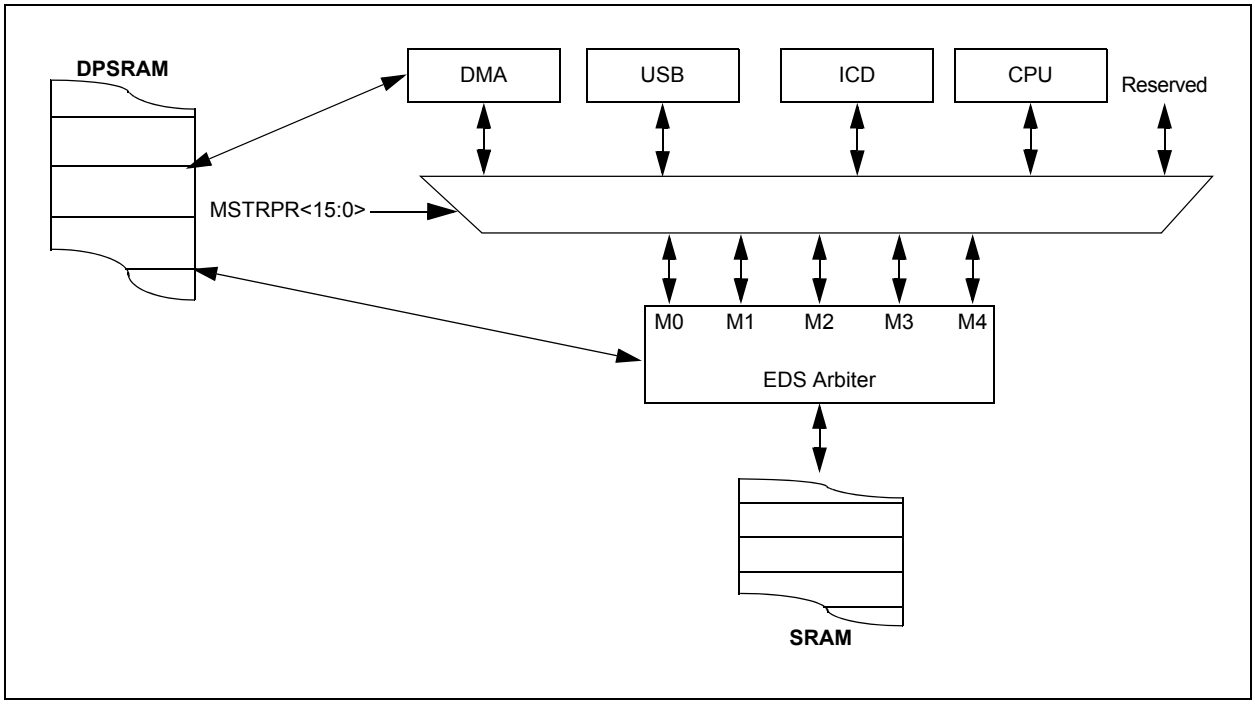
This bus master priority control allows the user application to manipulate the real-time response of the system, either statically during initialization, or dynamically in response to real-time events.

TABLE 4-74: EDS BUS ARBITER PRIORITY

Priority	MSTRPR<15:0> Bit Setting(1)			
	0x0000	0x0008	0x0020	0x0028
M0 (highest)	CPU	USB	DMA	USB
M1	Reserved	CPU	CPU	DMA
M2	USB	Reserved	Reserved	CPU
M3	DMA	DMA	USB	Reserved
M4 (lowest)	ICD	ICD	ICD	ICD

Note 1: All other values of MSTRPR<15:0> are reserved.

FIGURE 4-8: EDS ARBITER ARCHITECTURE



7.0 INTERRUPT CONTROLLER

Note 1: This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 6. "Interrupts"** (DS70600) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 CPU.

The interrupt controller has the following features:

- Up to eight processor exceptions and software traps
- Eight user-selectable priority levels
- Interrupt Vector Table (IVT) with a unique vector for each interrupt or exception source
- Fixed priority within a specified user priority level
- Fixed interrupt entry and return latencies

7.1 Interrupt Vector Table

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 Interrupt Vector Table (IVT), shown in Figure 7-1, resides in the General Segment of program memory, starting at location, 0x000004, and is used when executing code from the General Segment. The IVT contains seven non-maskable trap vectors and up to 114 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with vector 0 takes priority over interrupts at any other vector address.

Note: Any unimplemented or unused vector locations in the IVT should be programmed with the address of a default interrupt handler routine that contains a `RESET` instruction.

7.2 Auxiliary Interrupt Vector

When code is being executed in the Auxiliary Segment, a special single interrupt vector, located at address, 0x7FFFFA, is used for all interrupt sources and traps. Once vectored to this single routine, the VECNUM<7:0> bits (INTTREG<7:0>, Register 7-7) can be examined to determine the source of the interrupt or trap so that it can be properly processed.

7.3 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices clear their registers in response to a Reset, which forces the PC to zero. The digital signal controller then begins program execution at location, 0x000000. A `GOTO` instruction at the Reset address can redirect program execution to the appropriate start-up routine.

Note: Reset locations are also located in the Auxiliary Segment at the addresses 0x7FFFFC and 0x7FFFFE. The Reset Target Vector Select bit, RSTPRI (FICD<2>) controls whether the primary (General Segment) or Auxiliary Segment Reset location is used.

REGISTER 7-2: CORCON: CORE CONTROL REGISTER(1)

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
VAR	—	US<1:0>		EDT	DL<2:0>		
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R-0	R/W-0	R/W-0
SATA	SATB	SATDW	ACCSAT	**IPL3(2)**	SFA	RND	IF
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **VAR:** Variable Exception Processing Latency Control bit
1 = Variable exception processing is enabled
0 = Fixed exception processing is enabled

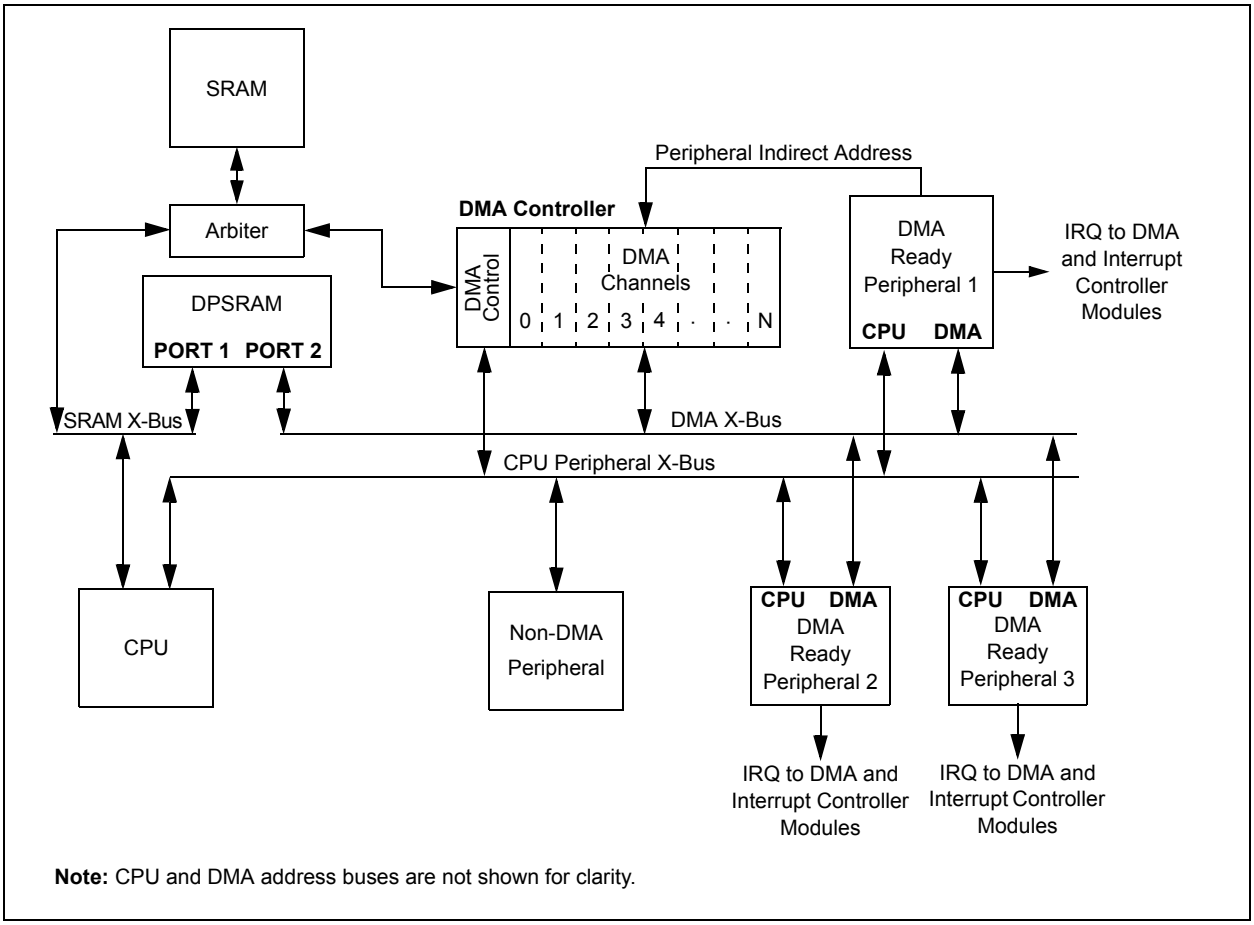
bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3(2)
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

Note 1: For complete register details, see **Register 3-2: "CORCON: Core Control Register"**.
2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

TABLE 8-1: DMA CHANNEL TO PERIPHERAL ASSOCIATIONS (CONTINUED)

Peripheral to DMA Association	DMAxREQ Register IRQSEL<7:0> Bits	DMAxPAD Register (Values to Read from Peripheral)	DMAxPAD Register (Values to Write to Peripheral)
UART4RX – UART4 Receiver	01011000	0x02B6 (U4RXREG)	—
UART4TX – UART4 Transmitter	01011001	—	0x02B4 (U4TXREG)
ECAN1 – RX Data Ready	00100010	0x0440 (C1RXD)	—
ECAN1 – TX Data Request	01000110	—	0x0442 (C1TXD)
ECAN2 – RX Data Ready	00110111	0x0540 (C2RXD)	—
ECAN2 – TX Data Request	01000111	—	0x0542 (C2TXD)
DCI – DCI Transfer Done	00111100	0x0290 (RXBUF0)	0x0298 (TXBUF0)
ADC1 – ADC1 Convert Done	00001101	0x0300 (ADC1BUF0)	—
ADC2 – ADC2 Convert Done	00010101	0x0340 (ADC2BUF0)	—
PMP – PMP Data Move	00101101	0x0608 (PMDIN1)	0x0608 (PMDIN1)

FIGURE 8-2: DMA CONTROLLER TO PERIPHERAL ASSOCIATIONS BLOCK DIAGRAM



Note: CPU and DMA address buses are not shown for clarity.

REGISTER 8-12: DMARQC: DMA REQUEST COLLISION STATUS REGISTER

U-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
—	RQCOL14	RQCOL13	RQCOL12	RQCOL11	RQCOL10	RQCOL9	RQCOL8
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
RQCOL7	RQCOL6	RQCOL5	RQCOL4	RQCOL3	RQCOL2	RQCOL1	RQCOL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **RQCOL14:** Channel 14 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 13 **RQCOL13:** Channel 13 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 12 **RQCOL12:** Channel 12 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 11 **RQCOL11:** Channel 11 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 10 **RQCOL10:** Channel 10 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 9 **RQCOL9:** Channel 9 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 8 **RQCOL8:** Channel 8 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 7 **RQCOL7:** Channel 7 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 6 **RQCOL6:** Channel 6 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 5 **RQCOL5:** Channel 5 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 4 **RQCOL4:** Channel 4 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 3 **RQCOL3:** Channel 3 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

REGISTER 10-2: PMD2: PERIPHERAL MODULE DISABLE CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IC8MD	IC7MD	IC6MD	IC5MD	IC4MD	IC3MD	IC2MD	IC1MD
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OC8MD	OC7MD	OC6MD	OC5MD	OC4MD	OC3MD	OC2MD	OC1MD
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **IC8MD:** Input Capture 8 Module Disable bit
1 = Input Capture 8 module is disabled
0 = Input Capture 8 module is enabled

bit 14 **IC7MD:** Input Capture 2 Module Disable bit
1 = Input Capture 7 module is disabled
0 = Input Capture 7 module is enabled

bit 13 **IC6MD:** Input Capture 6 Module Disable bit
1 = Input Capture 6 module is disabled
0 = Input Capture 6 module is enabled

bit 12 **IC5MD:** Input Capture 5 Module Disable bit
1 = Input Capture 5 module is disabled
0 = Input Capture 5 module is enabled

bit 11 **IC4MD:** Input Capture 4 Module Disable bit
1 = Input Capture 4 module is disabled
0 = Input Capture 4 module is enabled

bit 10 **IC3MD:** Input Capture 3 Module Disable bit
1 = Input Capture 3 module is disabled
0 = Input Capture 3 module is enabled

bit 9 **IC2MD:** Input Capture 2 Module Disable bit
1 = Input Capture 2 module is disabled
0 = Input Capture 2 module is enabled

bit 8 **IC1MD:** Input Capture 1 Module Disable bit
1 = Input Capture 1 module is disabled
0 = Input Capture 1 module is enabled

bit 7 **OC8MD:** Output Compare 8 Module Disable bit
1 = Output Compare 8 module is disabled
0 = Output Compare 8 module is enabled

bit 6 **OC7MD:** Output Compare 7 Module Disable bit
1 = Output Compare 7 module is disabled
0 = Output Compare 7 module is enabled

bit 5 **OC6MD:** Output Compare 6 Module Disable bit
1 = Output Compare 6 module is disabled
0 = Output Compare 6 module is enabled

bit 4 **OC5MD:** Output Compare 5 Module Disable bit
1 = Output Compare 5 module is disabled
0 = Output Compare 5 module is enabled

REGISTER 11-4: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	T3CKR<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	T2CKR<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **T3CKR<6:0>:** Assign Timer3 External Clock (T3CK) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **T2CKR<6:0>:** Assign Timer2 External Clock (T2CK) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

REGISTER 11-6: RPINR5: PERIPHERAL PIN SELECT INPUT REGISTER 5

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	T7CKR<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	T6CKR<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **T7CKR<6:0>:** Assign Timer7 External Clock (T7CK) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **T6CKR<6:0>:** Assign Timer6 External Clock (T6CK) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

REGISTER 15-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32
bit 15							bit 8

R/W-0	R/W-0 HS	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL<4:0>				
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **FLTMD:** Fault Mode Select bit
- 1 = Fault mode is maintained until the Fault source is removed; the corresponding OCFLTx bit is cleared in software and a new PWM period starts
- 0 = Fault mode is maintained until the Fault source is removed and a new PWM period starts

bit 14 **FLTOUT:** Fault Out bit
- 1 = PWM output is driven high on a Fault
- 0 = PWM output is driven low on a Fault

bit 13 **FLTTRIEN:** Fault Output State Select bit
- 1 = OCx pin is tri-stated on Fault condition
- 0 = OCx pin I/O state defined by FLTOUT bit on Fault condition

bit 12 **OCINV:** OCMP Invert bit
- 1 = OCx output is inverted
- 0 = OCx output is not inverted

bit 11-9 **Unimplemented:** Read as '0'

bit 8 **OC32:** Cascade Two OCx Modules Enable bit (32-bit operation)
- 1 = Cascade module operation is enabled
- 0 = Cascade module operation is disabled

bit 7 **OCTRIG:** OCx Trigger/Sync Select bit
- 1 = Triggers OCx from source designated by SYNCSELx bits
- 0 = Synchronizes OCx with source designated by SYNCSELx bits

bit 6 **TRIGSTAT:** Timer Trigger Status bit
- 1 = Timer source has been triggered and is running
- 0 = Timer source has not been triggered and is being held clear

bit 5 **OCTRIS:** OCx Output Pin Direction Select bit
- 1 = OCx is tri-stated
- 0 = Output compare module drives the OCx pin

Note 1: Do not use the OCx module as its own Sync or Trigger source.

2: When the OCy module is turned OFF, it sends a trigger out signal. If the OCx module uses the OCy module as a Trigger source, the OCy module must be unselected as a Trigger source prior to disabling it.

TABLE 32-9: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic**	**Min.**	**Typ(1)**	**Max.**	**Units**	**Conditions**
DI60a	IICL	**Input Low Injection Current**	0	—	-5(5,8)	mA	All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP, RB11, SOSCI, SOSCO, D+, D-, VUSB3V3 and VBUS
DI60b	IICH	**Input High Injection Current**	0	—	+5(6,7,4)	mA	All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP, RB11, SOSCI, SOSCO, D+, D-, VUSB3V3 and VBUS, and all 5V tolerant pins(7)
DI60c	∑IICT	**Total Input Injection Current (sum of all I/O and control pins)**	-20(9)	—	+20(9)	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins (| IICL + | IICH |) ≤ ∑IICT

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: See **"Pin Diagrams"** for the 5V tolerant I/O pins.

5: VIL source < (VSS – 0.3). Characterized but not tested.

6: Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.

7: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.

8: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

9: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted, provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

10: These parameters are characterized, but not tested.

32.2 AC Characteristics and Timing Parameters

This section defines the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 AC characteristics and timing parameters.

TABLE 32-14: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended Operating voltage VDD range as described in **Section 32.1 "DC Characteristics"**.

FIGURE 32-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

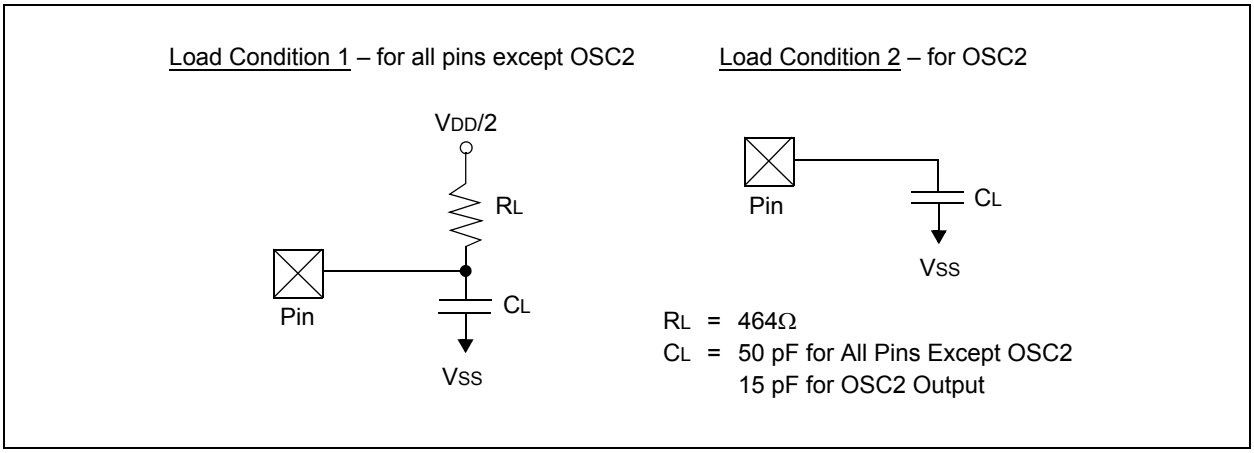


TABLE 32-15: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

Param.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DO50	COSCO	OSC2 Pin	—	—	15	pF	In XT and HS modes when external clock is used to drive OSC1
DO56	CIO	All I/O Pins and OSC2	—	—	50	pF	EC mode
DO58	CB	SCLx, SDAx	—	—	400	pF	In I^2C™ mode

FIGURE 32-7: TIMERQ (QEI MODULE) EXTERNAL CLOCK TIMING CHARACTERISTICS

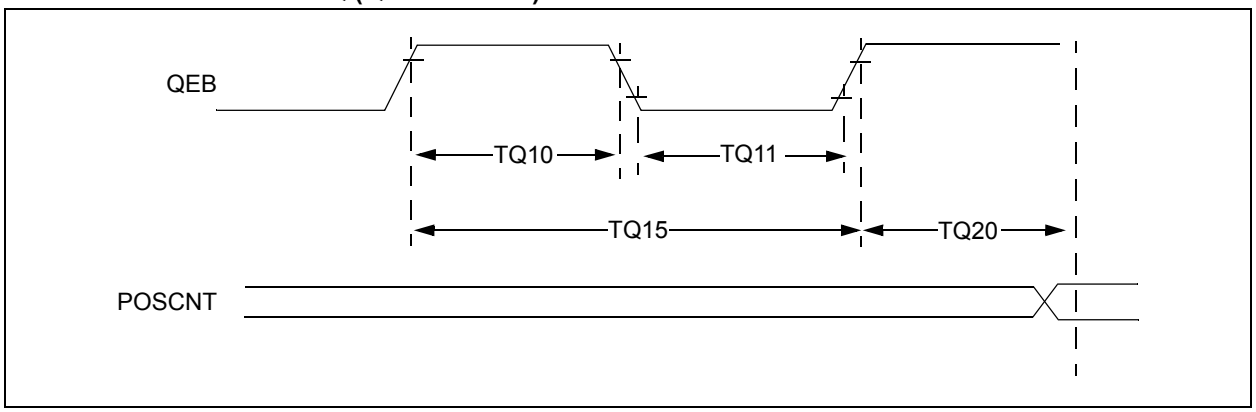


TABLE 32-26: QEI MODULE EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**		**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
TQ10	TtQH	TQCK High Time	Synchronous, with Prescaler	[Greater of (12.5 or 0.5 TCY)/N] + 25	—	—	ns	Must also meet Parameter TQ15
TQ11	TtQL	TQCK Low Time	Synchronous, with Prescaler	[Greater of (12.5 or 0.5 TCY)/N] + 25	—	—	ns	Must also meet Parameter TQ15
TQ15	TtQP	TQCP Input Period	Synchronous, with Prescaler	[Greater of (25 or TCY)/N] + 50	—	—	ns	
TQ20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		—	1	TCY	—	

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 32-42: PARALLEL SLAVE PORT TIMING

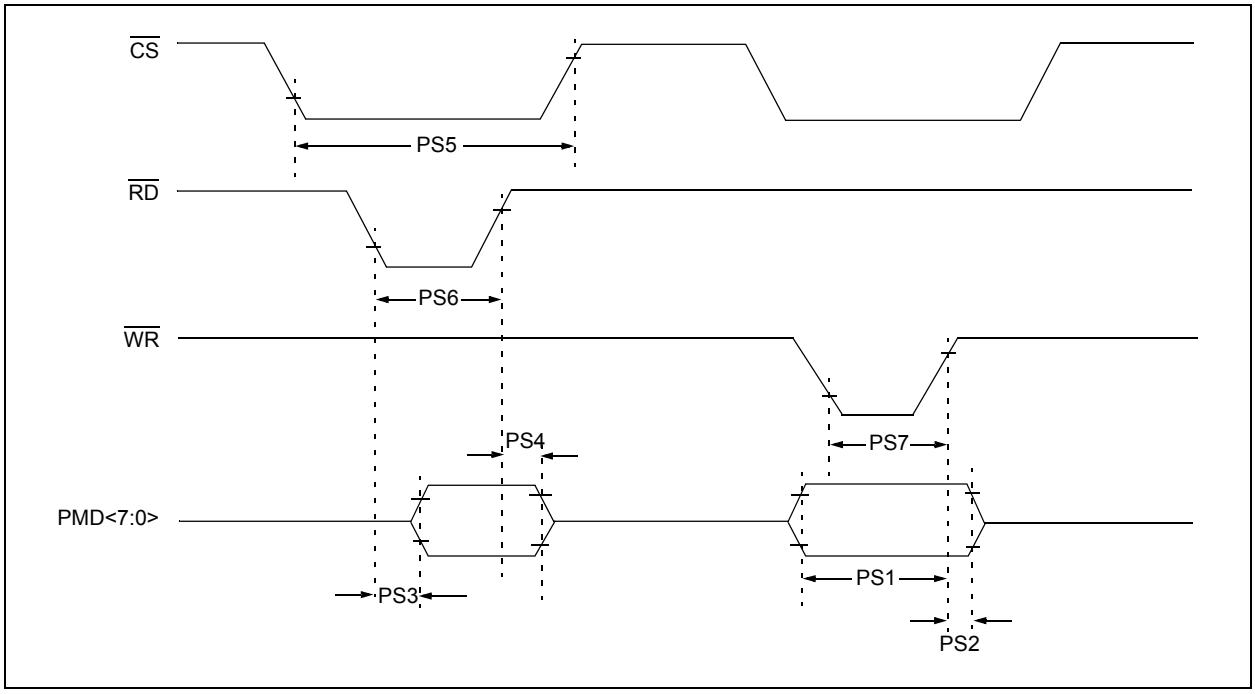


TABLE 32-65: PARALLEL SLAVE PORT TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
PS1	TdtV2wrH	Data In Valid Before $\overline{WR}$ or $\overline{CS}$ Inactive (setup time)	20	—	—	ns	
PS2	TwrH2dtI	$\overline{WR}$ or $\overline{CS}$ Inactive to Data In Invalid (hold time)	20	—	—	ns	
PS3	TrdL2dtV	$\overline{RD}$ and $\overline{CS}$ to Active Data Out Valid	—	—	80	ns	
PS4	TrdH2dtI	$\overline{RD}$ or $\overline{CS}$ Inactive to Data Out Invalid	10	—	30	ns	
PS5	Tcs	$\overline{CS}$ Active Time	33.33	—	—	ns	
PS6	Twr	$\overline{RD}$ Active Time	33.33	—	—	ns	
PS7	Trd	$\overline{WR}$ Active Time	33.33	—	—	ns	

Note 1: These parameters are characterized, but not tested in manufacturing.

TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 4.0 "Memory Organization"	Added the Write Latch and Auxiliary Interrupt Vector to the Program Memory Map (see Figure 4-1). Updated the All Resets value for the DSRPAG and DSWPAG registers in the CPU Core Register Maps (see Table 4-1 and Table 4-2). Updated the All Resets value for the INTCON2 register in the Interrupt Controller Register Maps (see Table 4-3 through Table 4-6). Updated the All Resets values for all registers in the Output Compare 1 - Output Compare 16 Register Map, with the exception of the OCxTMR and OCxCON1 registers (see Table 4-9). Removed the DTM bit (TRGCON1<7> from all PWM Generator # Register Maps (see Table 4-11 through Table 4-17). Updated the All Resets value for the QEI1IOC register in the QEI1 Register Map (see Table 4-18). Updated the All Resets value for the QEI2IOC register in the QEI1 Register Map (see Table 4-19). Added Note 4 to the USB OTG Register Map (see Table 4-25) Updated all addresses in the Real-Time Clock and Calendar Register Map (see Table 4-34). Removed RPINR22 from Table 4-37 through Table 4-40. Updated the All Resets values for all registers in the Peripheral Pin Select Input Register Maps and modified the RPIN37-RPINR43 registers (see Table 4-37 through Table 4-40). Added the VREGSF bit (RCON<11>) to the System Control Register Map (see Table 4-43). Added the REFOMD bit (PMD4<3>) to the PMD Register Maps (see Table 4-44 through Table 4-47). Changed the bit range for CNT from <15:0> to <13:0> for all DMAxCNT registers in the DMAC Register Map (see Table 4-49). Updated the All Resets value and removed the ANSC15 and ANSC12 bits in the ANSLEC registers in the PORTC Register Maps (see Table 4-52 and Table 4-53). Updated DSxPAG and Page Description of O, Read and U, Read in Table 4-66. Added Note to the Table 4-67. Updated Arbiter Architecture in Figure 4-8. Updated the Unimplemented value and removed the LATG3 and LATG2 bits in the LATG registers and the CNPUG3 and CNPUG2 bits from the CNPUG registers in the PORTG Register Maps (see Table 4-60 and Table 4-61) Updated the All Resets value and removed the TRISG3 and TRISG2 bits in the TRISG registers and the ODCG3 and ODCG2 bits from the ODCG registers in the PORTG Register Maps (see Table 4-60 and Table 4-61).
Section 5.0 "Flash Program Memory"	Updated the NVMOP<3:0> = 1110 definition to Reserved and added Note 6 to the Nonvolatile Memory (NVM) Control Register (see Register 5-1).
Section 6.0 "Resets"	Added the VREGSF bit (RCON<11>) to the Reset Control Register (see Register 6-1).

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