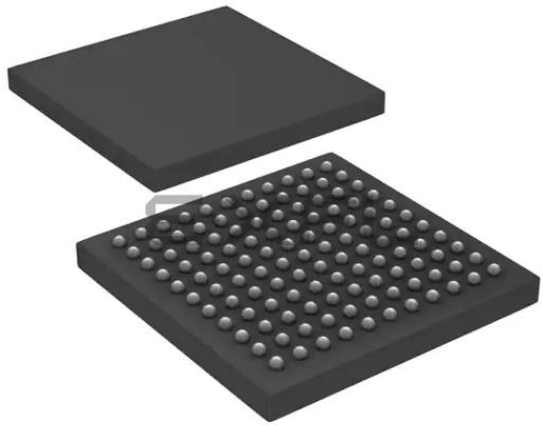

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

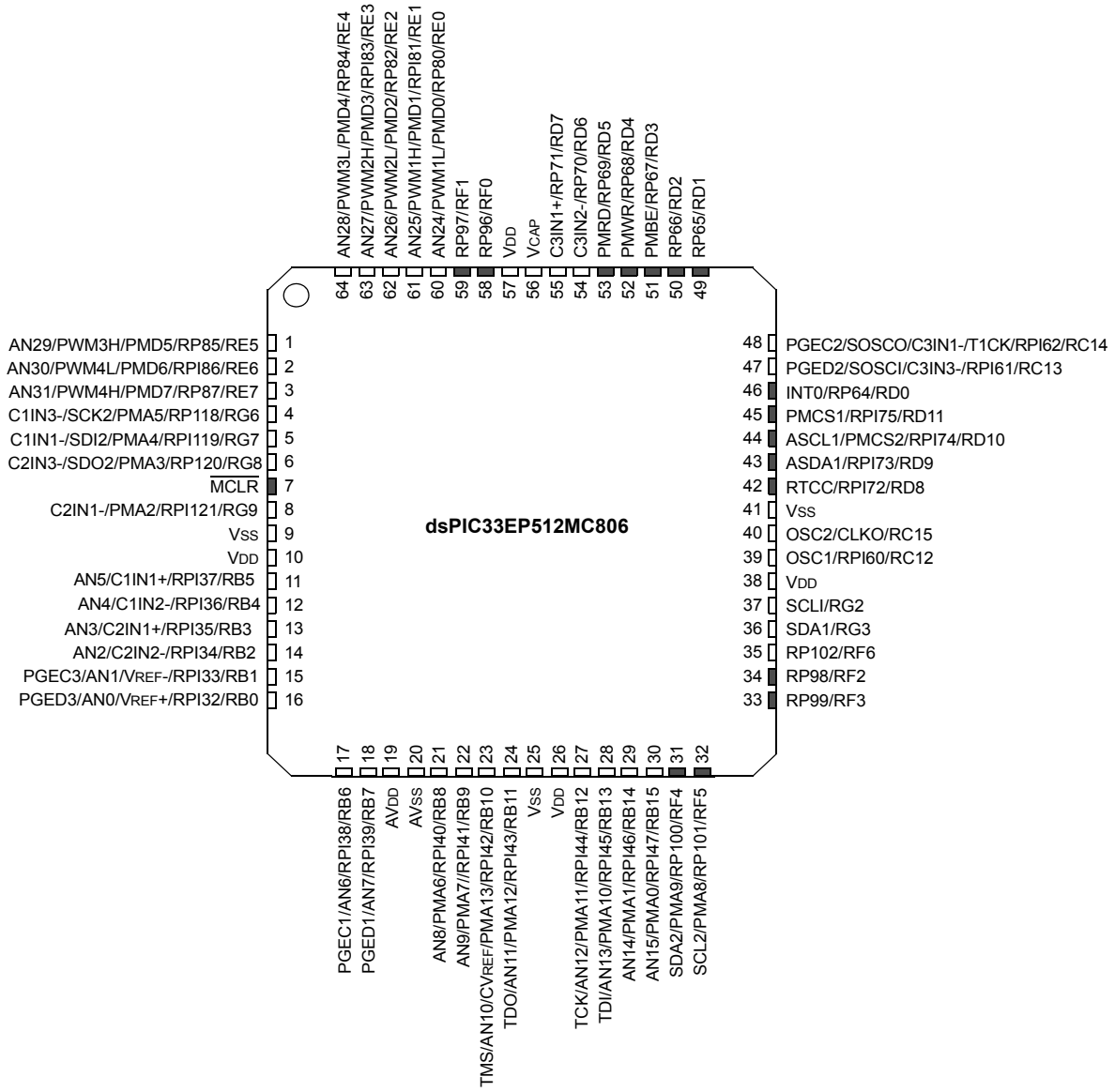
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 16-Bit |
| Speed | 60 MIPs |
| Connectivity | CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 83 |
| Program Memory Size | 256KB (85.5K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 12K x 16 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 32x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 121-TFBGA |
| Supplier Device Package | 121-TFBGA (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic24ep256gu810-e-bg |

## Pin Diagrams

**64-Pin QFN**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The availability of $I^2C$™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

## Pin Diagrams (Continued)

**121-Pin TFBGA(1)**

● = Pins are up to 5V tolerant

**dsPIC33EP256MU810**
**dsPIC33EP512MU810**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | RE4 | RE3 | RG13 | RE0 | RG0 | RF1 | VDD | NC | RD12 | RD2 | RD1 |
| B | NC | RG15 | RE2 | RE1 | RA7 | RF0 | VCAP | RD5 | RD3 | VSS | RC14 |
| C | RE6 | VDD | RG12 | RG14 | RA6 | NC | RD7 | RD4 | NC | RC13 | RD11 |
| D | RC1 | RE7 | RE5 | NC | NC | NC | RD6 | RD13 | RD0 | NC | RD10 |
| E | RC4 | RC3 | RG6 | RC2 | NC | RG1 | NC | RA15 | RD8 | RD9 | RA14 |
| F | $\overline{MCLR}$ | RG8 | RG9 | RG7 | VSS | NC | NC | VDD | RC12 | VSS | RC15 |
| G | RE8 | RE9 | RA0 | NC | VDD | VSS | VSS | NC | RA5 | RA3 | RA4 |
| H | RB5 | RB4 | NC | NC | NC | VDD | NC | VBUS | VUSB3V3 | RG2 | RA2 |
| J | RB3 | RB2 | RB7 | AVDD | RB11 | RA1 | RB12 | NC | NC | RF8 | RG3 |
| K | RB1 | RB0 | RA10 | RB8 | NC | RF12 | RB14 | VDD | RD15 | RF3 | RF2 |
| L | RB6 | RA9 | AVSS | RB9 | RB10 | RF13 | RB13 | RB15 | RD14 | RF4 | RF5 |

**Note 1:** Refer to Table 2 for full pin names.

### 4.1.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in word-addressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (Figure 4-2).

Program memory addresses are always word-aligned on the lower word and addresses are incremented or decremented by two during code execution. This arrangement provides compatibility with data memory space addressing and makes data in the program memory space accessible.

### 4.1.2 INTERRUPT AND TRAP VECTORS

All devices reserve the addresses between 0x00000 and 0x000200 for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A GOTO instruction is programmed by the user application at address 0x000000 of the primary Flash memory or at address 0x7FFFFC of the auxiliary Flash memory, with the actual address for the start of code at address 0x000002 of the primary Flash memory or at address 0x7FFFFE of the auxiliary Flash memory. Reset Target Vector Select bit (RSTPRI) in the FPOR Configuration register controls whether primary or auxiliary Flash Reset location is used.

A more detailed discussion of the interrupt vector tables is provided in **Section 7.1 "Interrupt Vector Table"**.

**FIGURE 4-2: PROGRAM MEMORY ORGANIZATION**

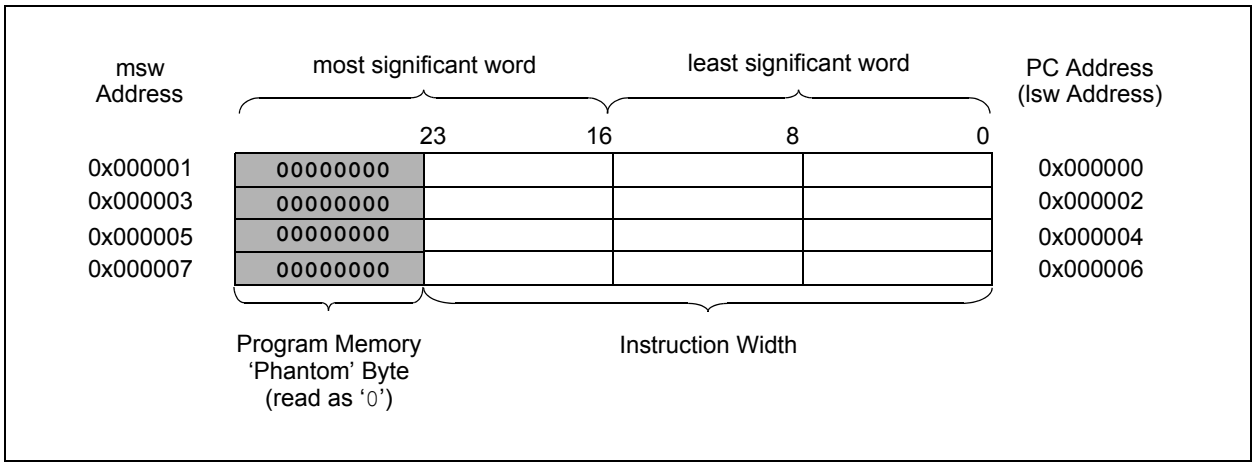


**TABLE 4-11: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 16 REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OC1CON1 | 0900 | — | — | OCSIDL | OCTSEL<2:0> | | | ENFLTC | ENFLTB | ENFLTA | OCFLTC | OCFLTB | OCFLTA | TRIGMODE | OCM<2:0> | | | 0000 |
| OC1CON2 | 0902 | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL<4:0> | | | | | 000C |
| OC1RS | 0904 | Output Compare 1 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC1R | 0906 | Output Compare 1 Register | | | | | | | | | | | | | | | | xxxx |
| OC1TMR | 0908 | Timer Value 1 Register | | | | | | | | | | | | | | | | xxxx |
| OC2CON1 | 090A | — | — | OCSIDL | OCTSEL<2:0> | | | ENFLTC | ENFLTB | ENFLTA | OCFLTC | OCFLTB | OCFLTA | TRIGMODE | OCM<2:0> | | | 0000 |
| OC2CON2 | 090C | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL<4:0> | | | | | 000C |
| OC2RS | 090E | Output Compare 2 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC2R | 0910 | Output Compare 2 Register | | | | | | | | | | | | | | | | xxxx |
| OC2TMR | 0912 | Timer Value 2 Register | | | | | | | | | | | | | | | | xxxx |
| OC3CON1 | 0914 | — | — | OCSIDL | OCTSEL<2:0> | | | ENFLTC | ENFLTB | ENFLTA | OCFLTC | OCFLTB | OCFLTA | TRIGMODE | OCM<2:0> | | | 0000 |
| OC3CON2 | 0916 | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL<4:0> | | | | | 000C |
| OC3RS | 0918 | Output Compare 3 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC3R | 091A | Output Compare 3 Register | | | | | | | | | | | | | | | | xxxx |
| OC3TMR | 091C | Timer Value 3 Register | | | | | | | | | | | | | | | | xxxx |
| OC4CON1 | 091E | — | — | OCSIDL | OCTSEL<2:0> | | | ENFLTC | ENFLTB | ENFLTA | OCFLTC | OCFLTB | OCFLTA | TRIGMODE | OCM<2:0> | | | 0000 |
| OC4CON2 | 0920 | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL<4:0> | | | | | 000C |
| OC4RS | 0922 | Output Compare 4 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC4R | 0924 | Output Compare 4 Register | | | | | | | | | | | | | | | | xxxx |
| OC4TMR | 0926 | Timer Value 4 Register | | | | | | | | | | | | | | | | xxxx |
| OC5CON1 | 0928 | — | — | OCSIDL | OCTSEL<2:0> | | | ENFLTC | ENFLTB | ENFLTA | OCFLTC | OCFLTB | OCFLTA | TRIGMODE | OCM<2:0> | | | 0000 |
| OC5CON2 | 092A | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL<4:0> | | | | | 000C |
| OC5RS | 092C | Output Compare 5 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC5R | 092D | Output Compare 5 Register | | | | | | | | | | | | | | | | xxxx |
| OC5TMR | 0930 | Timer Value 5 Register | | | | | | | | | | | | | | | | xxxx |
| OC6CON1 | 0932 | — | — | OCSIDL | OCTSEL<2:0> | | | ENFLTC | ENFLTB | ENFLTA | OCFLTC | OCFLTB | OCFLTA | TRIGMODE | OCM<2:0> | | | 0000 |
| OC6CON2 | 0934 | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL<4:0> | | | | | 000C |
| OC6RS | 0936 | Output Compare 6 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC6R | 0938 | Output Compare 6 Register | | | | | | | | | | | | | | | | xxxx |
| OC6TMR | 093A | Timer Value 6 Register | | | | | | | | | | | | | | | | xxxx |
| OC7CON1 | 093C | — | — | OCSIDL | OCTSEL<2:0> | | | ENFLTC | ENFLTB | ENFLTA | OCFLTC | OCFLTB | OCFLTA | TRIGMODE | OCM<2:0> | | | 0000 |
| OC7CON2 | 093E | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL<4:0> | | | | | 000C |
| OC7RS | 0940 | Output Compare 7 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC7R | 0942 | Output Compare 7 Register | | | | | | | | | | | | | | | | xxxx |
| OC7TMR | 0944 | Timer Value 7 Register | | | | | | | | | | | | | | | | xxxx |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-41: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXMU810 DEVICES ONLY (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPINR35 | 06E6 | — | IC14R<6:0> | | | | | | | — | IC13R<6:0> | | | | | | | 0000 |
| RPINR36 | 06E8 | — | IC16R<6:0> | | | | | | | — | IC15R<6:0> | | | | | | | 0000 |
| RPINR37 | 06EA | — | SYNCI1R<6:0> | | | | | | | — | OCFCR<6:0> | | | | | | | 0000 |
| RPINR38 | 06EC | — | DTCMP1R<6:0> | | | | | | | — | SYNCI2R<6:0> | | | | | | | 0000 |
| RPINR39 | 06EE | — | DTCMP3R<6:0> | | | | | | | — | DTCMP2R<6:0> | | | | | | | 0000 |
| RPINR40 | 06F0 | — | DTCMP5R<6:0> | | | | | | | — | DTCMP4R<6:0> | | | | | | | 0000 |
| RPINR41 | 06F2 | — | — | — | — | — | — | — | — | — | DTCMP6R<6:0> | | | | | | | 0000 |
| RPINR42 | 06F4 | — | FLT6R<6:0> | | | | | | | — | FLT5R<6:0> | | | | | | | 0000 |
| RPINR43 | 06F6 | — | — | — | — | — | — | — | — | — | FLT7R<6:0> | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-42: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXX(MC/MU)806 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPINR0 | 06A0 | — | INT1R<6:0> | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR1 | 06A2 | — | INT3R<6:0> | | | | | | | — | INT2R<6:0> | | | | | | | 0000 |
| RPINR2 | 06A4 | — | — | — | — | — | — | — | — | — | INT4R<6:0> | | | | | | | 0000 |
| RPINR3 | 06A6 | — | T3CKR<6:0> | | | | | | | — | T2CKR<6:0> | | | | | | | 0000 |
| RPINR4 | 06A8 | — | T5CKR<6:0> | | | | | | | — | T4CKR<6:0> | | | | | | | 0000 |
| RPINR5 | 06AA | — | T7CKR<6:0> | | | | | | | — | T6CKR<6:0> | | | | | | | 0000 |
| RPINR6 | 06AC | — | T9CKR<6:0> | | | | | | | — | T8CKR<6:0> | | | | | | | 0000 |
| RPINR7 | 06AE | — | IC2R<6:0> | | | | | | | — | IC1R<6:0> | | | | | | | 0000 |
| RPINR8 | 06B0 | — | IC4R<6:0> | | | | | | | — | IC3R<6:0> | | | | | | | 0000 |
| RPINR9 | 06B2 | — | IC6R<6:0> | | | | | | | — | IC5R<6:0> | | | | | | | 0000 |
| RPINR10 | 06B4 | — | IC8R<6:0> | | | | | | | — | IC7R<6:0> | | | | | | | 0000 |
| RPINR11 | 06B6 | — | OCFBR<6:0> | | | | | | | — | OCFAR<6:0> | | | | | | | 0000 |
| RPINR12 | 06B8 | — | FLT2R<6:0> | | | | | | | — | FLT1R<6:0> | | | | | | | 0000 |
| RPINR13 | 06BA | — | FLT4R<6:0> | | | | | | | — | FLT3R<6:0> | | | | | | | 0000 |
| RPINR14 | 06BC | — | QEB1R<6:0> | | | | | | | — | QEA1R<6:0> | | | | | | | 0000 |
| RPINR15 | 06BE | — | HOME1R<6:0> | | | | | | | — | INDX1R<6:0> | | | | | | | 0000 |
| RPINR16 | 06C0 | — | QEB2R<6:0> | | | | | | | — | QEA2R<6:0> | | | | | | | 0000 |
| RPINR17 | 06C2 | — | HOME2R<6:0> | | | | | | | — | INDX2R<6:0> | | | | | | | 0000 |
| RPINR18 | 06C4 | — | U1CTSR<6:0> | | | | | | | — | U1RXR<6:0> | | | | | | | 0000 |
| RPINR19 | 06C6 | — | U2CTSR<6:0> | | | | | | | — | U2RXR<6:0> | | | | | | | 0000 |
| RPINR20 | 06C8 | — | SCK1R<6:0> | | | | | | | — | SDI1R<6:0> | | | | | | | 0000 |
| RPINR21 | 06CA | — | — | — | — | — | — | — | — | — | SS1R<6:0> | | | | | | | 0000 |
| RPINR23 | 06CE | — | — | — | — | — | — | — | — | — | SS2R<6:0> | | | | | | | 0000 |
| RPINR24 | 06D0 | — | CSCKR<6:0> | | | | | | | — | CSDIR<6:0> | | | | | | | 0000 |
| RPINR25 | 06D2 | — | — | — | — | — | — | — | — | — | COFSINR<6:0> | | | | | | | 0000 |
| RPINR26 | 06D4 | — | C2RXR<6:0> | | | | | | | — | C1RXR<6:0> | | | | | | | 0000 |
| RPINR27 | 06D6 | — | U3CTSR<6:0> | | | | | | | — | U3RXR<6:0> | | | | | | | 0000 |
| RPINR28 | 06D8 | — | U4CTSR<6:0> | | | | | | | — | U4RXR<6:0> | | | | | | | 0000 |
| RPINR29 | 06DA | — | SCK3R<6:0> | | | | | | | — | SDI3R<6:0> | | | | | | | 0000 |
| RPINR30 | 06DC | — | — | — | — | — | — | — | — | — | SS3R<6:0> | | | | | | | 0000 |
| RPINR31 | 06DE | — | SCK4R<6:0> | | | | | | | — | SDI4R<6:0> | | | | | | | 0000 |
| RPINR32 | 06E0 | — | — | — | — | — | — | — | — | — | SS4R<6:0> | | | | | | | 0000 |
| RPINR33 | 06E2 | — | IC10R<6:0> | | | | | | | — | IC9R<6:0> | | | | | | | 0000 |
| RPINR34 | 06E4 | — | IC12R<6:0> | | | | | | | — | IC11R<6:0> | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**NOTES:**

**REGISTER 9-3: PLLFBD: PLL FEEDBACK DIVISOR REGISTER(1)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | PLLDIV<8> |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PLLDIV<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

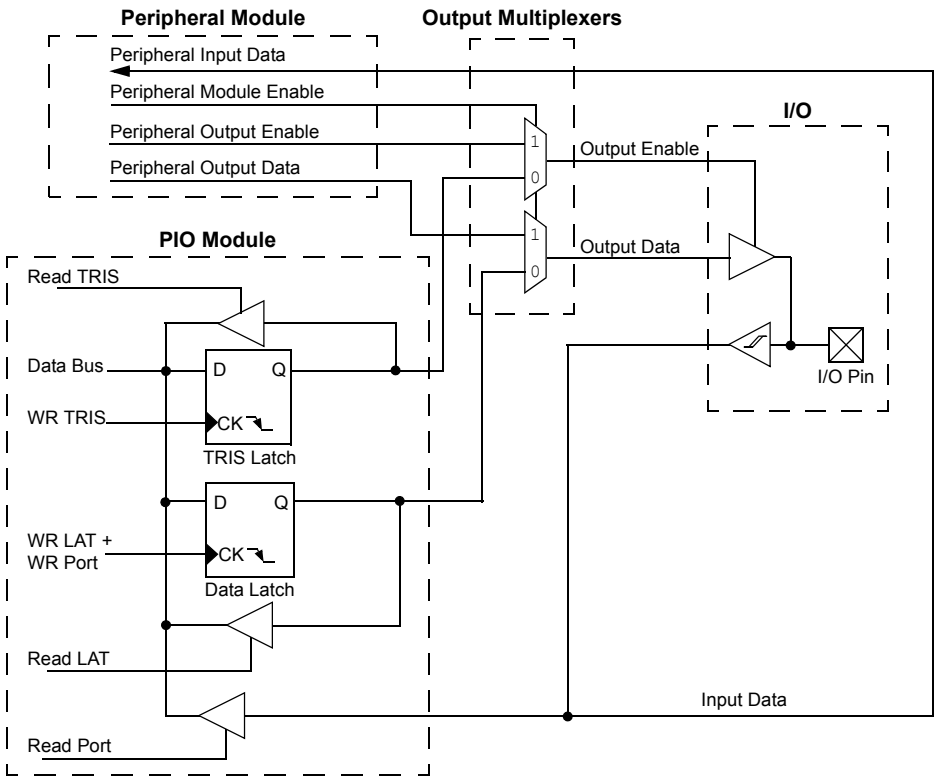
bit 15-9 **Unimplemented:** Read as '0'

bit 8-0 **PLLDIV<8:0>:** PLL Feedback Divisor bits (also denoted as 'M', PLL multiplier)

111111111 = 513
•
•
•
000110000 = 50 (default)
•
•
•
000000010 = 4
000000001 = 3
000000000 = 2

**Note 1:** This register is reset only on a Power-on Reset (POR).

**FIGURE 11-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE**



## 11.5 I/O Helpful Tips

1. In some cases, certain pins, as defined in Table 32-9 in **Section 32.0 "Electrical Characteristics"** under "Injection Current", have internal protection diodes to VDD and VSS; the term "Injection Current" is also referred to as "Clamp Current". On designated pins, with sufficient external current-limiting precautions by the user, I/O pin input voltages are allowed to be greater or less than the data sheet absolute maximum ratings with respect to the VSS and VDD supplies. Note that when the user application forward biases either of the high or low side internal input clamp diodes, that the resulting current being injected into the device that is clamped internally by the VDD and VSS power rails, may affect the ADC accuracy by four to six counts.
2. I/O pins that are shared with any analog input pin, (i.e., ANx, see Table 1-1 in **Section 1.0 "Device Overview"**), are always analog pins by default after any Reset. Consequently, configuring a pin as an analog input pin, automatically disables the digital input pin buffer and any attempt to read the digital input level by reading PORTx or LATx will always return a '0', regardless of the digital logic level on the pin. To use a pin as a digital I/O pin on a shared analog pin (see Table 1-1 in **Section 1.0 "Device Overview"**), the user application needs to configure the Analog Pin Configuration registers in the I/O ports module (i.e., ANSELx) by setting the appropriate bit that corresponds to that I/O port pin to a '0'.

| **Note:** | Although it is not possible to use a digital input pin when its analog function is enabled, it is possible to use the digital I/O output function, TRISx = 0x0, while the analog function is also enabled. However, this is not recommended, particularly if the analog input is connected to an external analog voltage source, which would create signal contention between the analog signal and the output pin driver. |
|---|---|

3. Most I/O pins have multiple functions. Referring to the device pin diagrams in the data sheet, the priorities of the functions allocated to any pins are indicated by reading the pin name from left to right. The left most function name takes precedence over any function to its right in the naming convention. For example: AN16/T2CK/T7CK/RC1; this indicates that AN16 is the highest priority in this example and will supersede all other functions to its right in the list. Those other functions to its right, even if enabled, would not work as long as any other function to its left was enabled. This rule applies to all of the functions listed for a given pin. Dedicated peripheral functions are always higher priority than remappable functions. I/O pins are always the lowest priority.
4. Each pin has an internal weak pull-up resistor and pull-down resistor that can be configured using the CNPUx and CNPDx registers, respectively. These resistors eliminate the need for external resistors in certain applications. The internal pull-up is up to ~(VDD-0.8), not VDD. This value is still above the minimum VIH of CMOS and TTL devices.
5. When driving LEDs directly, the I/O pin can source or sink more current than what is specified in the VOH/IOH and VOL/IOL DC characteristic specification. The respective IOH and IOL current rating only applies to maintaining the corresponding output at or above the VOH and at or below the VOL levels. However, for LEDs, unlike digital inputs of an externally connected device, they are not governed by the same minimum VIH/VIL levels. An I/O pin output can safely sink or source any current less than that listed in the absolute maximum rating section of the data sheet. For example:

   VOH = 2.4v @ IOH = -8 mA and VDD = 3.3V

   The maximum output current sourced by any 8 mA I/O pin = 12 mA.

   LED source current < 12 mA is technically permitted. Refer to the VOH/IOH graphs in **Section 32.0 "Electrical Characteristics"** for additional information.
6. The Peripheral Pin Select (PPS) pin mapping rules are as follows:
   a) Only one "output" function can be active on a given pin at any time regardless if it is a dedicated or remappable function (one pin, one output).
   b) It is possible to assign a "remappable output" function to multiple pins and externally short or tie them together for increased current drive.
   c) If any "dedicated output" function is enabled on a pin, it will take precedence over any remappable "output" function.
   d) If any "dedicated digital" (input or output) function is enabled on a pin, any number of "input" remappable functions can be mapped to the same pin.
   e) If any "dedicated analog" function(s) are enabled on a given pin, "digital input(s)" of any kind will all be disabled, although a single "digital output", at the user's cautionary discretion, can be enabled and active as long as there is no signal contention with an external analog input signal. For example, it is possible for the ADC to convert the digital output logic level, or to toggle a digital output on a comparator or ADC input, provided there is no external analog input, such as for a built-in self test.
   f) Any number of "input" remappable functions can be mapped to the same pin(s) at the same time, including any pin with a single output from either a dedicated or remappable "output".

**REGISTER 11-22: RPINR21: PERIPHERAL PIN SELECT INPUT REGISTER 21**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | SS1R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **SS1R<6:0>:** Assign SPI1 Slave Select Input ($\overline{SS1}$) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-23: RPINR23: PERIPHERAL PIN SELECT INPUT REGISTER 23**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | SS2R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

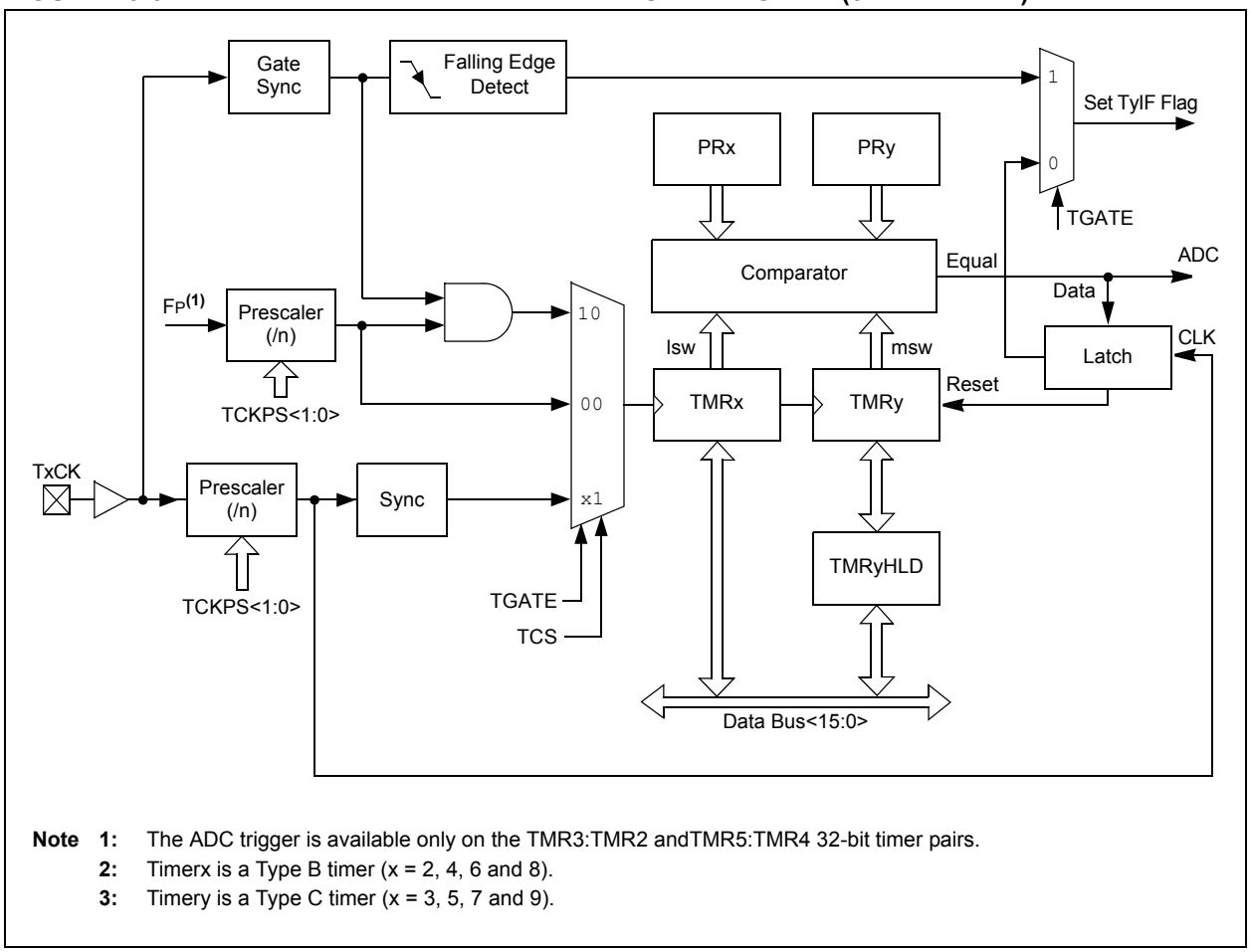
| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **SS2R<6:0>:** Assign SPI2 Slave Select Input ($\overline{SS2}$) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**FIGURE 13-3: TYPE B/TYPE C TIMER PAIR BLOCK DIAGRAM (32-BIT TIMER)**




**Note 1:** The ADC trigger is available only on the TMR3:TMR2 andTMR5:TMR4 32-bit timer pairs.
**2:** Timerx is a Type B timer (x = 2, 4, 6 and 8).
**3:** Timery is a Type C timer (x = 3, 5, 7 and 9).

## 13.1 Timer Resources

Many useful resources related to timers are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310 |
|---|---|

### 13.1.1 KEY RESOURCES

- **Section 11. "Timers"** (DS70362) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

## 13.2 Timerx/y Control Registers

**REGISTER 13-1: TxCON: (T2CON, T4CON, T6CON OR T8CON) CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| TON | — | TSIDL | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | TGATE | TCKPS<1:0> | | T32 | — | TCS(1) | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **TON:** Timerx On bit
When T32 = 1:
1 = Starts 32-bit Timerx/y
0 = Stops 32-bit Timerx/y
When T32 = 0:
1 = Starts 16-bit Timerx
0 = Stops 16-bit Timerx

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timerx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timerx Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timerx Input Clock Prescale Select bits
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3 **T32:** 32-Bit Timer Mode Select bit
1 = Timerx and Timery form a single 32-bit timer
0 = Timerx and Timery act as two 16-bit timers

bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timerx Clock Source Select bit(1)
1 = External clock from TxCK pin (on the rising edge)
0 = Internal clock (FP)

bit 0 **Unimplemented:** Read as '0'

**Note 1:** The TxCK pin is not available on all timers. Refer to the **"Pin Diagrams"** section for the available pins.

**REGISTER 17-2: QEIxIOC: QEIx I/O CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QCAPEN | FLTREN | QFDIV<2:0> | | | OUTFNC<1:0> | | SWPAB |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-x | R-x | R-x | R-x |
|---|---|---|---|---|---|---|---|
| HOMPOL | IDXPOL | QEBPOL | QEAPOL | HOME | INDEX | QEB | QEA |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **QCAPEN:** Position Counter Input Capture Enable bit
1 = Positive edge detect of home input triggers position capture function
0 = HOMEx input event (positive edge) does not trigger a capture event

bit 14 **FLTREN:** QEAx/QEBx/INDXx/HOMEx Digital Filter Enable bit
1 = Input pin digital filter is enabled
0 = Input pin digital filter is disabled (bypassed)

bit 13-11 **QFDIV<2:0>:** QEAx/QEBx/INDXx/HOMEx Digital Input Filter Clock Divide Select bits
111 = 1:256 clock divide
110 = 1:64 clock divide
101 = 1:32 clock divide
100 = 1:16 clock divide
011 = 1:8 clock divide
010 = 1:4 clock divide
001 = 1:2 clock divide
000 = 1:1 clock divide

bit 10-9 **OUTFNC<1:0>:** QEI Module Output Function Mode Select bits
11 = The CTNCMPx pin goes high when QEIxLEC ≥ POSxCNT ≥ QEIxGEC
10 = The CTNCMPx pin goes high when POSxCNT ≤ QEIxLEC
01 = The CTNCMPx pin goes high when POSxCNT ≥ QEIxGEC
00 = Output is disabled

bit 8 **SWPAB:** Swap QEA and QEB Inputs bit
1 = QEAx and QEBx are swapped prior to quadrature decoder logic
0 = QEAx and QEBx are not swapped

bit 7 **HOMPOL:** HOMEx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 6 **IDXPOL:** HOMEx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 5 **QEBPOL:** QEBx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 4 **QEAPOL:** QEAx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 3 **HOME:** Status of HOMEx Input Pin After Polarity Control bit
1 = Pin is at logic '1'
0 = Pin is at logic '0'

## 20.3 UARTx Registers

**REGISTER 20-1: UxMODE: UARTx MODE REGISTER**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| UARTEN(1) | — | USIDL | IREN(2) | RTSMD | — | UEN<1:0> | |
| bit 15 | | | | | | | bit 8 |

| R/W-0, HC | R/W-0 | R/W-0, HC | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| WAKE | LPBACK | ABAUD | URXINV | BRGH | PDSEL<1:0> | | STSEL |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HC = Hardware Clearable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **UARTEN:** UARTx Enable bit(1)
- 1 = UARTx is enabled; all UARTx pins are controlled by UARTx as defined by UEN<1:0>
- 0 = UARTx is disabled; all UARTx pins are controlled by port latches; UARTx power consumption is minimal

bit 14 **Unimplemented:** Read as '0'

bit 13 **USIDL:** UARTx Stop in Idle Mode bit
- 1 = Discontinues module operation when device enters Idle mode
- 0 = Continues module operation in Idle mode

bit 12 **IREN:** IrDA® Encoder and Decoder Enable bit(2)
- 1 = IrDA encoder and decoder are enabled
- 0 = IrDA encoder and decoder are disabled

bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit
- 1 = $\overline{\text{UxRTS}}$ pin in Simplex mode
- 0 = $\overline{\text{UxRTS}}$ pin in Flow Control mode

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **UEN<1:0>:** UARTx Pin Enable bits
- 11 = UxTX, UxRX and BCLK pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by port latches
- 10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used
- 01 = UxTX, UxRX and $\overline{\text{UxRTS}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by port latches
- 00 = UxTX and UxRX pins are enabled and used; $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$/BCLK pins are controlled by port latches

bit 7 **WAKE:** Wake-up on Start Bit Detect During Sleep Mode Enable bit
- 1 = UARTx continues to sample the UxRX pin; interrupt is generated on falling edge; bit is cleared in hardware on following rising edge
- 0 = No wake-up is enabled

bit 6 **LPBACK:** UARTx Loopback Mode Select bit
- 1 = Enables Loopback mode
- 0 = Loopback mode is disabled

bit 5 **ABAUD:** Auto-Baud Enable bit
- 1 = Enables baud rate measurement on the next character – requires reception of a Sync field (55h) before other data; cleared in hardware upon completion
- 0 = Baud rate measurement is disabled or has completed

**Note 1:** Refer to **Section 17. "UART"** (DS70582) in the *"dsPIC33E/PIC24E Family Reference Manual"* for information on enabling the UARTx module for receive or transmit operation.

**2:** This feature is only available for the 16x BRG mode (BRGH = 0).

**REGISTER 21-10: CxCFG2: ECANx BAUD RATE CONFIGURATION REGISTER 2**

| U-0 | R/W-x | U-0 | U-0 | U-0 | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | WAKFIL | — | — | — | SEG2PH<2:0> | | |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| SEG2PHTS | SAM | SEG1PH<2:0> | | | PRSEG<2:0> | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14 **WAKFIL:** Select CAN Bus Line Filter for Wake-up bit
1 = Uses CAN bus line filter for wake-up
0 = CAN bus line filter is not used for wake-up

bit 13-11 **Unimplemented:** Read as '0'

bit 10-8 **SEG2PH<2:0>:** Phase Segment 2 bits
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

bit 7 **SEG2PHTS:** Phase Segment 2 Time Select bit
1 = Freely programmable
0 = Maximum of SEG1PH bits or Information Processing Time (IPT), whichever is greater

bit 6 **SAM:** Sample of the CAN Bus Line bit
1 = Bus line is sampled three times at the sample point
0 = Bus line is sampled once at the sample point

bit 5-3 **SEG1PH<2:0>:** Phase Segment 1 bits
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

bit 2-0 **PRSEG<2:0>:** Propagation Time Segment bits
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

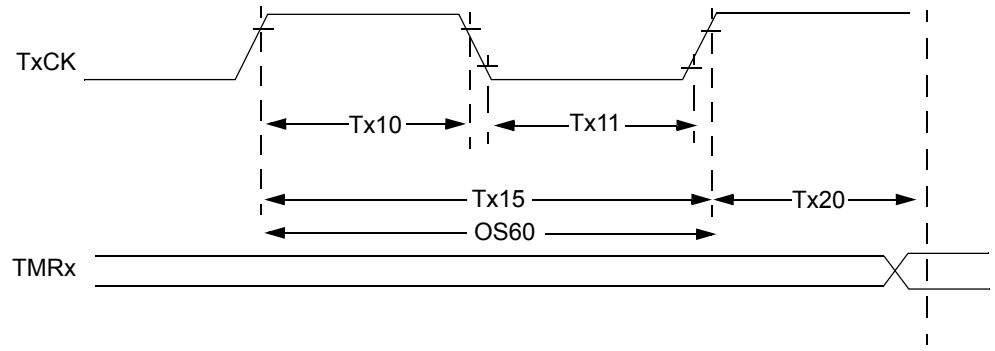
**TABLE 29-2: CONFIGURATION BITS DESCRIPTION (CONTINUED)**

| Bit Field | Register | RTSP Effect | Description |
|---|---|---|---|
| WINDIS | FWDT | Immediate | Watchdog Timer Window Enable bit<br>1 = Watchdog Timer is in Non-Window mode<br>0 = Watchdog Timer is in Window mode |
| PLLKEN | FWDT | Immediate | PLL Lock Wait Enable bit<br>1 = Clock switches to the PLL source will wait until the PLL lock signal is valid<br>0 = Clock switch will not wait for PLL lock |
| WDTPRE | FWDT | Immediate | Watchdog Timer Prescaler bit<br>1 = 1:128<br>0 = 1:32 |
| APLK<1:0> | FAS(2) | Immediate | Auxiliary Segment Key bits<br>These bits must be set to '00' if AWRP = 1 and APL = 1. These bits must be set to '11' for any other value of the AWRP and APL bits.<br>Any mismatch between either the AWRP or APL bits and the APLK bits (as described above), will result in code protection becoming enabled for the Auxiliary Segment. A Flash bulk erase will be required to unlock the device. |
| APL | FAS(2) | Immediate | Auxiliary Segment Code-Protect bit<br>1 = Auxiliary program memory is not code-protected<br>0 = Auxiliary program memory is code-protected |
| AWRP | FAS(2) | Immediate | Auxiliary Segment Write-Protect bit<br>1 = Auxiliary program memory is not write-protected<br>0 = Auxiliary program memory is write-protected |
| WDTPOST<3:0> | FWDT | Immediate | Watchdog Timer Postscaler bits<br>1111 = 1:32,768<br>1110 = 1:16,384<br>•<br>•<br>•<br>0001 = 1:2<br>0000 = 1:1 |
| FPWRT<2:0> | FPOR | Immediate | Power-on Reset Timer Value Select bits<br>111 = PWRT = 128 ms<br>110 = PWRT = 64 ms<br>101 = PWRT = 32 ms<br>100 = PWRT = 16 ms<br>011 = PWRT = 8 ms<br>010 = PWRT = 4 ms<br>001 = PWRT = 2 ms<br>000 = PWRT = Disabled |
| BOREN(1) | FPOR | Immediate | Brown-out Reset (BOR) Detection Enable bit<br>1 = BOR is enabled<br>0 = BOR is disabled |
| ALTI2C2 | FPOR | Immediate | Alternate $I^2C$™ pins for I2C2 bit<br>1 = I2C2 is mapped to the SDA2/SCL2 pins<br>0 = I2C2 is mapped to the ASDA2/ASCL2 pins |
| ALTI2C1 | FPOR | Immediate | Alternate $I^2C$ pins for I2C1 bit<br>1 = I2C1 is mapped to the SDA1/SCL1 pins<br>0 = I2C1 is mapped to the ASDA1/ASCL1 pins |

**Note 1:** BOR should always be enabled for proper operation (BOREN = 1).

**2:** This register can only be modified when code protection and write protection are disabled for both the General and Auxiliary Segments (APL = 1, AWRP = 1, APLK = 0, GSS = 1, GWRP = 1 and GSSK = 0).

**FIGURE 32-6: TIMER1-TIMER9 EXTERNAL CLOCK TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.

**TABLE 32-23: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS(1)**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(2)** | | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| TA10 | TTXH | TxCK High Time | Synchronous mode | Greater of: 20 or (TCY + 20)/N | — | — | ns | Must also meet Parameter TA15, N = prescaler value (1, 8, 64, 256) |
| | | | Asynchronous | 35 | — | — | ns | |
| TA11 | TTXL | TxCK Low Time | Synchronous mode | Greater of: 20 or (TCY + 20)/N | — | — | ns | Must also meet Parameter TA15, N = prescaler value (1, 8, 64, 256) |
| | | | Asynchronous | 10 | — | — | ns | |
| TA15 | TTXP | TxCK Input Period | Synchronous mode | Greater of: 40 or (2 TCY + 40)/N | — | — | ns | N = prescale value (1, 8, 64, 256) |
| OS60 | Ft1 | SOSC1/T1CK Oscillator Input Frequency Range (oscillator enabled by setting bit, TCS (T1CON<1>)) | | DC | — | 50 | kHz | |
| TA20 | TCKEXTMRL | Delay from External TxCK Clock Edge to Timer Increment | | 0.75 TCY + 40 | — | 1.75 TCY + 40 | ns | |

**Note 1:** Timer1 is a Type A.

**2:** These parameters are characterized, but are not tested in manufacturing.

**TABLE 32-61: COMPARATOR TIMING SPECIFICATIONS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (see Note 3) (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| 300 | TRESP | Response Time(2) | — | 150 | 400 | ns | |
| 301 | TMC2OV | Comparator Mode Change to Output Valid | — | — | 10 | μs | |

**Note 1:** Parameters are characterized but not tested.

**2:** Response time is measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from VSS to VDD.

**3:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.

**TABLE 32-62: COMPARATOR MODULE SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (see Note 2) (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| D300 | VIOFF | Input Offset Voltage | — | ±10 | — | mV | |
| D301 | VICM | Input Common-Mode Voltage | AVSS | — | AVDD | V | |
| D302 | CMRR | Common-Mode Rejection Ratio | -54 | — | — | dB | |
| D305 | IVREF | Internal Voltage Reference | 0.19 | 0.20 | 0.21 | V | BGSEL<1:0> = 10 |
| | | | 0.57 | 0.60 | 0.63 | V | BGSEL<1:0> = 01 |
| | | | 1.14 | 1.20 | 1.26 | V | BGSEL<1:0> = 00 |

**Note 1:** Parameters are characterized but not tested.

**2:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.

**TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)**

| Section Name | Update Description |
|---|---|
| **Section 4.0 "Memory Organization"** | Added the Write Latch and Auxiliary Interrupt Vector to the Program Memory Map (see Figure 4-1).<br><br>Updated the All Resets value for the DSRPAG and DSWPAG registers in the CPU Core Register Maps (see Table 4-1 and Table 4-2).<br><br>Updated the All Resets value for the INTCON2 register in the Interrupt Controller Register Maps (see Table 4-3 through Table 4-6).<br><br>Updated the All Resets values for all registers in the Output Compare 1 - Output Compare 16 Register Map, with the exception of the OCxTMR and OCxCON1 registers (see Table 4-9).<br><br>Removed the DTM bit (TRGCON1<7> from all PWM Generator # Register Maps (see Table 4-11 through Table 4-17).<br><br>Updated the All Resets value for the QEI1IOC register in the QEI1 Register Map (see Table 4-18).<br><br>Updated the All Resets value for the QEI2IOC register in the QEI1 Register Map (see Table 4-19).<br><br>Added Note 4 to the USB OTG Register Map (see Table 4-25)<br><br>Updated all addresses in the Real-Time Clock and Calendar Register Map (see Table 4-34).<br><br>Removed RPINR22 from Table 4-37 through Table 4-40.<br><br>Updated the All Resets values for all registers in the Peripheral Pin Select Input Register Maps and modified the RPIN37-RPINR43 registers (see Table 4-37 through Table 4-40).<br><br>Added the VREGSF bit (RCON<11>) to the System Control Register Map (see Table 4-43).<br><br>Added the REFOMD bit (PMD4<3>) to the PMD Register Maps (see Table 4-44 through Table 4-47).<br><br>Changed the bit range for CNT from <15:0> to <13:0> for all DMAxCNT registers in the DMAC Register Map (see Table 4-49).<br><br>Updated the All Resets value and removed the ANSC15 and ANSC12 bits in the ANSLEC registers in the PORTC Register Maps (see Table 4-52 and Table 4-53).<br><br>Updated DSxPAG and Page Description of O, Read and U, Read in Table 4-66.<br><br>Added Note to the Table 4-67.<br><br>Updated Arbiter Architecture in Figure 4-8.<br><br>Updated the Unimplemented value and removed the LATG3 and LATG2 bits in the LATG registers and the CNPUG3 and CNPUG2 bits from the CNPUG registers in the PORTG Register Maps (see Table 4-60 and Table 4-61)<br><br>Updated the All Resets value and removed the TRISG3 and TRISG2 bits in the TRISG registers and the ODCG3 and ODCG2 bits from the ODCG registers in the PORTG Register Maps (see Table 4-60 and Table 4-61). |
| **Section 5.0 "Flash Program Memory"** | Updated the NVMOP<3:0> = 1110 definition to Reserved and added Note 6 to the Nonvolatile Memory (NVM) Control Register (see Register 5-1). |
| **Section 6.0 "Resets"** | Added the VREGSF bit (RCON<11>) to the Reset Control Register (see Register 6-1). |