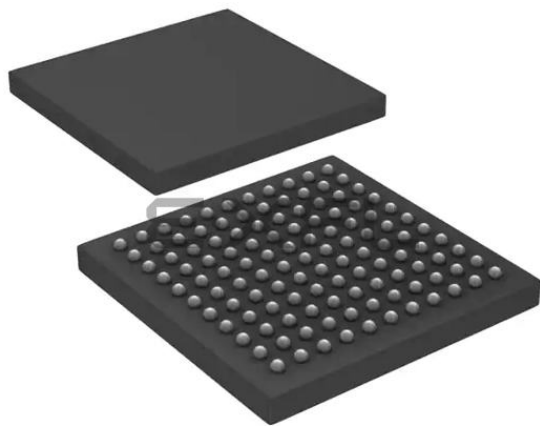




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Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	83
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep256gu810t-i-bg

3.5 Programmer's Model

The programmer's model is shown in Figure 3-2. All registers in the programmer's model are memory mapped and can be manipulated directly by instructions. Table 3-1 lists a description of each register.

In addition to the registers contained in the programmer's model, all devices in this family contain control registers for interrupts, while the dsPIC33EPXXX(GP/MC/MU)806/810/814 devices contain control registers for Modulo and Bit-reversed Addressing. These registers are described in subsequent sections of this document.

All registers associated with the programmer's model are memory mapped, as shown in Table 4-1.

TABLE 3-1: PROGRAMMER'S MODEL REGISTER DESCRIPTIONS

Register(s) Name	Description
W0 through W15	Working Register Array
ACCA, ACCB	40-Bit DSP Accumulators
PC	23-Bit Program Counter
SR	ALU and DSP Engine Status register
SPLIM	Stack Pointer Limit Value register
TBLPAG	Table Memory Page Address register
DSRPAG	Extended Data Space (EDS) Read Page register
DSWPAG	Extended Data Space (EDS) Write Page register
RCOUNT	REPEAT Loop Count register
DCOUNT ⁽¹⁾	DO Loop Count register
DOSTARTH ^(1,2) , DOSTARTL ^(1,2)	DO Loop Start Address register (High and Low)
DOENDH ⁽¹⁾ , DOENDL ⁽¹⁾	DO Loop End Address register (High and Low)
CORCON	Contains DSP Engine, DO Loop Control and Trap Status bits

Note 1: This register is available on dsPIC33EPXXX(GP/MC/MU)806/810/814 devices only.

2: The DOSTARTH and DOSTARTL registers are read-only.

TABLE 4-1: CPU CORE REGISTER MAP FOR dsPIC33EPXXX(GP/MC/MU)806/810/814 DEVICES ONLY (CONTINUED)

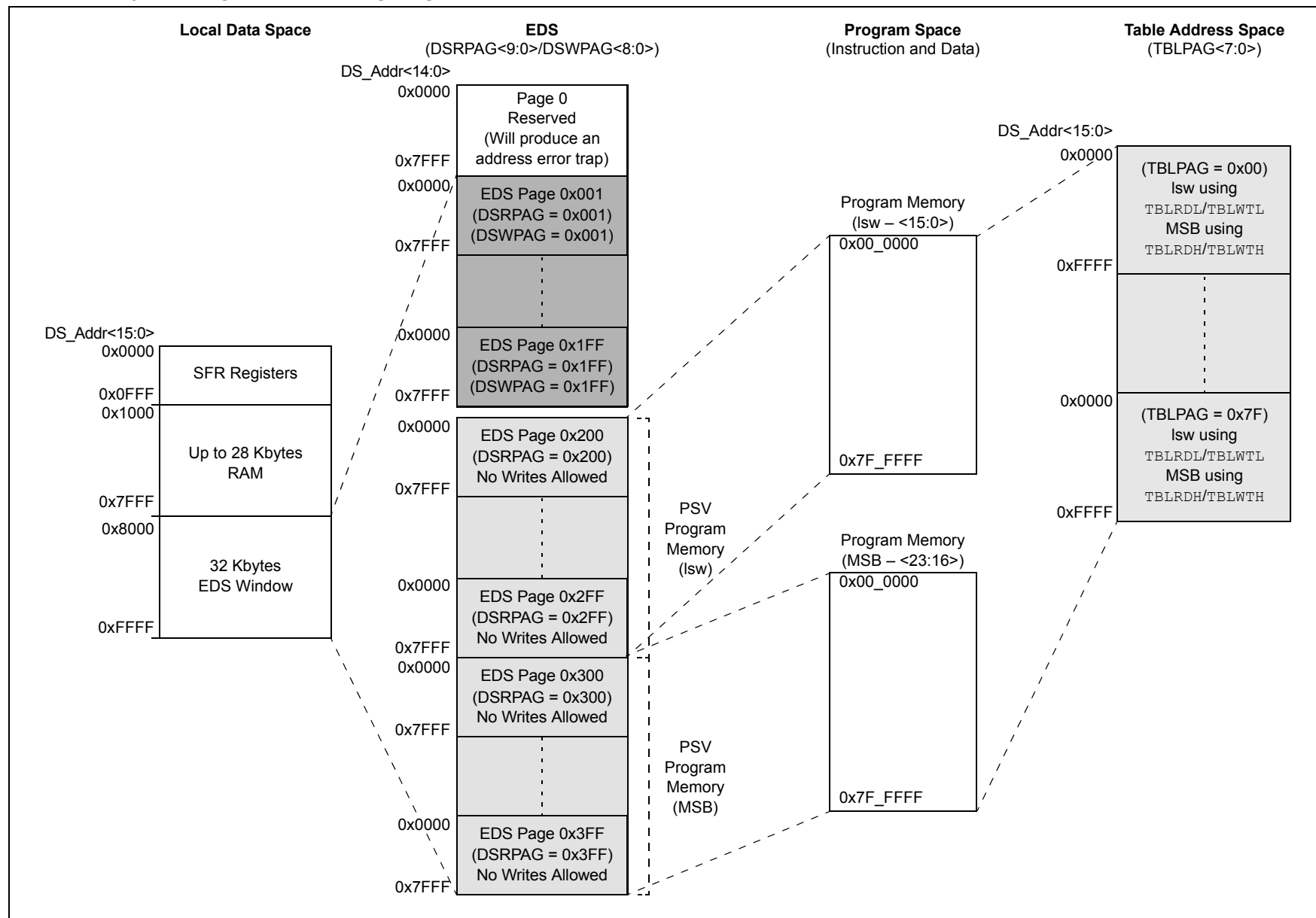
File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
SR	0042	OA	OB	SA	SB	OAB	SAB	DA	DC	IPL2	IPL1	IPL0	RA	N	OV	Z	C	0000	
CORCON	0044	VAR	—	US<1:0>		EDT	DL<2:0>			SATA	SATB	SATDW	ACCSAT	IPL3	SFA	RND	IF	0020	
MODCON	0046	XMODEN	YMODEN	—	—	BWM<3:0>				YWM<3:0>				XWM<3:0>				0000	
XMODSRT	0048	XMODSRT<15:1>																0	0000
XMODEND	004A	XMODEND<15:1>																1	0001
YMODSRT	004C	YMODSRT<15:1>																0	0000
YMODEND	004E	YMODEND<15:1>																1	0001
XBREV	0050	BREN	XBREV<14:0>																0000
DISCNT	0052	—	—	DISCNT<13:0>														0000	
TBLPAG	0054	—	—	—	—	—	—	—	—	TBLPAG<7:0>								0000	
MSTRPR	0058	MSTRPR<15:0>																0000	

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-53: COMPARATOR REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMSTAT	0A80	CMSIDL	—	—	—	—	C3EVT	C2EVT	C1EVT	—	—	—	—	—	C3OUT	C2OUT	C1OUT	0000
CVRCON	0A82	—	—	—	—	—	VREFSEL	BGSEL<1:0>		CVREN	CVROE	CVRR	CVRSS	CVR<3:0>				0000
CM1CON	0A84	CON	COE	CPOL	—	—	—	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
CM1MSKSRC	0A86	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
CM1MSKCON	0A88	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM1FLTR	0A8A	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000
CM2CON	0A8C	CON	COE	CPOL	—	—	—	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
CM2MSKSRC	0A8E	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
CM2MSKCON	0A90	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM2FLTR	0A92	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000
CM3CON	0A94	CON	COE	CPOL	—	—	—	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
CM3MSKSRC	0A96	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
CM3MSKCON	0A98	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM3FLTR	0A9A	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

EXAMPLE 4-3: PAGED DATA MEMORY SPACE

REGISTER 8-11: DMAPWC: DMA PERIPHERAL WRITE COLLISION STATUS REGISTER

U-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
—	PWCOL14	PWCOL13	PWCOL12	PWCOL11	PWCOL10	PWCOL9	PWCOL8
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
PWCOL7	PWCOL6	PWCOL5	PWCOL4	PWCOL3	PWCOL2	PWCOL1	PWCOL0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **Unimplemented:** Read as '0'
- bit 14 **PWCOL14:** Channel 14 Peripheral Write Collision Flag bit
 1 = Write collision detected
 0 = No write collision detected
- bit 13 **PWCOL13:** Channel 13 Peripheral Write Collision Flag bit
 1 = Write collision detected
 0 = No write collision detected
- bit 12 **PWCOL12:** Channel 12 Peripheral Write Collision Flag bit
 1 = Write collision detected
 0 = No write collision detected
- bit 11 **PWCOL11:** Channel 11 Peripheral Write Collision Flag bit
 1 = Write collision detected
 0 = No write collision detected
- bit 10 **PWCOL10:** Channel 10 Peripheral Write Collision Flag bit
 1 = Write collision detected
 0 = No write collision detected
- bit 9 **PWCOL9:** Channel 9 Peripheral Write Collision Flag bit
 1 = Write collision detected
 0 = No write collision detected
- bit 8 **PWCOL8:** Channel 8 Peripheral Write Collision Flag bit
 1 = Write collision detected
 0 = No write collision detected
- bit 7 **PWCOL7:** Channel 7 Peripheral Write Collision Flag bit
 1 = Write collision detected
 0 = No write collision detected
- bit 6 **PWCOL6:** Channel 6 Peripheral Write Collision Flag bit
 1 = Write collision detected
 0 = No write collision detected
- bit 5 **PWCOL5:** Channel 5 Peripheral Write Collision Flag bit
 1 = Write collision detected
 0 = No write collision detected
- bit 4 **PWCOL4:** Channel 4 Peripheral Write Collision Flag bit
 1 = Write collision detected
 0 = No write collision detected
- bit 3 **PWCOL3:** Channel 3 Peripheral Write Collision Flag bit
 1 = Write collision detected
 0 = No write collision detected

REGISTER 8-12: DMARQC: DMA REQUEST COLLISION STATUS REGISTER (CONTINUED)

- bit 2 **RQCOL2:** Channel 2 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected
- bit 1 **RQCOL1:** Channel 1 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected
- bit 0 **RQCOL0:** Channel 0 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

9.3 Oscillator Control Registers

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER^(1,3)

U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	R/W-y
—	COSC<2:0>			—	NOSC<2:0> ⁽²⁾		
bit 15				bit 8			

R/W-0	R/W-0	R-0	U-0	R/C-0	U-0	R/W-0	R/W-0
CLKLOCK	IOLOCK	LOCK	—	CF	—	LPOSCEN	OSWEN
bit 7				bit 0			

Legend:	y = Value Set from Configuration bits on POR	C = Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits (read-only)

- 111 = Fast RC Oscillator (FRC) with Divide-by-N
- 110 = Fast RC Oscillator (FRC) with Divide-by-16
- 101 = Low-Power RC Oscillator (LPRC)
- 100 = Secondary Oscillator (SOSC)
- 011 = Primary Oscillator (XT, HS, EC) with PLL
- 010 = Primary Oscillator (XT, HS, EC)
- 001 = Fast RC Oscillator (FRC) with Divide-by-N and PLL
- 000 = Fast RC Oscillator (FRC)

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits⁽²⁾

- 111 = Fast RC Oscillator (FRC) with Divide-by-N
- 110 = Fast RC Oscillator (FRC) with Divide-by-16
- 101 = Low-Power RC Oscillator (LPRC)
- 100 = Secondary Oscillator (SOSC)
- 011 = Primary Oscillator (XT, HS, EC) with PLL
- 010 = Primary Oscillator (XT, HS, EC)
- 001 = Fast RC Oscillator (FRC) with Divide-by-N and PLL
- 000 = Fast RC Oscillator (FRC)

bit 7 **CLKLOCK:** Clock Lock Enable bit

- 1 = If (FCKSM0 = 1), then clock and PLL configurations are locked
If (FCKSM0 = 0), then clock and PLL configurations may be modified
- 0 = Clock and PLL selections are not locked, configurations may be modified

bit 6 **IOLOCK:** I/O Lock Enable bit

- 1 = I/O lock is active
- 0 = I/O lock is not active

bit 5 **LOCK:** PLL Lock Status bit (read-only)

- 1 = Indicates that PLL is in lock or PLL start-up timer is satisfied
- 0 = Indicates that PLL is out of lock, start-up timer is in progress or PLL is disabled

bit 4 **Unimplemented:** Read as '0'

Note 1: Writes to this register require an unlock sequence. Refer to **Section 7. "Oscillator"** (DS70580) in the *"dsPIC33E/PIC24E Family Reference Manual"* (available from the Microchip web site) for details.

2: Direct clock switches between any Primary Oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.

3: This register resets only on a Power-on Reset (POR).

REGISTER 11-34: RPINR34: PERIPHERAL PIN SELECT INPUT REGISTER 34

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IC12R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IC11R<6:0>						
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **IC12R<6:0>:** Assign Input Capture 12 (IC12) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **IC11R<6:0>:** Assign Input Capture 11 (IC11) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

14.2 Input Capture Control Registers

REGISTER 14-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	ICSIDL	ICTSEL<2:0>			—	—
bit 15						bit 8	

U-0	R/W-0	R/W-0	R/HC/HS-0	R/HC/HS-0	R/W-0	R/W-0	R/W-0
—	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		
bit 7							bit 0

Legend:

R = Readable bit HC = Hardware Clearable bit HS = Hardware Settable bit '0' = Bit is cleared
 -n = Value at POR W = Writable bit U = Unimplemented bit, read as '0'

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **ICSIDL:** Input Capture Stop in Idle Control bit
 1 = Input capture will Halt in CPU Idle mode
 0 = Input capture will continue to operate in CPU Idle mode

bit 12-10 **ICTSEL<12:10>:** Input Capture Timer Select bits
 111 = Peripheral clock (FP) is the clock source of the ICx
 110 = Reserved
 101 = Reserved
 100 = Clock source of T1CLK is the clock source of the ICx (only the synchronous clock is supported)
 011 = Clock source of T5CLK is the clock source of the ICx
 010 = Clock source of T4CLK is the clock source of the ICx
 001 = Clock source of T2CLK is the clock source of the ICx
 000 = Clock source of T3CLK is the clock source of the ICx

bit 9-7 **Unimplemented:** Read as '0'

bit 6-5 **ICI<1:0>:** Number of Captures per Interrupt Select bits (this field is not used if ICM<2:0> = 001 or 111)
 11 = Interrupt on every fourth capture event
 10 = Interrupt on every third capture event
 01 = Interrupt on every second capture event
 00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)
 1 = Input capture buffer overflow occurred
 0 = No input capture buffer overflow occurred

bit 3 **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)
 1 = Input capture buffer is not empty, at least one more capture value can be read
 0 = Input capture buffer is empty

bit 2-0 **ICM<2:0>:** Input Capture Mode Select bits
 111 = Input capture functions as interrupt pin only in CPU Sleep and Idle modes (rising edge detect only, all other control bits are not applicable)
 110 = Unused (module disabled)
 101 = Capture mode, every 16th rising edge (Prescaler Capture mode)
 100 = Capture mode, every 4th rising edge (Prescaler Capture mode)
 011 = Capture mode, every rising edge (Simple Capture mode)
 010 = Capture mode, every falling edge (Simple Capture mode)
 001 = Capture mode, every edge rising and falling (Edge Detect mode (ICI<1:0>) is not used in this mode)
 000 = Input capture module is turned off

18.3 SPI Control Registers

REGISTER 18-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
SPIEN	—	SPISIDL	—	—	SPIBEC<2:0>		
bit 15						bit 8	

R/W-0	R/C-0, HS	R/W-0	R/W-0	R/W-0	R/W-0	R-0, HS, HC	R-0, HS, HC
SRMPT	SPIROV	SRXMPT	SISEL<2:0>			SPITBF	SPIRBF
bit 7						bit 0	

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
HS = Hardware Settable bit	HC = Hardware Clearable bit	U = Unimplemented bit, read as '0'	

- bit 15 **SPIEN:** SPIx Enable bit
1 = Enables the module and configures SCKx, SDOx, SDIx and $\overline{SSx}$ as serial port pins
0 = Disables the module
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **SPISIDL:** SPIx Stop in Idle Mode bit
1 = Discontinues the module operation when device enters Idle mode
0 = Continues the module operation in Idle mode
- bit 12-11 **Unimplemented:** Read as '0'
- bit 10-8 **SPIBEC<2:0>:** SPIx Buffer Element Count bits (valid in Enhanced Buffer mode)
Master mode:
Number of SPIx transfers that are pending.
Slave mode:
Number of SPIx transfers that are unread.
- bit 7 **SRMPT:** SPIx Shift Register (SPIxSR) Empty bit (valid in Enhanced Buffer mode)
1 = SPIx Shift register is empty and Ready-to-Send or receive the data
0 = SPIx Shift register is not empty
- bit 6 **SPIROV:** SPIx Receive Overflow Flag bit
1 = A new byte/word is completely received and discarded; the user application has not read the previous data in the SPIxBUF register
0 = No overflow has occurred
- bit 5 **SRXMPT:** SPIx Receive FIFO Empty bit (valid in Enhanced Buffer mode)
1 = RX FIFO is empty
0 = RX FIFO is not empty
- bit 4-2 **SISEL<2:0>:** SPIx Buffer Interrupt Mode bits (valid in Enhanced Buffer mode)
111 = Interrupt when the SPIx transmit buffer is full
110 = Interrupt when last bit is shifted into SPIxSR, and as a result, the TX FIFO is empty
101 = Interrupt when the last bit is shifted out of SPIxSR and the transmit is complete
100 = Interrupt when one data is shifted into the SPIxSR, and as a result, the TX FIFO has one open memory location
011 = Interrupt when the SPIx receive buffer is full
010 = Interrupt when the SPIx receive buffer is 3/4 or more full
001 = Interrupt when data is available in the receive buffer (SRMPT bit is set)
000 = Interrupt when the last data in the receive buffer is read, and as a result, the buffer is empty (SRXMPT bit is set)

REGISTER 21-7: CxINTE: ECANx INTERRUPT ENABLE REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
IVRIE	WAKIE	ERRIE	—	FIFOIE	RBOVIE	RBIE	TBIE
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-8 **Unimplemented:** Read as '0'
- bit 7 **IVRIE:** Invalid Message Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled
- bit 6 **WAKIE:** Bus Wake-up Activity Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled
- bit 5 **ERRIE:** Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled
- bit 4 **Unimplemented:** Read as '0'
- bit 3 **FIFOIE:** FIFO Almost Full Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled
- bit 2 **RBOVIE:** RX Buffer Overflow Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled
- bit 1 **RBIE:** RX Buffer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled
- bit 0 **TBIE:** TX Buffer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

REGISTER 25-4: CMxMSKCON: COMPARATOR x MASK GATING CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN
bit 15		bit 8					

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN
bit 7		bit 0					

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **HLMS:** High or Low-Level Masking Select bits
1 = The masking (blanking) function will prevent any asserted ('0') comparator signal from propagating
0 = The masking (blanking) function will prevent any asserted ('1') comparator signal from propagating
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **OCEN:** OR Gate C Input Enable bit
1 = MCI is connected to OR gate
0 = MCI is not connected to OR gate
- bit 12 **OCNEN:** OR Gate C Input Inverted Enable bit
1 = Inverted MCI is connected to OR gate
0 = Inverted MCI is not connected to OR gate
- bit 11 **OBEN:** OR Gate B Input Enable bit
1 = MBI is connected to OR gate
0 = MBI is not connected to OR gate
- bit 10 **OBNEN:** OR Gate B Input Inverted Enable bit
1 = Inverted MBI is connected to OR gate
0 = Inverted MBI is not connected to OR gate
- bit 9 **OAEN:** OR Gate A Input Enable bit
1 = MAI is connected to OR gate
0 = MAI is not connected to OR gate
- bit 8 **OANEN:** OR Gate A Input Inverted Enable bit
1 = Inverted MAI is connected to OR gate
0 = Inverted MAI is not connected to OR gate
- bit 7 **NAGS:** AND Gate Output Inverted Enable bit
1 = Inverted ANDI is connected to OR gate
0 = Inverted ANDI is not connected to OR gate
- bit 6 **PAGS:** AND Gate Output Enable bit
1 = ANDI is connected to OR gate
0 = ANDI is not connected to OR gate
- bit 5 **ACEN:** AND Gate C Input Enable bit
1 = MCI is connected to AND gate
0 = MCI is not connected to AND gate
- bit 4 **ACNEN:** AND Gate C Input Inverted Enable bit
1 = Inverted MCI is connected to AND gate
0 = Inverted MCI is not connected to AND gate

32.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings

(See Note 1)

Ambient temperature under bias	-40°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on VDD with respect to VSS	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to VSS ⁽³⁾	-0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to VSS when VDD ≥ 3.0V ⁽³⁾	-0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to VSS when VDD < 3.0V ⁽³⁾	-0.3V to 3.6V
Voltage on D+ OR D- pin with respect to VUSB3V3	-0.3V to (VUSB3V3 + 0.3V)
Voltage on VBUS with respect to VSS	-0.3V to +5.5V
Maximum current out of VSS pin	320 mA
Maximum current into VDD pin ⁽²⁾	320 mA
Maximum current sourced/sunk by any 4x I/O pin ⁽⁴⁾	15 mA
Maximum current sourced/sunk by any 8x I/O pin ⁽⁴⁾	25 mA
Maximum current sunk by all ports	200 mA
Maximum current sourced by all ports ⁽²⁾	200 mA

Note 1: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 32-2).

3: See the “Pin Diagrams” section for the 5V tolerant pins.

4: Characterized but not tested.

TABLE 32-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param.	Symbol	Characteristic	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
Operating Voltage							
DC10	VDD	Supply Voltage ⁽³⁾	3.0	—	3.6	V	
DC12	VDR	RAM Data Retention Voltage ⁽²⁾	1.8	—	—	V	
DC16	VPOR	VDD Start Voltage to Ensure Internal Power-on Reset Signal	—	—	VSS	V	
DC17	SVDD	VDD Rise Rate to Ensure Internal Power-on Reset Signal	1.0	—	—	V/ms	0-3.0V in 3 ms

Note 1: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

2: This is the limit to which VDD may be lowered without losing RAM data.

3: Device is functional at $V_{BORMIN} < V_{DD} < V_{DDMIN}$. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.

**TABLE 32-39: SPI1, SPI3 AND SPI4 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0)
TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	TscP	Maximum SCKx Input Frequency	—	—	15	MHz	See Note 3
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx} \downarrow$ to SCKx $\uparrow$ or SCKx $\downarrow$ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx} \uparrow$ to SDOx Output High-Impedance	10	—	50	ns	See Note 4
SP52	Tsch2ssH TscL2ssH	$\overline{SSx} \uparrow$ after SCKx Edge	1.5 TCY + 40	—	—	ns	See Note 4

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCKx is 66.7 ns. Therefore, the SCKx clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

FIGURE 32-31: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)

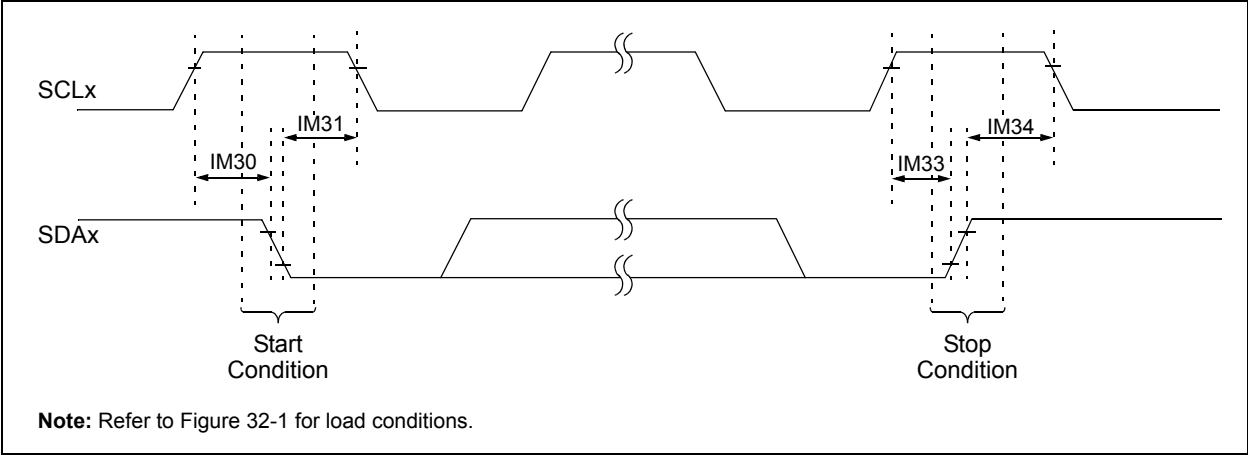


FIGURE 32-32: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)

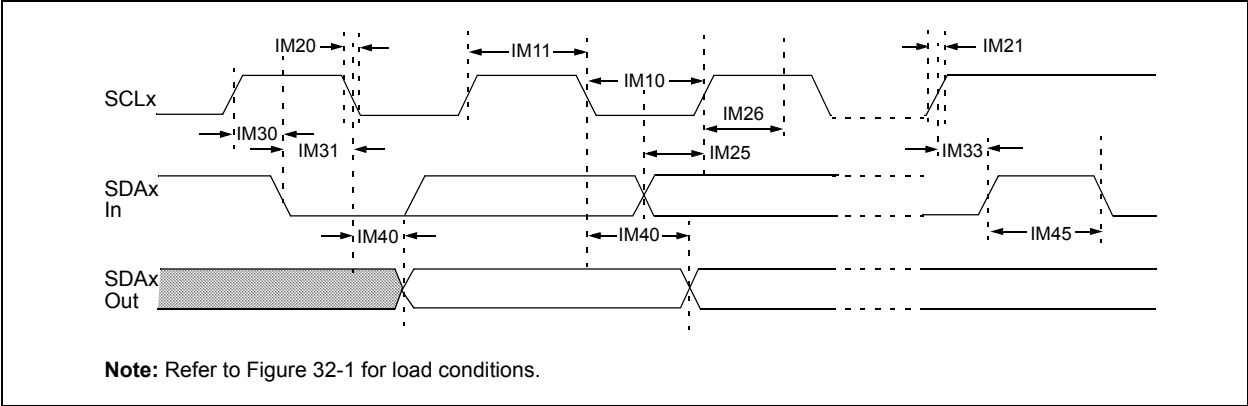


TABLE 32-63: COMPARATOR REFERENCE VOLTAGE SETTling TIME SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (see Note 3) (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽²⁾	Min.	Typ.	Max.	Units	Conditions
VR310	TSET	Settling Time ⁽¹⁾	—	—	10	μs	

- Note 1:** Settling time measured while CVRR = 1 and CVR<3:0> bits transition from '0000' to '1111'.
- 2:** These parameters are characterized, but not tested in manufacturing.
- 3:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.

TABLE 32-64: COMPARATOR REFERENCE VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (see Note 2) (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
VRD310	CVRES	Resolution	CVRSRC/24	—	CVRSRC/32	LSb	
VRD311	CVRAA	Absolute Accuracy	—	—	0.5	LSb	
VRD312	CVRL	Maximum Load on CVREF Output Pin	—	—	0.75	μA	AVDD = 3.6V, CVRSS = 0, CVRR = 0, CVR<3:0> = 1111

- Note 1:** These parameters are characterized, but not tested in manufacturing.
- 2:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.

FIGURE 33-9: TYPICAL FRC FREQUENCY @ VDD = 3.3V

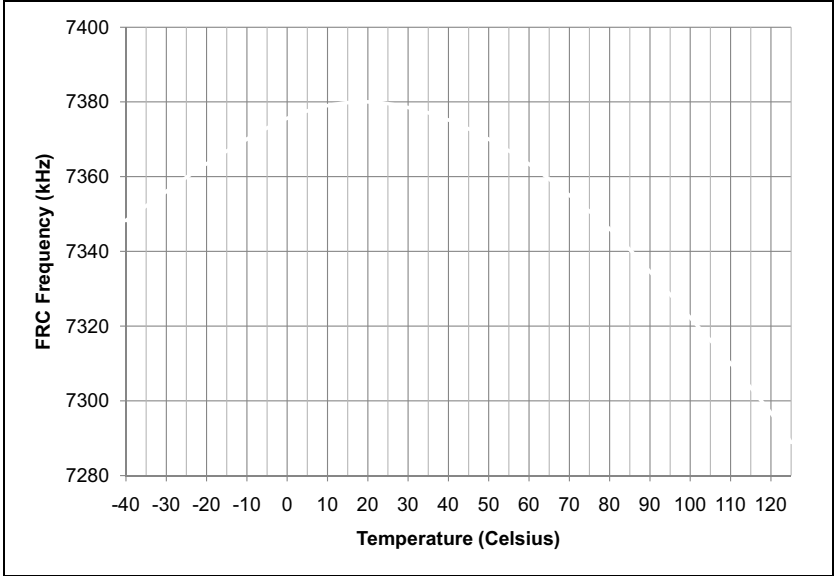
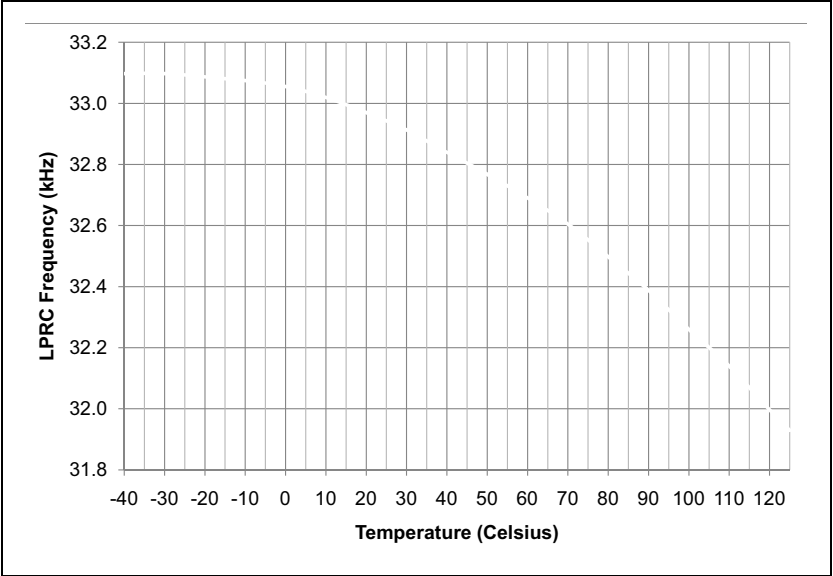


FIGURE 33-10: TYPICAL LPRC FREQUENCY @ VDD = 3.3V



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