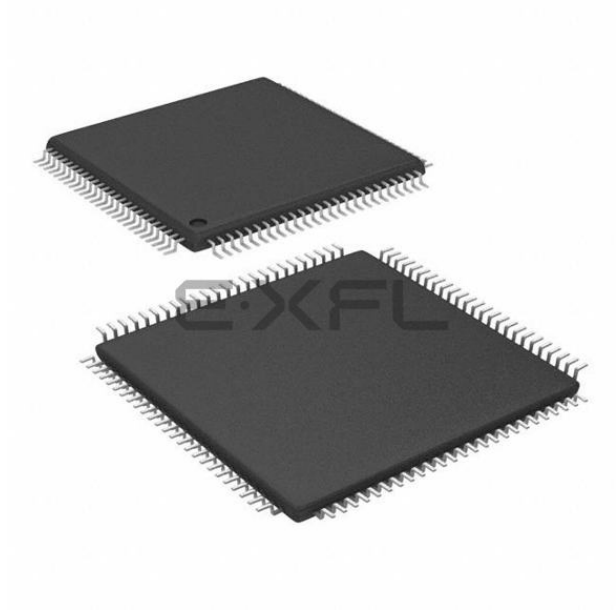
Microchip Technology - PIC24EP256GU810T-I/PF Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

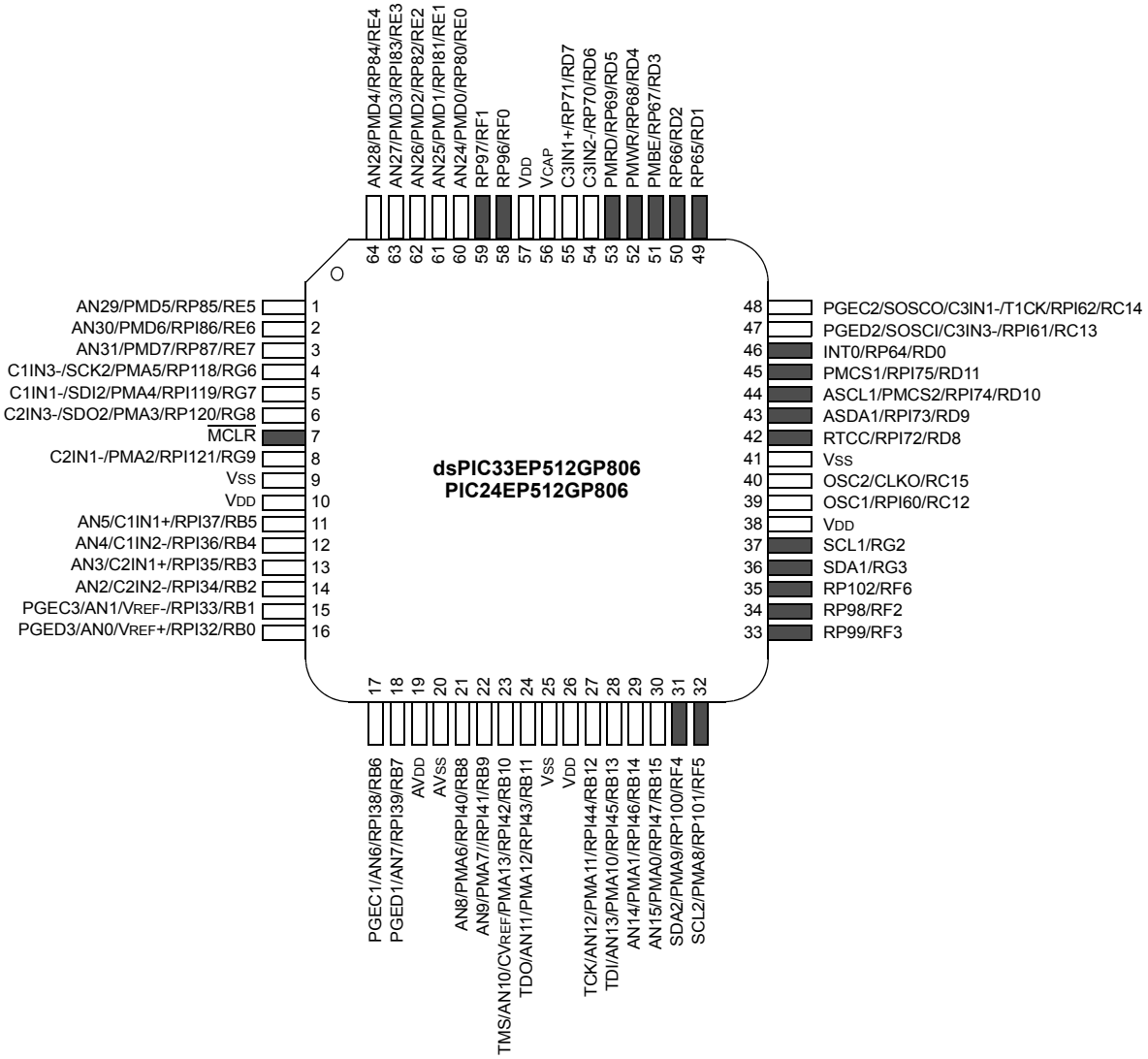
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	83
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep256gu810t-i-pf

Pin Diagrams (Continued)

64-Pin TQFP

■ = Pins are up to 5V tolerant



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The availability of I^2C™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

Pin Diagrams (Continued)

121-Pin TFBGA(1)

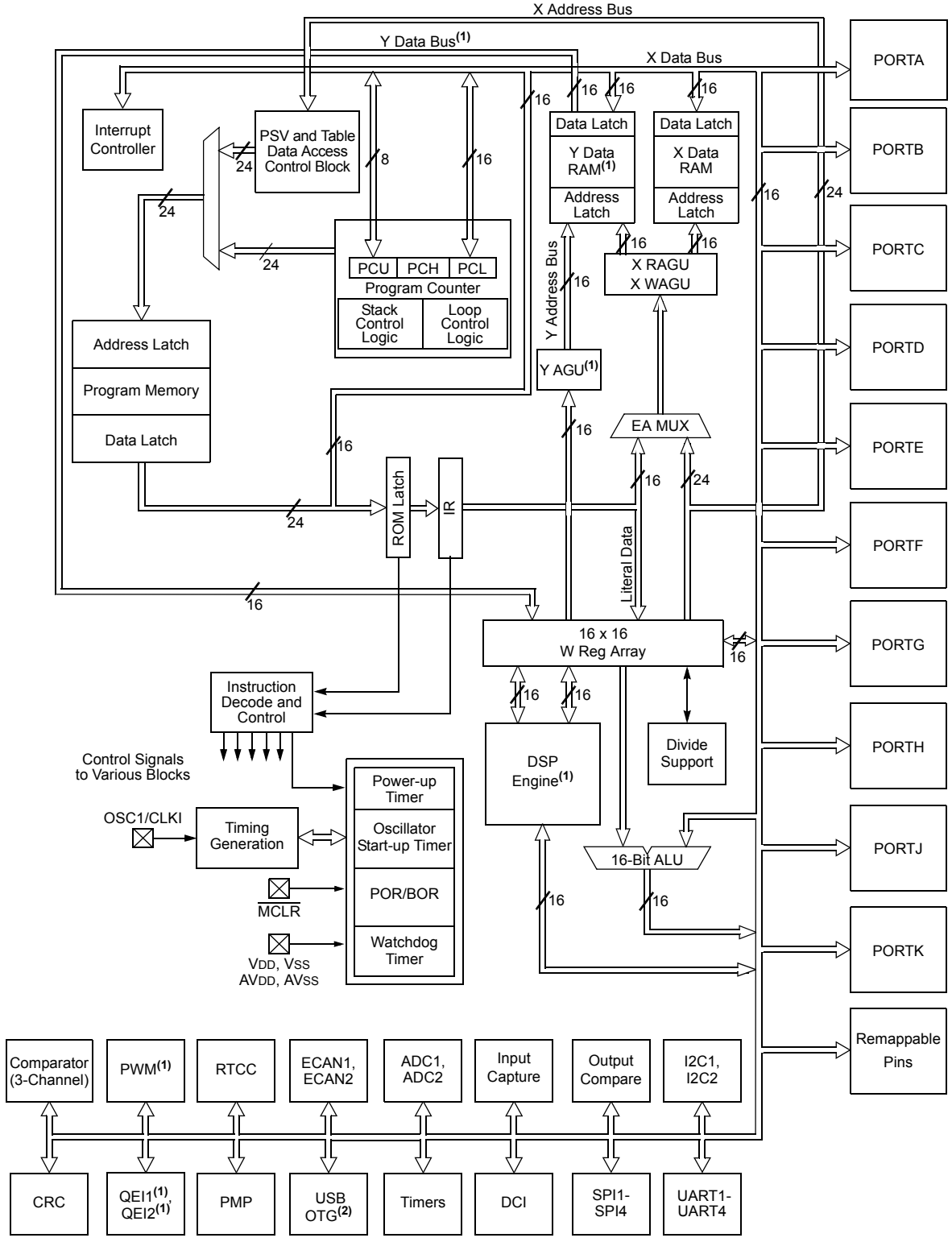
● = Pins are up to 5V tolerant

PIC24EP256GU810
PIC24EP512GU810

	1	2	3	4	5	6	7	8	9	10	11
A	RE4	RE3	RG13	RE0	RG0	RF1	VDD	NC	RD12	RD2	RD1
B	NC	RG15	RE2	RE1	RA7	RF0	VCAP	RD5	RD3	VSS	RC14
C	RE6	VDD	RG12	RG14	RA6	NC	RD7	RD4	NC	RC13	RD11
D	RC1	RE7	RE5	NC	NC	NC	RD6	RD13	RD0	NC	RD10
E	RC4	RC3	RG6	RC2	NC	RG1	NC	RA15	RD8	RD9	RA14
F	$\overline{\text{MCLR}}$	RG8	RG9	RG7	VSS	NC	NC	VDD	RC12	VSS	RC15
G	RE8	RE9	RA0	NC	VDD	VSS	VSS	NC	RA5	RA3	RA4
H	RB5	RB4	NC	NC	NC	VDD	NC	VBUS	VUSB3V3	RG2	RA2
J	RB3	RB2	RB7	AVDD	RB11	RA1	RB12	NC	NC	RF8	RG3
K	RB1	RB0	RA10	RB8	NC	RF12	RB14	VDD	RD15	RF3	RF2
L	RB6	RA9	AVSS	RB9	RB10	RF13	RB13	RB15	RD14	RF4	RF5

Note 1: Refer to Table 3 for full pin names.

FIGURE 1-1: dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 BLOCK DIAGRAM



Note 1: This feature or peripheral is only available on dsPIC33EPXXX(MC/MU)806/810/814 devices.

2: This feature or peripheral is only available on dsPIC33EPXXXMU806/810/814 and PIC24EPXXXGU806/810/814 devices.

TABLE 4-2: CPU CORE REGISTER MAP FOR PIC24EPXXX(GP/GU)810/814 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
W0	0000	W0 (WREG)																0000
W1	0002	W1																0000
W2	0004	W2																0000
W3	0006	W3																0000
W4	0008	W4																0000
W5	000A	W5																0000
W6	000C	W6																0000
W7	000E	W7																0000
W8	0010	W8																0000
W9	0012	W9																0000
W10	0014	W10																0000
W11	0016	W11																0000
W12	0018	W12																0000
W13	001A	W13																0000
W14	001C	W14																0000
W15	001E	W15																1000
SPLIM	0020	SPLIM																0000
PCL	002E	PCL															—	0000
PCH	0030	—	—	—	—	—	—	—	—	—	PCH							0000
DSRPAG	0032	—	—	—	—	—	—	DSRPAG<9:0>										0001
DSWPAG	0034	—	—	—	—	—	—	—	DSWPAG<8:0>									0001
RCOUNT	0036	RCOUNT<15:0>																0000
SR	0042	—	—	—	—	—	—	—	DC	IPL2	IPL1	IPL0	RA	N	OV	Z	C	0000
CORCON	0044	VAR	—	—	—	—	—	—	—	—	—	—	—	IPL3	SFA	—	—	0020
DISICNT	0052	—	—	DISICNT<13:0>														0000
TBLPAG	0054	—	—	—	—	—	—	—	—	TBLPAG<7:0>								0000
MSTRPR	0058	MSTRPR<15:0>																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-30: ECAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 1

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
—	0400-041E	See Table 4-28																—
C1BUFPNT1	0420	F3BP<3:0>				F2BP<3:0>				F1BP<3:0>				F0BP<3:0>				0000
C1BUFPNT2	0422	F7BP<3:0>				F6BP<3:0>				F5BP<3:0>				F4BP<3:0>				0000
C1BUFPNT3	0424	F11BP<3:0>				F10BP<3:0>				F9BP<3:0>				F8BP<3:0>				0000
C1BUFPNT4	0426	F15BP<3:0>				F14BP<3:0>				F13BP<3:0>				F12BP<3:0>				0000
C1RXM0SID	0430	SID<10:3>								SID<2:0>			—	MIDE	—	EID<17:16>		xxxx
C1RXM0EID	0432	EID<15:8>								EID<7:0>								xxxx
C1RXM1SID	0434	SID<10:3>								SID<2:0>			—	MIDE	—	EID<17:16>		xxxx
C1RXM1EID	0436	EID<15:8>								EID<7:0>								xxxx
C1RXM2SID	0438	SID<10:3>								SID<2:0>			—	MIDE	—	EID<17:16>		xxxx
C1RXM2EID	043A	EID<15:8>								EID<7:0>								xxxx
C1RXF0SID	0440	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF0EID	0442	EID<15:8>								EID<7:0>								xxxx
C1RXF1SID	0444	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF1EID	0446	EID<15:8>								EID<7:0>								xxxx
C1RXF2SID	0448	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF2EID	044A	EID<15:8>								EID<7:0>								xxxx
C1RXF3SID	044C	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF3EID	044E	EID<15:8>								EID<7:0>								xxxx
C1RXF4SID	0450	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF4EID	0452	EID<15:8>								EID<7:0>								xxxx
C1RXF5SID	0454	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF5EID	0456	EID<15:8>								EID<7:0>								xxxx
C1RXF6SID	0458	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF6EID	045A	EID<15:8>								EID<7:0>								xxxx
C1RXF7SID	045C	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF7EID	045E	EID<15:8>								EID<7:0>								xxxx
C1RXF8SID	0460	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF8EID	0462	EID<15:8>								EID<7:0>								xxxx
C1RXF9SID	0464	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF9EID	0466	EID<15:8>								EID<7:0>								xxxx
C1RXF10SID	0468	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF10EID	046A	EID<15:8>								EID<7:0>								xxxx
C1RXF11SID	046C	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-42: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXX(MC/MU)806 DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR35	06E6	—	IC14R<6:0>							—	IC13R<6:0>							0000
RPINR36	06E8	—	IC16R<6:0>							—	IC15R<6:0>							0000
RPINR37	06EA	—	SYNCI1R<6:0>							—	OCFCR<6:0>							0000
RPINR38	06EC	—	DTCMP1R<6:0>							—	SYNCI2R<6:0>							0000
RPINR39	06EE	—	DTCMP3R<6:0>							—	DTCMP2R<6:0>							0000
RPINR40	06F0	—	—	—	—	—	—	—	—	—	DTCMP4R<6:0>							0000
RPINR42	06F4	—	FLT6R<6:0>							—	FLT5R<6:0>							0000
RPINR43	06F6	—	—	—	—	—	—	—	—	—	FLT7R<6:0>							0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-54: DMAC REGISTER MAP (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
DMA4STAL	0B44	STA<15:0>																0000
DMA4STAH	0B46	—	—	—	—	—	—	—	—	STA<23:16>								0000
DMA4STBL	0B48	STB<15:0>																0000
DMA4STBH	0B4A	—	—	—	—	—	—	—	—	STB<23:16>								0000
DMA4PAD	0B4C	PAD<15:0>																0000
DMA4CNT	0B4E	—	—	CNT<13:0>														0000
DMA5CON	0B50	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000
DMA5REQ	0B52	FORCE	—	—	—	—	—	—	—	IRQSEL<7:0>								00FF
DMA5STAL	0B54	STA<15:0>																0000
DMA5STAH	0B56	—	—	—	—	—	—	—	—	STA<23:16>								0000
DMA5STBL	0B58	STB<15:0>																0000
DMA5STBH	0B5A	—	—	—	—	—	—	—	—	STB<23:16>								0000
DMA5PAD	0B5C	PAD<15:0>																0000
DMA5CNT	0B5E	—	—	CNT<13:0>														0000
DMA6CON	0B60	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000
DMA6REQ	0B62	FORCE	—	—	—	—	—	—	—	IRQSEL<7:0>								00FF
DMA6STAL	0B64	STA<15:0>																0000
DMA6STAH	0B66	—	—	—	—	—	—	—	—	STA<23:16>								0000
DMA6STBL	0B68	STB<15:0>																0000
DMA6STBH	0B6A	—	—	—	—	—	—	—	—	STB<23:16>								0000
DMA6PAD	0B6C	PAD<15:0>																0000
DMA6CNT	0B6E	—	—	CNT<13:0>														0000
DMA7CON	0B70	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000
DMA7REQ	0B72	FORCE	—	—	—	—	—	—	—	IRQSEL<7:0>								00FF
DMA7STAL	0B74	STA<15:0>																0000
DMA7STAH	0B76	—	—	—	—	—	—	—	—	STA<23:16>								0000
DMA7STBL	0B78	STB<15:0>																0000
DMA7STBH	0B7A	—	—	—	—	—	—	—	—	STB<23:16>								0000
DMA7PAD	0B7C	PAD<15:0>																0000
DMA7CNT	0B7E	—	—	CNT<13:0>														0000
DMA8CON	0B80	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE<1:0>		—	—	MODE<1:0>		0000
DMA8REQ	0B82	FORCE	—	—	—	—	—	—	—	IRQSEL<7:0>								00FF
DMA8STAL	0B84	STA<15:0>																0000
DMA8STAH	0B86	—	—	—	—	—	—	—	—	STA<23:16>								0000
DMA8STBL	0B88	STB<15:0>																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-71: PORTK REGISTER MAP FOR dsPIC33EPXXXMU814 AND PIC24EPXXXGU814 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISK	0E90	TRISK15	TRISK14	TRISK13	TRISK12	TRISK11	—	—	—	—	—	—	—	—	—	TRISK1	TRISK0	F803
PORTK	0E92	RK15	RK14	RK13	RK12	RK11	—	—	—	—	—	—	—	—	—	RK1	RK0	xxxx
LATK	0E94	LATK15	LATK14	LATK13	LATK12	LATK11	—	—	—	—	—	—	—	—	—	LATK1	LATK0	xxxx
ODCK	0E96	ODCK15	ODCK14	ODCK13	ODCK12	ODCK11	—	—	—	—	—	—	—	—	—	ODCK1	ODCK0	0000
CNENK	0E98	CNIEK15	CNIEK14	CNIEK13	CNIEK12	CNIEK11	—	—	—	—	—	—	—	—	—	CNIEK1	CNIEK0	0000
CNPUK	0E9A	CNPUK15	CNPUK14	CNPUK13	CNPUK12	CNPUK11	—	—	—	—	—	—	—	—	—	CNPUK1	CNPUK0	0000
CNPDK	0E9C	CNPDK15	CNPDK14	CNPDK13	CNPDK12	CNPDK11	—	—	—	—	—	—	—	—	—	CNPDK1	CNPDK0	0000
ANSELK	0E9E	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-72: PAD CONFIGURATION REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PADCFG1	0EFE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RTSECSEL	PMPTTL	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 8-14: DMAPPS: DMA PING-PONG STATUS REGISTER

U-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
—	PPST14	PPST13	PPST12	PPST11	PPST10	PPST9	PPST8
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **PPST14:** Channel 14 Ping-Pong Mode Status Flag bit
1 = DMASTB14 register selected
0 = DMASTA14 register selected

bit 13 **PPST13:** Channel 13 Ping-Pong Mode Status Flag bit
1 = DMASTB13 register selected
0 = DMASTA13 register selected

bit 12 **PPST12:** Channel 12 Ping-Pong Mode Status Flag bit
1 = DMASTB12 register selected
0 = DMASTA12 register selected

bit 11 **PPST11:** Channel 11 Ping-Pong Mode Status Flag bit
1 = DMASTB11 register selected
0 = DMASTA11 register selected

bit 10 **PPST10:** Channel 10 Ping-Pong Mode Status Flag bit
1 = DMASTB10 register selected
0 = DMASTA10 register selected

bit 9 **PPST9:** Channel 9 Ping-Pong Mode Status Flag bit
1 = DMASTB9 register selected
0 = DMASTA9 register selected

bit 8 **PPST8:** Channel 8 Ping-Pong Mode Status Flag bit
1 = DMASTB8 register selected
0 = DMASTA8 register selected

bit 7 **PPST7:** Channel 7 Ping-Pong Mode Status Flag bit
1 = DMASTB7 register selected
0 = DMASTA7 register selected

bit 6 **PPST6:** Channel 6 Ping-Pong Mode Status Flag bit
1 = DMASTB6 register selected
0 = DMASTA6 register selected

bit 5 **PPST5:** Channel 5 Ping-Pong Mode Status Flag bit
1 = DMASTB5 register selected
0 = DMASTA5 register selected

bit 4 **PPST4:** Channel 4 Ping-Pong Mode Status Flag bit
1 = DMASTB4 register selected
0 = DMASTA4 register selected

bit 3 **PPST3:** Channel 3 Ping-Pong Mode Status Flag bit
1 = DMASTB3 register selected
0 = DMASTA3 register selected

REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1 (CONTINUED)

bit 3 **SPI1MD:** SPI1 Module Disable bit
1 = SPI1 module is disabled
0 = SPI1 module is enabled

bit 2 **C2MD:** ECAN2 Module Disable bit
1 = ECAN2 module is disabled
0 = ECAN2 module is enabled

bit 1 **C1MD:** ECAN1 Module Disable bit
1 = ECAN1 module is disabled
0 = ECAN1 module is enabled

bit 0 **AD1MD:** ADC1 Module Disable bit
1 = ADC1 module is disabled
0 = ADC1 module is enabled

Note 1: This bit is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

REGISTER 10-6: PMD6: PERIPHERAL MODULE DISABLE CONTROL REGISTER 6

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	PWM7MD(1)	PWM6MD(1)	PWM5MD(1)	PWM4MD(1)	PWM3MD(1)	PWM2MD(1)	PWM1MD(1)
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	SPI4MD	SPI3MD
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **PWM7MD:** PWM7 Module Disable bit(1)
1 = PWM7 module is disabled
0 = PWM7 module is enabled

bit 13 **PWM6MD:** PWM6 Module Disable bit(1)
1 = PWM6 module is disabled
0 = PWM6 module is enabled

bit 12 **PWM5MD:** PWM5 Module Disable bit(1)
1 = PWM5 module is disabled
0 = PWM5 module is enabled

bit 11 **PWM4MD:** PWM4 Module Disable bit(1)
1 = PWM4 module is disabled
0 = PWM4 module is enabled

bit 10 **PWM3MD:** PWM3 Module Disable bit(1)
1 = PWM3 module is disabled
0 = PWM3 module is enabled

bit 9 **PWM2MD:** PWM2 Module Disable bit(1)
1 = PWM2 module is disabled
0 = PWM2 module is enabled

bit 8 **PWM1MD:** PWM1 Module Disable bit(1)
1 = PWM1 module is disabled
0 = PWM1 module is enabled

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **SPI4MD:** SPI4 Module Disable bit
1 = SPI4 module is disabled
0 = SPI4 module is enabled

bit 0 **SPI3MD:** SPI3 Module Disable bit
1 = SPI3 module is disabled
0 = SPI3 module is enabled

Note 1: This bit is available in dsPIC33EPXXX(MC/MU)806/810/814 devices only.

TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES

Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment
000 0000	I	Vss
000 0001	I	C1OUT(1)
000 0010	I	C2OUT(1)
000 0011	I	C3OUT(1)
000 0100	—	Reserved
000 0101	—	Reserved
000 0110	—	Reserved
000 0111	—	Reserved
000 1000	I	FINDX1(1)
000 1001	I	FHOME1(1)
000 1010	I	FINDX2(1)
000 1011	I	FHOME2(1)
000 1100	—	Reserved
000 1101	—	Reserved
000 1110	—	Reserved
000 1111	—	Reserved
001 0000	I	RPI16
001 0001	I	RPI17
001 0010	I	RPI18
001 0011	I	RPI19
001 0100	I	RPI20
001 0101	I	RPI21
001 0110	I	RPI22
001 0111	I	RPI23
001 1000	—	Reserved
001 1001	—	Reserved
001 1010	—	Reserved
001 1011	—	Reserved
001 1100	—	Reserved
001 1101	—	Reserved
001 1110	I	RPI30
001 1111	I	RPI31
010 0000	I	RPI32
010 0001	I	RPI33
010 0010	I	RPI34
010 0011	I	RPI35
010 0100	I	RPI36
010 0101	I	RPI37
010 0110	I	RPI38
010 0111	I	RPI39
010 1000	I	RPI40
010 1001	I	RPI41
010 1010	I	RPI42
010 1101	I	RPI45
010 1110	I	RPI46
010 1111	I	RPI47
011 0000	—	Reserved
011 0001	I	RPI49
011 0010	I	RPI50
011 0011	I	RPI51
011 0100	I	RPI52
011 0101	—	Reserved
011 0110	—	Reserved
011 0111	—	Reserved
011 1000	—	Reserved
011 1001	—	Reserved
011 1010	—	Reserved
011 1011	—	Reserved
011 1100	I	RPI60
011 1101	I	RPI61
011 1110	I	RPI62
011 1111	—	Reserved
100 0000	I/O	RP64
100 0001	I/O	RP65
100 0010	I/O	RP66
100 0011	I/O	RP67
100 0100	I/O	RP68
100 0101	I/O	RP69
100 0110	I/O	RP70
100 0111	I/O	RP71
100 1000	I	RPI72
100 1001	I	RPI73
100 1010	I	RPI74
100 1011	I	RPI75
100 1100	I	RPI76
100 1101	I	RPI77
100 1110	I	RPI78
100 1111	I/O	RP79
101 0000	I/O	RP80
101 0001	I	RPI81
101 0010	I/O	RP82
101 0011	I	RPI83
101 0100	I/O	RP84
101 0101	I/O	RP85
101 0110	I	RPI86
101 0111	I/O	RP87

Note 1: See **Section 11.4.4.2 “Virtual Connections”** for more information on selecting this pin assignment.

REGISTER 11-17: RPINR16: PERIPHERAL PIN SELECT INPUT REGISTER 16 (dsPIC33EPXXXMU806/810/814 DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	QEB2R<6:0>(1)						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	QEA2R<6:0>(1)						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **QEB2R<6:0>:** Assign B (QEI2) to the Corresponding RPn/RPIn Pin bits(1)
(see Table 11-2 for input pin selection numbers)
1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **QEA2R<6:0>:** Assign A (QEI2) to the Corresponding RPn/RPIn Pin bits(1)
(see Table 11-2 for input pin selection numbers)
1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

Note 1: These bits are available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

REGISTER 18-2: SPIxCON1: SPIx CONTROL REGISTER 1 (CONTINUED)

bit 4-2 **SPRE<2:0>:** Secondary Prescale bits (Master mode)(3)

111 = Secondary prescale 1:1
110 = Secondary prescale 2:1
•
•
•
000 = Secondary prescale 8:1

bit 1-0 **PPRE<1:0>:** Primary Prescale bits (Master mode)(3)

11 = Primary prescale 1:1
10 = Primary prescale 4:1
01 = Primary prescale 16:1
00 = Primary prescale 64:1

Note 1: The CKE bit is not used in the Framed SPIx modes. Program this bit to '0' for Framed SPIx modes (FRMEN = 1).

2: This bit must be cleared when FRMEN = 1.

3: Do not set both primary and secondary prescalers to a value of 1:1.

4: The SMP bit must be set only after setting the MSTEN bit. The SMP bit remains cleared if MSTEN = 0.

REGISTER 21-13: CxBUFPNT2: ECANx FILTER 4-7 BUFFER POINTER REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7BP<3:0>				F6BP<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F5BP<3:0>				F4BP<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **F7BP<3:0>:** RX Buffer Mask for Filter 7 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F6BP<3:0>:** RX Buffer Mask for Filter 6 bits (same values as bit 15-12)

bit 7-4 **F5BP<3:0>:** RX Buffer Mask for Filter 5 bits (same values as bit 15-12)

bit 3-0 **F4BP<3:0>:** RX Buffer Mask for Filter 4 bits (same values as bit 15-12)

REGISTER 21-14: CxBUFPNT3: ECANx FILTER 8-11 BUFFER POINTER REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F11BP<3:0>				F10BP<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F9BP<3:0>				F8BP<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **F11BP<3:0>:** RX Buffer Mask for Filter 11 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F10BP<3:0>:** RX Buffer Mask for Filter 10 bits (same values as bit 15-12)

bit 7-4 **F9BP<3:0>:** RX Buffer Mask for Filter 9 bits (same values as bit 15-12)

bit 3-0 **F8BP<3:0>:** RX Buffer Mask for Filter 8 bits (same values as bit 15-12)

FIGURE 33-9: TYPICAL FRC FREQUENCY @ VDD = 3.3V

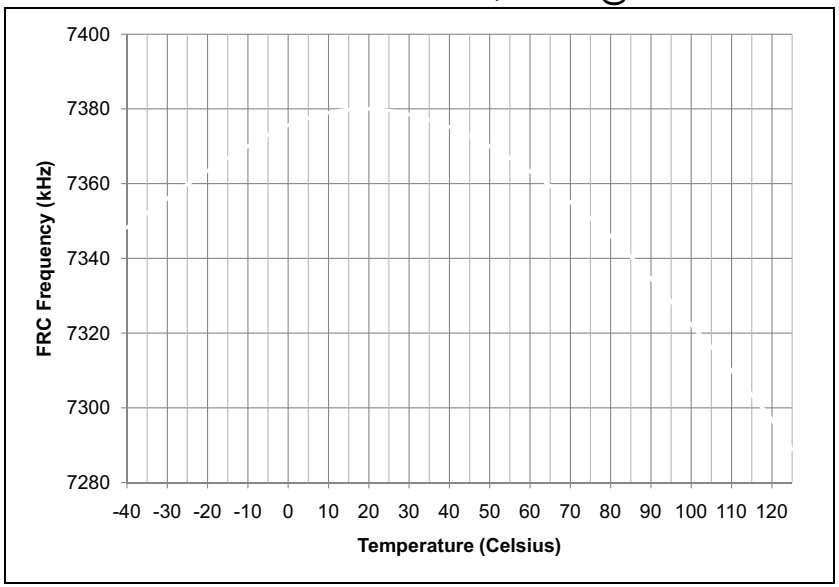
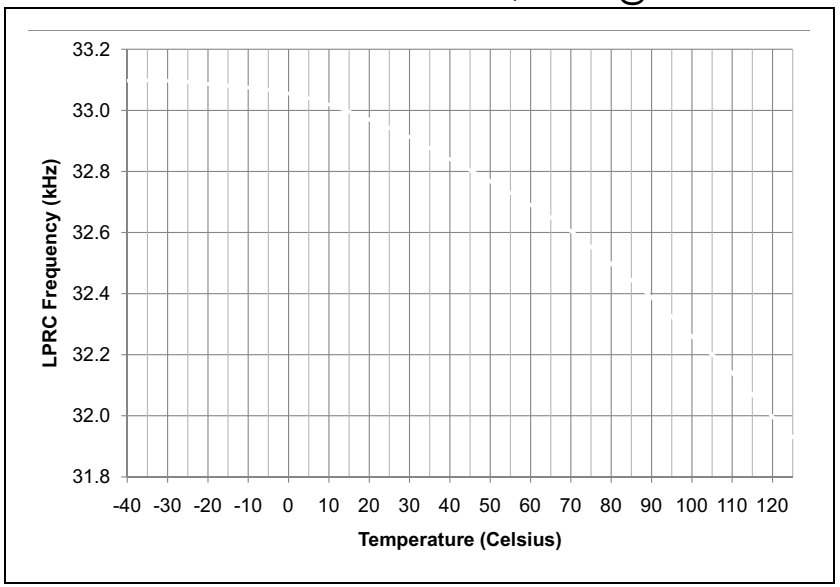
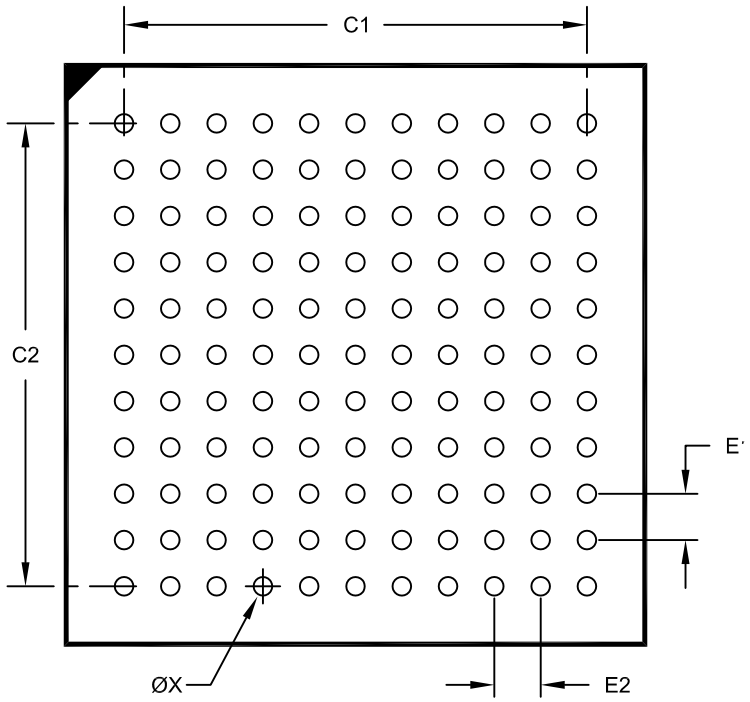


FIGURE 33-10: TYPICAL LPRC FREQUENCY @ VDD = 3.3V



121-Lead Plastic Thin Profile Ball Grid Array (BG) - 10x10x1.10 mm Body [TFBGA--Formerly XBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E1		0.80 BSC	
Contact Pitch	E2		0.80 BSC	
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Diameter (X121)	X			0.32

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2148 Rev D

Revision E (August 2011)

This revision includes the following updates to **Section 32.0 "Electrical Characteristics"**:

- The maximum HS value for parameter OS10 was updated (see Table 32-16)
- The OC/PWM Module Timing Characteristics for OCx were updated (see Figure 32-10)
- The Maximum Data Rate values were updated for the SPI1, SPI3, and SPI4 Maximum Data/Clock Rate Summary (see Table 32-33)
- These SPI1, SPI3, and SPI4 Timing Requirements were updated:
  - Maximum value for parameter SP10 and the minimum clock period value for SCKx in Note 3 (see Table 32-34, Table 32-35, and Table 32-36)
  - Maximum value for parameter SP70 and the minimum clock period value for SCKx in Note 3 (see Table 32-38 and Table 32-40)
- The Maximum Data Rate values were updated for the SPI2 Maximum Data/Clock Rate Summary (see Table 32-41)
- These SPI2 Timing Requirements were updated:
  - Maximum value for parameter SP10 and the minimum clock period value for SCKx in Note 3 (see Table 32-42, Table 32-43, and Table 32-44)
  - Maximum value for parameter SP70 and the minimum clock period value for SCKx in Note 3 (see Table 32-45 through Table 32-48)
  - Minimum value for parameters SP40 and SP41 see Table 32-43 through Table 32-48)
- These ADC Module Specifications were updated (see Table 32-54):
  - Minimum value for parameter AD05
  - Maximum value for parameter AD06
  - Minimum value for parameter AD07

NOTES: