# Microchip Technology - PIC24EP256GU814-E/PH Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 16-Bit |
| Speed | 60 MIPs |
| Connectivity | CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 122 |
| Program Memory Size | 256KB (85.5K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 12K x 16 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 32x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-TQFP |
| Supplier Device Package | 144-TQFP (16x16) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic24ep256gu814-e-ph |

**NOTES:**

**TABLE 4-3: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMU814 DEVICES ONLY (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IPC16 | 0860 | — | CRCIP<2:0> | | | — | U2EIP<2:0> | | | — | U1EIP<2:0> | | | — | — | — | — | 4440 |
| IPC17 | 0862 | — | C2TXIP<2:0> | | | — | C1TXIP<2:0> | | | — | DMA7IP<2:0> | | | — | DMA6IP<2:0> | | | 4444 |
| IPC18 | 0864 | — | QEI2IP<2:0> | | | — | — | — | — | — | PSESMIP<2:0> | | | — | — | — | — | 4040 |
| IPC20 | 0868 | — | U3TXIP<2:0> | | | — | U3RXIP<2:0> | | | — | U3EIP<2:0> | | | — | — | — | — | 4440 |
| IPC21 | 086A | — | U4EIP<2:0> | | | — | USB1IP<2:0> | | | — | — | — | — | — | — | — | — | 4400 |
| IPC22 | 086C | — | SPI3IP<2:0> | | | — | SPI3EIP<2:0> | | | — | U4TXIP<2:0> | | | — | U4RXIP<2:0> | | | 4444 |
| IPC23 | 086E | — | PWM2IP<2:0> | | | — | PWM1IP<2:0> | | | — | IC9IP<2:0> | | | — | OC9IP<2:0> | | | 4444 |
| IPC24 | 0870 | — | PWM6IP<2:0> | | | — | PWM5IP<2:0> | | | — | PWM4IP<2:0> | | | — | PWM3IP<2:0> | | | 4444 |
| IPC25 | 0872 | — | — | — | — | — | — | — | — | — | — | — | — | — | PWM7IP<2:0> | | | 0004 |
| IPC29 | 087A | — | DMA9IP<2:0> | | | — | DMA8IP<2:0> | | | — | — | — | — | — | — | — | — | 4400 |
| IPC30 | 087C | — | SPI4IP<2:0> | | | — | SPI4EIP<2:0> | | | — | DMA11IP<2:0> | | | — | DMA10IP<2:0> | | | 4444 |
| IPC31 | 087E | — | IC11IP<2:0> | | | — | OC11IP<2:0> | | | — | IC10IP<2:0> | | | — | OC10IP<2:0> | | | 4444 |
| IPC32 | 0880 | — | DMA13IP<2:0> | | | — | DMA12IP<2:0> | | | — | IC12IP<2:0> | | | — | OC12IP<2:0> | | | 4444 |
| IPC33 | 0882 | — | IC13IP<2:0> | | | — | OC13IP<2:0> | | | — | — | — | — | — | DMA14IP<2:0> | | | 4404 |
| IPC34 | 0884 | — | IC15IP<2:0> | | | — | OC15IP<2:0> | | | — | IC14IP<2:0> | | | — | OC14IP<2:0> | | | 4444 |
| IPC35 | 0886 | — | — | — | — | — | ICDIP<2:0> | | | — | IC16IP<2:0> | | | — | OC16IP<2:0> | | | 0444 |
| INTCON1 | 08C0 | NSTDIS | OVAERR | OVBERR | COVAERR | COVBERR | OVATE | OVBTE | COVTE | SFTACERR | DIV0ERR | DMACERR | MATHERR | ADDRERR | STKERR | OSCFAIL | — | 0000 |
| INTCON2 | 08C2 | GIE | DISI | SWTRAP | — | — | — | — | — | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP | 8000 |
| INTCON3 | 08C4 | — | — | — | — | — | — | — | — | — | UAE | DAE | DOOVR | — | — | — | — | 0000 |
| INTCON4 | 08C6 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SGHT | 0000 |
| INTTREG | 08C8 | — | — | — | — | ILR<3:0> | | | | VECNUM<7:0> | | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-54: DMAC REGISTER MAP (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DMA13CON | 0BD0 | CHEN | SIZE | DIR | HALF | NULLW | — | — | — | — | — | AMODE<1:0> | | — | — | MODE<1:0> | | 0000 |
| DMA13REQ | 0BD2 | FORCE | — | — | — | — | — | — | — | IRQSEL<7:0> | | | | | | | | 00FF |
| DMA13STAL | 0BD4 | STA<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA13STAH | 0BD6 | — | — | — | — | — | — | — | — | STA<23:16> | | | | | | | | 0000 |
| DMA13STBL | 0BD8 | STB<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA13STBH | 0BDA | — | — | — | — | — | — | — | — | STB<23:16> | | | | | | | | 0000 |
| DMA13PAD | 0BDC | PAD<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA13CNT | 0BDE | — | — | CNT<13:0> | | | | | | | | | | | | | | 0000 |
| DMA14CON | 0BE0 | CHEN | SIZE | DIR | HALF | NULLW | — | — | — | — | — | AMODE<1:0> | | — | — | MODE<1:0> | | 0000 |
| DMA14REQ | 0BE2 | FORCE | — | — | — | — | — | — | — | IRQSEL<7:0> | | | | | | | | 00FF |
| DMA14STAL | 0BE4 | STA<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA14STAH | 0BE6 | — | — | — | — | — | — | — | — | STA<23:16> | | | | | | | | 0000 |
| DMA14STBL | 0BE8 | STB<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA14STBH | 0BEA | — | — | — | — | — | — | — | — | STB<23:16> | | | | | | | | 0000 |
| DMA14PAD | 0BEC | PAD<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA14CNT | 0BEE | — | — | CNT<13:0> | | | | | | | | | | | | | | 0000 |
| DMAPWC | 0BF0 | — | PWCOL14 | PWCOL13 | PWCOL12 | PWCOL11 | PWCOL10 | PWCOL9 | PWCOL8 | PWCOL7 | PWCOL6 | PWCOL5 | PWCOL4 | PWCOL3 | PWCOL2 | PWCOL1 | PWCOL0 | 0000 |
| DMARQC | 0BF2 | — | RQCOL14 | RQCOL13 | RQCOL12 | RQCOL11 | RQCOL10 | RQCOL9 | RQCOL8 | RQCOL7 | RQCOL6 | RQCOL5 | RQCOL4 | RQCOL3 | RQCOL2 | RQCOL1 | RQCOL0 | 0000 |
| DMAPPS | 0BF4 | — | PPST14 | PPST13 | PPST12 | PPST11 | PPST10 | PPST9 | PPST8 | PPST7 | PPST6 | PPST5 | PPST4 | PPST3 | PPST2 | PPST1 | PPST0 | 0000 |
| DMALCA | 0BF6 | — | — | — | — | — | — | — | — | — | — | — | — | LSTCH<3:0> | | | | 000F |
| DSADRL | 0BF8 | DSADR<15:0> | | | | | | | | | | | | | | | | 0000 |
| DSADRH | 0BFA | — | — | — | — | — | — | — | — | DSADR<23:16> | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-58: PORTC REGISTER MAP FOR dsPIC33EPXXX(GP/MC/MU)806 AND PIC24EPXXXGP806 DEVICES ONLY**

| File Name | Addr, | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISC | 0E20 | TRISC15 | TRISC14 | TRISC13 | TRISC12 | — | — | — | — | — | — | — | — | — | — | — | — | F000 |
| PORTC | 0E22 | RC15 | RC14 | RC13 | RC12 | — | — | — | — | — | — | — | — | — | — | — | — | xxxx |
| LATC | 0E24 | LATC15 | LATC14 | LATC13 | LATC12 | — | — | — | — | — | — | — | — | — | — | — | — | xxxx |
| ODCC | 0E26 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| CNENC | 0E28 | CNIEC15 | CNIEC14 | CNIEC13 | CNIEC12 | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| CNPUC | 0E2A | CNPUC15 | CNPUC14 | CNPUC13 | CNPUC12 | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| CNPDC | 0E2C | CNPDC15 | CNPDC14 | CNPDC13 | CNPDC12 | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| ANSELC | 0E2E | — | ANSC14 | ANSC13 | — | — | — | — | — | — | — | — | — | — | — | — | — | 6000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-59: PORTD REGISTER MAP FOR dsPIC33EPXXXMU810/814 AND PIC24EPXXXGU810/814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISD | 0E30 | TRISD15 | TRISD14 | TRISD13 | TRISD12 | TRISD11 | TRISD10 | TRISD9 | TRISD8 | TRISD7 | TRISD6 | TRISD5 | TRISD4 | TRISD3 | TRISD2 | TRISD1 | TRISD0 | FFFF |
| PORTD | 0E32 | RD15 | RD14 | RD13 | RD12 | RD11 | RD10 | RD9 | RD8 | RD7 | RD6 | RD5 | RD4 | RD3 | RD2 | RD1 | RD0 | xxxx |
| LATD | 0E34 | LATD15 | LATD14 | LATD13 | LATD12 | LATD11 | LATD10 | LATD9 | LATD8 | LATD7 | LATD6 | LATD5 | LATD4 | LATD3 | LATD2 | LATD1 | LATD0 | xxxx |
| ODCD | 0E36 | ODCD15 | ODCD14 | ODCD13 | ODCD12 | ODCD11 | ODCD10 | ODCD9 | ODCD8 | — | — | ODCD5 | ODCD4 | ODCD3 | ODCD2 | ODCD1 | ODCD0 | 0000 |
| CNEND | 0E38 | CNIED15 | CNIED14 | CNIED13 | CNIED12 | CNIED11 | CNIED10 | CNIED9 | CNIED8 | CNIED7 | CNIED6 | CNIED5 | CNIED4 | CNIED3 | CNIED2 | CNIED1 | CNIED0 | 0000 |
| CNPUD | 0E3A | CNPUD15 | CNPUD14 | CNPUD13 | CNPUD12 | CNPUD11 | CNPUD10 | CNPUD9 | CNPUD8 | CNPUD7 | CNPUD6 | CNPUD5 | CNPUD4 | CNPUD3 | CNPUD2 | CNPUD1 | CNPUD0 | 0000 |
| CNPDD | 0E3C | CNPDD15 | CNPDD14 | CNPDD13 | CNPDD12 | CNPDD11 | CNPDD10 | CNPDD9 | CNPDD8 | CNPDD7 | CNPDD6 | CNPDD5 | CNPDD4 | CNPDD3 | CNPDD2 | CNPDD1 | CNPDD0 | 0000 |
| ANSELD | 0E3E | — | — | — | — | — | — | — | — | ANSD7 | ANSD6 | — | — | — | — | — | — | 00C0 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-60: PORTD REGISTER MAP FOR dsPIC33EPXXX(GP/MC/MU)806 AND PIC24EPXXXGP806 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISD | 0E30 | — | — | — | — | TRISD11 | TRISD10 | TRISD9 | TRISD8 | TRISD7 | TRISD6 | TRISD5 | TRISD4 | TRISD3 | TRISD2 | TRISD1 | TRISD0 | 0FFF |
| PORTD | 0E32 | — | — | — | — | RD11 | RD10 | RD9 | RD8 | RD7 | RD6 | RD5 | RD4 | RD3 | RD2 | RD1 | RD0 | xxxx |
| LATD | 0E34 | — | — | — | — | LATD11 | LATD10 | LATD9 | LATD8 | LATD7 | LATD6 | LATD5 | LATD4 | LATD3 | LATD2 | LATD1 | LATD0 | xxxx |
| ODCD | 0E36 | — | — | — | — | ODCD11 | ODCD10 | ODCD9 | ODCD8 | — | — | ODCD5 | ODCD4 | ODCD3 | ODCD2 | ODCD1 | ODCD0 | 0000 |
| CNEND | 0E38 | — | — | — | — | CNIED11 | CNIED10 | CNIED9 | CNIED8 | CNIED7 | CNIED6 | CNIED5 | CNIED4 | CNIED3 | CNIED2 | CNIED1 | CNIED0 | 0000 |
| CNPUD | 0E3A | — | — | — | — | CNPUD11 | CNPUD10 | CNPUD9 | CNPUD8 | CNPUD7 | CNPUD6 | CNPUD5 | CNPUD4 | CNPUD3 | CNPUD2 | CNPUD1 | CNPUD0 | 0000 |
| CNPDD | 0E3C | — | — | — | — | CNPDD11 | CNPDD10 | CNPDD9 | CNPDD8 | CNPDD7 | CNPDD6 | CNPDD5 | CNPDD4 | CNPDD3 | CNPDD2 | CNPDD1 | CNPDD0 | 0000 |
| ANSELD | 0E3E | — | — | — | — | — | — | — | — | ANSD7 | ANSD6 | — | — | — | — | — | — | 00C0 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**REGISTER 10-3: PMD3: PERIPHERAL MODULE DISABLE CONTROL REGISTER 3**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| T9MD | T8MD | T7MD | T6MD | — | CMPMD | RTCCMD | PMPMD |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | U-0 | R/W-0 | U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CRCMD | — | QEI2MD(1) | — | U3MD | — | I2C2MD | AD2MD |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **T9MD:** Timer9 Module Disable bit
1 = Timer9 module is disabled
0 = Timer9 module is enabled

bit 14 **T8MD:** Timer8 Module Disable bit
1 = Timer8 module is disabled
0 = Timer8 module is enabled

bit 13 **T7MD:** Timer7 Module Disable bit
1 = Timer7 module is disabled
0 = Timer7 module is enabled

bit 12 **T6MD:** Timer6 Module Disable bit
1 = Timer6 module is disabled
0 = Timer6 module is enabled

bit 11 **Unimplemented:** Read as '0'

bit 10 **CMPMD:** Comparator Module Disable bit
1 = Comparator module is disabled
0 = Comparator module is enabled

bit 9 **RTCCMD:** RTCC Module Disable bit
1 = RTCC module is disabled
0 = RTCC module is enabled

bit 8 **PMPMD:** PMP Module Disable bit
1 = PMP module is disabled
0 = PMP module is enabled

bit 7 **CRCMD:** CRC Module Disable bit
1 = CRC module is disabled
0 = CRC module is enabled

bit 6 **Unimplemented:** Read as '0'

bit 5 **QEI2MD:** QEI2 Module Disable bit(1)
1 = QEI2 module is disabled
0 = QEI2 module is enabled

bit 4 **Unimplemented:** Read as '0'

bit 3 **U3MD:** UART3 Module Disable bit
1 = UART3 module is disabled
0 = UART3 module is enabled

bit 2 **Unimplemented:** Read as '0'

**Note 1:** This bit is available in dsPIC33EPXXX(MC/MU)806/810/814 devices only.

**REGISTER 15-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 HS | R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL<4:0> | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HS = Hardware Settable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **FLTMD:** Fault Mode Select bit
- 1 = Fault mode is maintained until the Fault source is removed; the corresponding OCFLTx bit is cleared in software and a new PWM period starts
- 0 = Fault mode is maintained until the Fault source is removed and a new PWM period starts

bit 14 **FLTOUT:** Fault Out bit
- 1 = PWM output is driven high on a Fault
- 0 = PWM output is driven low on a Fault

bit 13 **FLTTRIEN:** Fault Output State Select bit
- 1 = OCx pin is tri-stated on Fault condition
- 0 = OCx pin I/O state defined by FLTOUT bit on Fault condition

bit 12 **OCINV:** OCMP Invert bit
- 1 = OCx output is inverted
- 0 = OCx output is not inverted

bit 11-9 **Unimplemented:** Read as '0'

bit 8 **OC32:** Cascade Two OCx Modules Enable bit (32-bit operation)
- 1 = Cascade module operation is enabled
- 0 = Cascade module operation is disabled

bit 7 **OCTRIG:** OCx Trigger/Sync Select bit
- 1 = Triggers OCx from source designated by SYNCSELx bits
- 0 = Synchronizes OCx with source designated by SYNCSELx bits

bit 6 **TRIGSTAT:** Timer Trigger Status bit
- 1 = Timer source has been triggered and is running
- 0 = Timer source has not been triggered and is being held clear

bit 5 **OCTRIS:** OCx Output Pin Direction Select bit
- 1 = OCx is tri-stated
- 0 = Output compare module drives the OCx pin

**Note 1:** Do not use the OCx module as its own Sync or Trigger source.

**2:** When the OCy module is turned OFF, it sends a trigger out signal. If the OCx module uses the OCy module as a Trigger source, the OCy module must be unselected as a Trigger source prior to disabling it.

**REGISTER 16-11: PWMCONx: PWMx CONTROL REGISTER**

| HSC-0 | HSC-0 | HSC-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| FLTSTAT(1) | CLSTAT(1) | TRGSTAT | FLTIEN | CLIEN | TRGIEN | ITB(2) | MDCS(2) |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| DTC<1:0> | | DTCP(3) | — | MTBS | CAM(2,4) | XPRES(5) | IUE(2) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HSC = Set or Cleared in Hardware | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **FLTSTAT:** Fault Interrupt Status bit(1)
1 = Fault interrupt is pending
0 = No Fault interrupt is pending
This bit is cleared by setting FLTIEN = 0.

bit 14 **CLSTAT:** Current-Limit Interrupt Status bit(1)
1 = Current-limit interrupt is pending
0 = No current-limit interrupt is pending
This bit is cleared by setting CLIEN = 0.

bit 13 **TRGSTAT:** Trigger Interrupt Status bit
1 = Trigger interrupt is pending
0 = No trigger interrupt is pending
This bit is cleared by setting TRGIEN = 0.

bit 12 **FLTIEN:** Fault Interrupt Enable bit
1 = Fault interrupt is enabled
0 = Fault interrupt is disabled and FLTSTAT bit is cleared

bit 11 **CLIEN:** Current-Limit Interrupt Enable bit
1 = Current-limit interrupt is enabled
0 = Current-limit interrupt is disabled and CLSTAT bit is cleared

bit 10 **TRGIEN:** Trigger Interrupt Enable bit
1 = A trigger event generates an interrupt request
0 = Trigger event interrupts are disabled and TRGSTAT bit is cleared

bit 9 **ITB:** Independent Time Base Mode bit(2)
1 = PHASEx/SPHASEx registers provide time base period for this PWM generator
0 = PTPER register provides timing for this PWM generator

bit 8 **MDCS:** Master Duty Cycle Register Select bit(2)
1 = MDC register provides duty cycle information for this PWM generator
0 = PDCx and SDCx registers provide duty cycle information for this PWM generator

**Note 1:** Software must clear the interrupt status here and in the corresponding IFS bit in the interrupt controller.
**2:** These bits should not be changed after the PWM is enabled (PTEN = 1).
**3:** DTC<1:0> = 11 for DTCP to be effective; otherwise, DTCP is ignored.
**4:** The Independent Time Base (ITB = 1) mode must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
**5:** To operate in External Period Reset mode, the ITB bit must be '1' and the CLMOD bit in the FCLCONx register must be '0'.

**REGISTER 19-3: I2CxMSK: I2Cx SLAVE MODE ADDRESS MASK REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | AMSK9 | AMSK8 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| AMSK7 | AMSK6 | AMSK5 | AMSK4 | AMSK3 | AMSK2 | AMSK1 | AMSK0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **AMSKx:** Mask for Address bit x Select bit

For 10-Bit Address:

1 = Enables masking for bit Ax of incoming message address; bit match is not required in this position

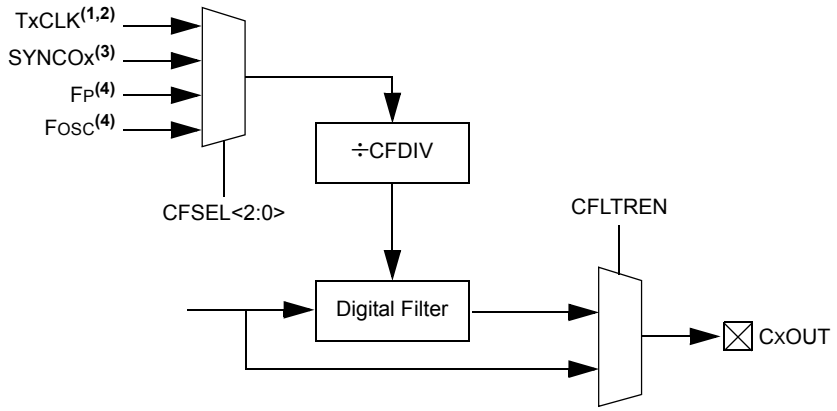
0 = Disables masking for bit Ax; bit match is required in this position

For 7-Bit Address (I2CxMSK<6:0> only):

1 = Enables masking for bit Ax + 1 of incoming message address; bit match is not required in this position

0 = Disable masking for bit Ax + 1; bit match is required in this position

**FIGURE 25-4: DIGITAL FILTER INTERCONNECT BLOCK DIAGRAM**




**Note 1:** See the Type C Timer Block Diagram (Figure 13-2).

**2:** See the Type B Timer Block Diagram (Figure 13-1).

**3:** See the PWM Module Register Interconnect Diagram (Figure 16-2).

**4:** See the Oscillator System Diagram (Figure 9-1).

## 25.1 Comparator Resources

Many useful resources related to the Comparator are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310 |

### 25.1.1 KEY RESOURCES

- **Section 26. "Op Amp/Comparator"** (DS70357) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

**REGISTER 25-3: CMxMSKSRC: COMPARATOR x MASK SOURCE SELECT CONTROL REGISTER**

| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | RW-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | SELSRCC<3:0> | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SELSRCB<3:0> | | | | SELSRCA<3:0> | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-12 **Unimplemented:** Read as ‘0’

bit 11-8 **SELSRCC<3:0>:** Mask C Input Select bits
1111 = FLT4
1110 = FLT2
1101 = PWM7H
1100 = PWM7L
1011 = PWM6H
1010 = PWM6L
1001 = PWM5H
1000 = PWM5L
0111 = PWM4H
0110 = PWM4L
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

bit 7-4 **SELSRCB<3:0>:** Mask B Input Select bits
1111 = FLT4
1110 = FLT2
1101 = PWM7H
1100 = PWM7L
1011 = PWM6H
1010 = PWM6L
1001 = PWM5H
1000 = PWM5L
0111 = PWM4H
0110 = PWM4L
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

**REGISTER 28-2: PMMODE: PARALLEL MASTER PORT MODE REGISTER (CONTINUED)**

bit 1-0 **WAITE<1:0>:** Data Hold After Strobe Wait State Configuration bits(1,2,3)

11 = Wait of 4 TP
10 = Wait of 3 TP
01 = Wait of 2 TP
00 = Wait of 1 TP

**Note 1:** The applied Wait state depends on whether data and address are multiplexed or demultiplexed. See **Section 28.4.1.8. "Wait States"** in **Section 28. "Parallel Master Port (PMP)"** (DS70576) in the *"dsPIC33E/PIC24E Family Reference Manual"* for more information.

**2:** WAITB<1:0> and WAITE<1:0> bits are ignored whenever WAITM<3:0> = 0000.

**3:** TP = 1/FP.

**TABLE 29-2: CONFIGURATION BITS DESCRIPTION**

| Bit Field | Register | RTSP Effect | Description |
|---|---|---|---|
| GSSK<1:0> | FGS | Immediate | General Segment Key bits<br>These bits must be set to '00' if GWRP = 1 and GSS = 1. These bits must be set to '11' for any other value of the GWRP and GSS bits.<br>Any mismatch between either the GWRP or GSS bits, and the GSSK bits (as described above), will result in code protection becoming enabled for the General Segment. A Flash bulk erase will be required to unlock the device. |
| GSS | FGS | Immediate | General Segment Code-Protect bit<br>1 = User program memory is not code-protected<br>0 = User program memory is code-protected |
| GWRP | FGS | Immediate | General Segment Write-Protect bit<br>1 = User program memory is not write-protected<br>0 = User program memory is write-protected |
| IESO | FOSCSEL | Immediate | Two-Speed Oscillator Start-up Enable bit<br>1 = Start-up device with FRC, then automatically switch to the user-selected oscillator source when ready<br>0 = Start-up device with user-selected oscillator source |
| FNOSC<2:0> | FOSCSEL | If clock switch is enabled, the RTSP effect is on any device Reset; otherwise, immediate | Initial Oscillator Source Selection bits<br>111 = Internal Fast RC (FRC) Oscillator with Postscaler<br>110 = Internal Fast RC (FRC) Oscillator with Divide-by-16<br>101 = LPRC Oscillator<br>100 = Secondary (LP) Oscillator<br>011 = Primary (XT, HS, EC) Oscillator with PLL<br>010 = Primary (XT, HS, EC) Oscillator<br>001 = Internal Fast RC (FRC) Oscillator with PLL<br>000 = FRC Oscillator |
| FCKSM<1:0> | FOSC | Immediate | Clock Switching Mode bits<br>1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled<br>01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled<br>00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled |
| IOL1WAY | FOSC | Immediate | Peripheral Pin Select Configuration bit<br>1 = Allows only one reconfiguration<br>0 = Allows multiple reconfigurations |
| OSCIOFNC | FOSC | Immediate | OSC2 Pin Function bit (except in XT and HS modes)<br>1 = OSC2 is the clock output<br>0 = OSC2 is the general purpose digital I/O pin |
| POSCMD<1:0> | FOSC | Immediate | Primary Oscillator Mode Select bits<br>11 = Primary Oscillator is disabled<br>10 = HS Crystal Oscillator mode<br>01 = XT Crystal Oscillator mode<br>00 = EC (External Clock) mode |
| FWDTEN | FWDT | Immediate | Watchdog Timer Enable bit<br>1 = Watchdog Timer is always enabled (LPRC Oscillator cannot be disabled. Clearing the SWDTEN bit in the RCON register has no effect.)<br>0 = Watchdog Timer is enabled/disabled by user software (LPRC can be disabled by clearing the SWDTEN bit in the RCON register.) |

**Note 1:** BOR should always be enabled for proper operation (BOREN = 1).

**2:** This register can only be modified when code protection and write protection are disabled for both the General and Auxiliary Segments (APL = 1, AWRP = 1, APLK = 0, GSS = 1, GWRP = 1 and GSSK = 0).

**TABLE 29-2: CONFIGURATION BITS DESCRIPTION (CONTINUED)**

| Bit Field | Register | RTSP Effect | Description |
|---|---|---|---|
| WINDIS | FWDT | Immediate | Watchdog Timer Window Enable bit<br>1 = Watchdog Timer is in Non-Window mode<br>0 = Watchdog Timer is in Window mode |
| PLLKEN | FWDT | Immediate | PLL Lock Wait Enable bit<br>1 = Clock switches to the PLL source will wait until the PLL lock signal is valid<br>0 = Clock switch will not wait for PLL lock |
| WDTPRE | FWDT | Immediate | Watchdog Timer Prescaler bit<br>1 = 1:128<br>0 = 1:32 |
| APLK<1:0> | FAS(2) | Immediate | Auxiliary Segment Key bits<br>These bits must be set to '00' if AWRP = 1 and APL = 1. These bits must be set to '11' for any other value of the AWRP and APL bits.<br>Any mismatch between either the AWRP or APL bits and the APLK bits (as described above), will result in code protection becoming enabled for the Auxiliary Segment. A Flash bulk erase will be required to unlock the device. |
| APL | FAS(2) | Immediate | Auxiliary Segment Code-Protect bit<br>1 = Auxiliary program memory is not code-protected<br>0 = Auxiliary program memory is code-protected |
| AWRP | FAS(2) | Immediate | Auxiliary Segment Write-Protect bit<br>1 = Auxiliary program memory is not write-protected<br>0 = Auxiliary program memory is write-protected |
| WDTPOST<3:0> | FWDT | Immediate | Watchdog Timer Postscaler bits<br>1111 = 1:32,768<br>1110 = 1:16,384<br>•<br>•<br>•<br>0001 = 1:2<br>0000 = 1:1 |
| FPWRT<2:0> | FPOR | Immediate | Power-on Reset Timer Value Select bits<br>111 = PWRT = 128 ms<br>110 = PWRT = 64 ms<br>101 = PWRT = 32 ms<br>100 = PWRT = 16 ms<br>011 = PWRT = 8 ms<br>010 = PWRT = 4 ms<br>001 = PWRT = 2 ms<br>000 = PWRT = Disabled |
| BOREN(1) | FPOR | Immediate | Brown-out Reset (BOR) Detection Enable bit<br>1 = BOR is enabled<br>0 = BOR is disabled |
| ALTI2C2 | FPOR | Immediate | Alternate $I^2C$™ pins for I2C2 bit<br>1 = I2C2 is mapped to the SDA2/SCL2 pins<br>0 = I2C2 is mapped to the ASDA2/ASCL2 pins |
| ALTI2C1 | FPOR | Immediate | Alternate $I^2C$ pins for I2C1 bit<br>1 = I2C1 is mapped to the SDA1/SCL1 pins<br>0 = I2C1 is mapped to the ASDA1/ASCL1 pins |

**Note 1:** BOR should always be enabled for proper operation (BOREN = 1).

**2:** This register can only be modified when code protection and write protection are disabled for both the General and Auxiliary Segments (APL = 1, AWRP = 1, APLK = 0, GSS = 1, GWRP = 1 and GSSK = 0).

## 29.5 JTAG Interface

dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices implement a JTAG interface, which supports boundary scan device testing. Detailed information on this interface is provided in future revisions of the document.

**Note:** Refer to **Section 24. "Programming and Diagnostics"** (DS70608) of the *"dsPIC33E/PIC24E Family Reference Manual"* for further information on usage, configuration and operation of the JTAG interface.

## 29.6 In-Circuit Serial Programming

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices can be serially programmed while in the end application circuit. This is done with two lines for clock and data, and three other lines for power, ground and the programming sequence. Serial programming allows customers to manufacture boards with unprogrammed devices and then program the digital signal controller just before shipping the product. Serial programming also allows the most recent firmware or a custom firmware to be programmed. Refer to the *"dsPIC33E/PIC24E Flash Programming Specification"* (DS70619) for details about In-Circuit Serial Programming (ICSP).

Any of the three pairs of programming clock/data pins can be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

## 29.7 In-Circuit Debugger

When MPLAB® ICD 3 or REAL ICE™ is selected as a debugger, the in-circuit debugging functionality is enabled. This function allows simple debugging functions when used with MPLAB IDE. Debugging functionality is controlled through the PGECx (Emulation/Debug Clock) and PGEDx (Emulation/Debug Data) pin functions.

Any of the three pairs of debugging clock/data pins can be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

To use the in-circuit debugger function of the device, the design must implement ICSP connections to $\overline{MCLR}$, $V_{DD}$, $V_{SS}$ and the PGECx/PGEDx pin pair. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two I/O pins.

## 29.8 Code Protection and CodeGuard™ Security

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices offer basic implementation of CodeGuard Security that supports only General Segment (GS) security. This feature helps protect individual Intellectual Property in collaborative system designs.

When coupled with software encryption libraries, CodeGuard Security can be used to securely update Flash even when multiple IPs reside on the single chip. The code protection features vary depending on the actual dsPIC33E implemented. The following sections provide an overview of these features.

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices do not support Boot Segment (BS), Secure Segment (SS) and RAM protection.

**Note:** Refer to **Section 23. "CodeGuard™ Security"** (DS70634) of the *"dsPIC33E/PIC24E Family Reference Manual"* for further information on usage, configuration and operation of CodeGuard Security.

**FIGURE 32-5: BOR AND MASTER CLEAR RESET TIMING CHARACTERISTICS**

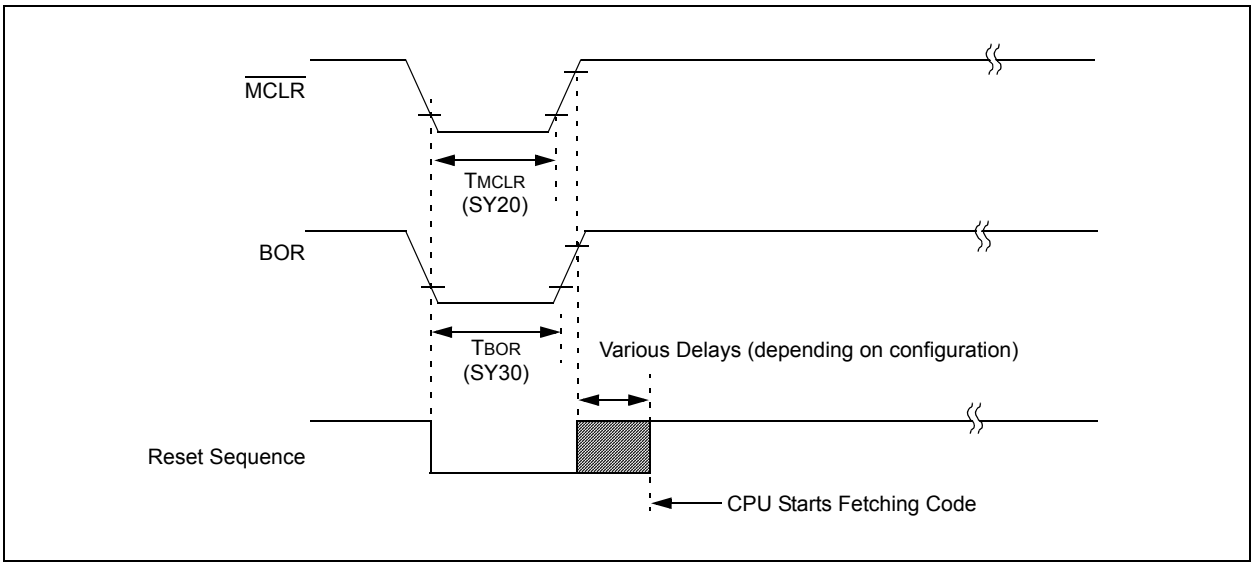
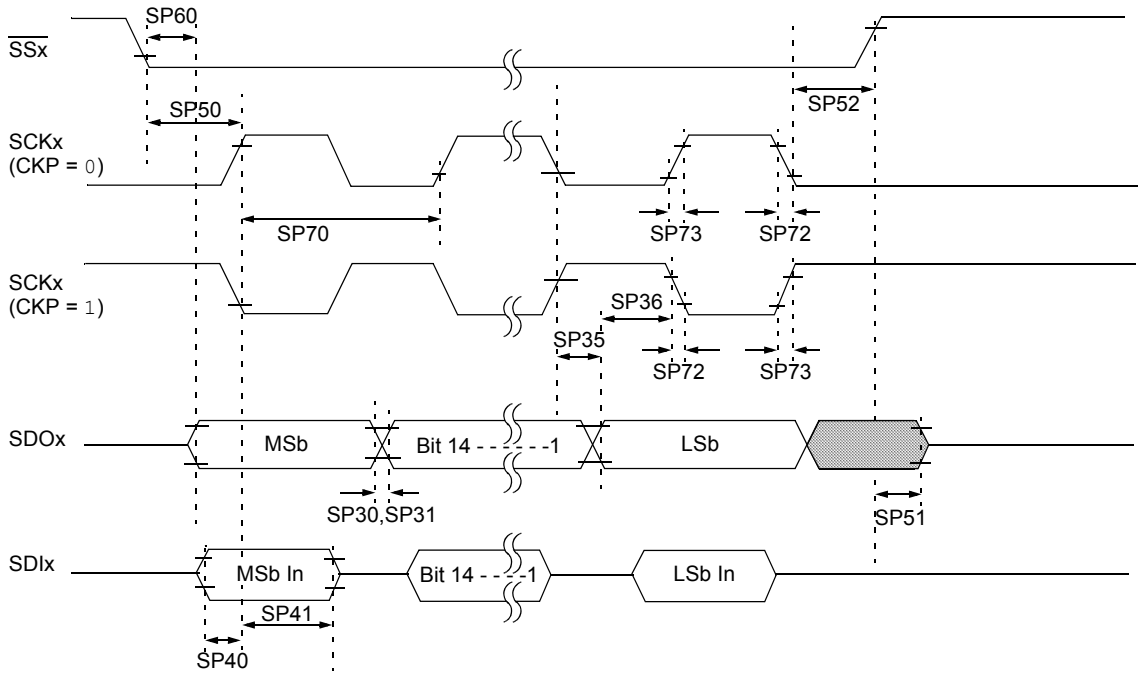



**TABLE 32-22: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SY00 | TPU | Power-up Period | — | 400 | 600 | μs | |
| SY10 | TOST | Oscillator Start-up Time | — | 1024 TOSC | — | — | TOSC = OSC1 period |
| SY11 | TPWRT | Power-up Timer Period | — | — | — | — | See **Section 29.1 "Configuration Bits"** and LPRC Parameters F21a and F21b (Table 32-20) |
| SY12 | TWDT | Watchdog Timer Time-out Period | — | — | — | — | See **Section 29.4 "Watchdog Timer (WDT)"** and LPRC Parameters F21a and F21b (Table 32-20) |
| SY13 | TIOZ | I/O High-Impedance from MCLR Low or Watchdog Timer Reset | 0.68 | 0.72 | 1.2 | μs | |
| SY20 | TMCLR | MCLR Pulse Width (low) | 2 | — | — | μs | |
| SY30 | TBOR | BOR Pulse Width (low) | 1 | — | — | μs | |
| SY35 | TFSCM | Fail-Safe Clock Monitor Delay | — | 500 | 900 | μs | -40°C to +85°C |
| SY36 | TVREG | Voltage Regulator Standby-to-Active Mode Transition Time | — | — | 30 | μs | |
| SY37 | TOSCDFRC | FRC Oscillator Start-up Delay | — | — | 29 | μs | |
| SY38 | TOSCDLPRC | LPRC Oscillator Start-up Delay | — | — | 70 | μs | |

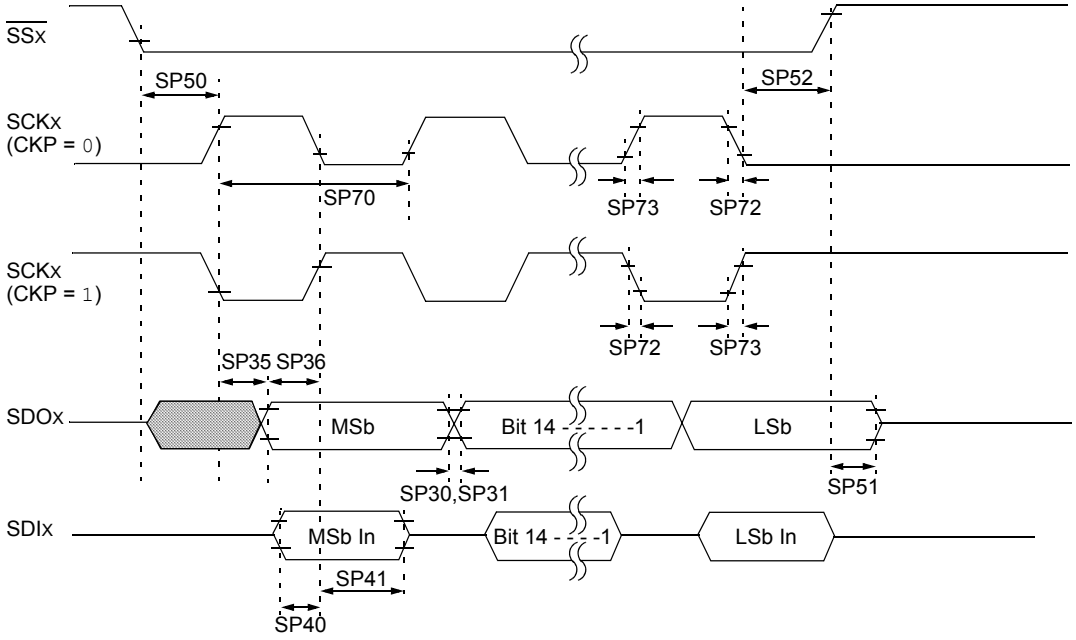
**Note 1:** These parameters are characterized but not tested in manufacturing.
**2:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

**FIGURE 32-28: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.

**FIGURE 32-29: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.

**FIGURE 32-35: ECAN™ MODULE I/O TIMING CHARACTERISTICS**

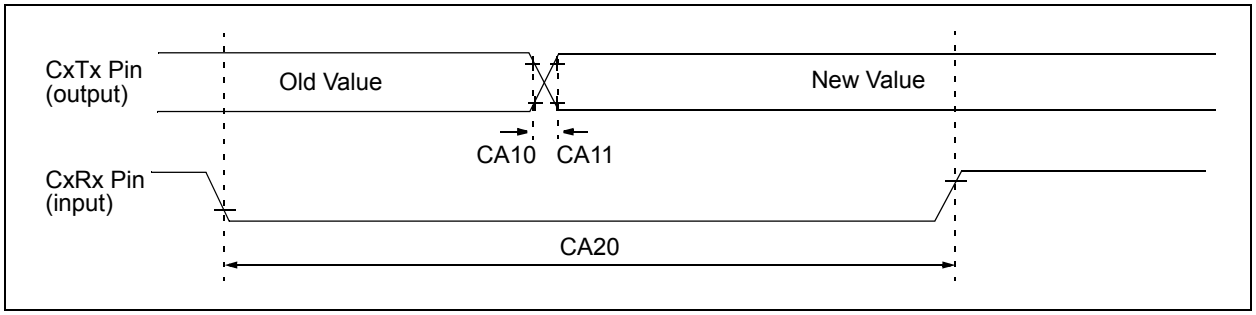



**TABLE 32-51: ECAN™ MODULE I/O TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| CA10 | TioF | Port Output Fall Time | — | — | — | ns | See Parameter DO32 |
| CA11 | TioR | Port Output Rise Time | — | — | — | ns | See Parameter DO31 |
| CA20 | TCWF | Pulse Width to Trigger CAN Wake-up Filter | 120 | — | — | ns | |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**FIGURE 32-36: UARTx MODULE I/O TIMING CHARACTERISTICS**

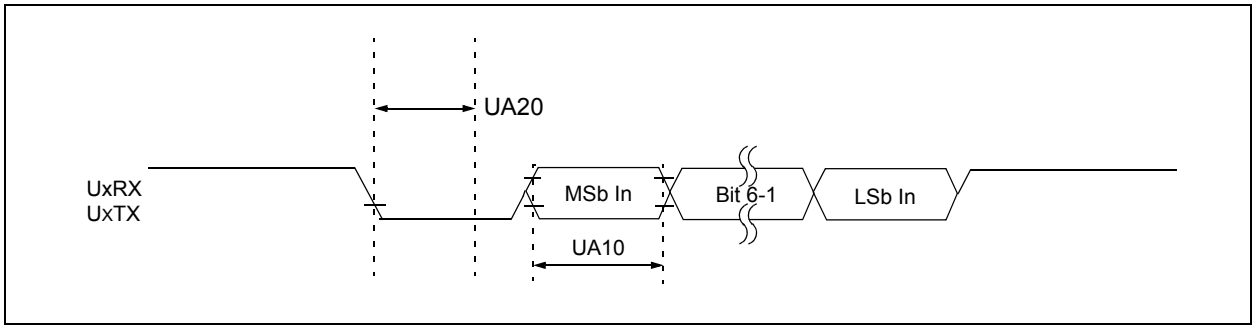



**TABLE 32-52: UARTx MODULE I/O TIMING REQUIREMENTS**

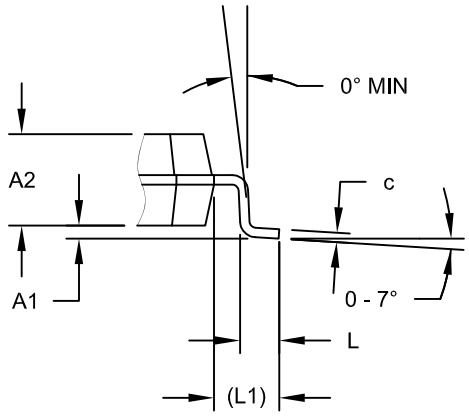
| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +125°C | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| UA10 | TUABAUD | UARTx Baud Time | 66.67 | — | — | ns | |
| UA11 | FBAUD | UARTx Baud Frequency | — | — | 15 | mbps | |
| UA20 | TCWF | Start Bit Pulse Width to Trigger UARTx Wake-up | 500 | — | — | ns | |

**Note 1:** These parameters are characterized but not tested in manufacturing.

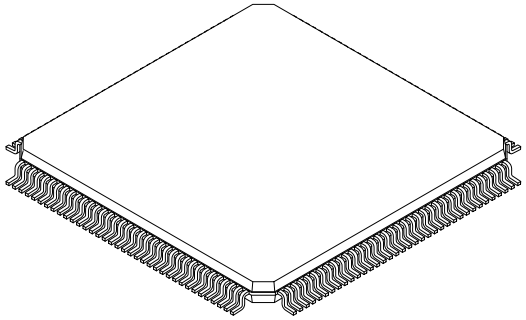
**2:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

## 144-Lead Plastic Low Profile Quad Flatpack (PL) – 20x20x1.40 mm Body, with 2.00 mm Footprint [LQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




**DETAIL A**



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Leads | N | | 144 | |
| Lead Pitch | e | | 0.50 BSC | |
| Overall Height | A | - | - | 1.60 |
| Molded Package Height | A2 | 1.35 | 1.40 | 1.45 |
| Standoff | A1 | 0.05 | - | 0.15 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 (REF) | |
| Overall Width | E | | 22.00 BSC | |
| Overall Length | D | | 22.00 BSC | |
| Molded Body Width | E1 | | 20.00 BSC | |
| Molded Body Length | D1 | | 20.00 BSC | |
| Lead Thickness | c | 0.09 | - | 0.20 |
| Lead Width | b | 0.17 | 0.22 | 0.27 |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-044B Sheet 2 of 2